Application Report

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High-Efficiency Power Solution Using DC/DC Converter for the DM365

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ABSTRACT

This reference design is intended for users designing with TMS320DM365 Processor. This design is ideal for achieving the requirement of a input voltage of 5V, and uses single-output high-efficiency DCDC Converters with integrated FETs for a highly flexible and small configuration.

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1 Introduction

In multi-voltage architectures, coordinated management of power supplies is necessary to avoid potential problems and ensure reliable performance. Power supply designers must consider the timing and voltage differences between core and I/O voltage supplies during power up and power down operations.

Sequencing refers to the order, timing and differential in which the two voltage rails are powered up and down. A system designed without proper sequencing may be at risk for two types of failures. The first of these represents a threat to the long term reliability of the dual voltage device, while the second is more immediate, with the possibility of damaging interface circuits in the processor or system devices such as memory, logic or data converter ICs.

Another potential problem with improper supply sequencing is bus contention. Bus contention is a condition when the processor and another device both attempt to control a bi-directional bus during power up. Bus contention may also affect I/O reliability. Power supply designers should check the requirements regarding bus contention for individual devices.

2 Power Requirements

The power specifications and sequencing requirements for TMS320DM365 Processor is shown in the table below.

Table 1. TMS320DM365 Power Specs

	PIN NAME(s)	VOLTAGE (V)	Imax (mA)	TOLERANCE	SEQUENCING ORDER
Core	CVDD, VDD12_PRTCSS, VDDA12_DAC, VPP	1.2*	650	±5%	1
I/O	VDDS18, VDD18_PRTCSS, VDDMXI, VDD18_SLDO, VDD18_DDR, VDDA18_PLL, VDDA18_USB, VDDA18_VC, VDDA18_ADC, VDDA18_DAC	1.8	95	±5%	2
I/O	VDDS33, VDDA33_USB, VDDA33_VC	3.3	51	±5%	3
I/O	VDD_AEMIF1_18_3 3, VDD_AEMIF2_18_3 3, VDD_ISIF18_33	1.8 / 3.3	65	±5%	Ramp with appropriate voltage

Note:

- If running DM365 @ 300MHz, then CVDD, VDD12_PRTCSS, VDDA12_DAC and VPP = 1.35V and Imax = 800mA.
- If using PRTCSS, power-up sequencing changes to:

1. Power on PRTCSS core (1.2-V) while RESET is low
2. Power on PRTCSS I/O (1.8-V)
3. Power on Main core (1.2-V)
4. Power on Main I/O (1.8-V))
5. Power on Main/Analog I/O (3.3-V)

3 Features

The design uses the following high-efficiency DCDC Converters with integrated FETs

Devices:	**TPS62260(3.3V),TPS62290(1.2V),TPS62231(1.8V)**
Power supply specs:	
Vin	5 V ± 10%
Vout1	1.2 V ± 5% at 800 mA
Vout2	1.8 V ± 5% at 200 mA
Vout3	3.3 V ± 5% at 200 mA
Sequencing	1) Vout1 2) Vout2 3) Vout3

TPS62260

- High Efficiency Step Down Converter
- Output Current up to 600mA
- Power Save Mode at Light Load Currents
- Allows < 1 mm Solution Height

TPS62290

- High Efficiency Step Down Converter
- Up to 1-A Output Current
- Power Save Mode at Light Load Currents
- Output Voltage Accuracy in PWM mode ±1.5%

TPS62231

- 3 MHz switch frequency
- Up to 94% efficiency
- Output Peak Current up to 500 mA
- Small External Output Filter Components (1.0µH/ 4.7µF)
- Small 1 × 1.5 × 0.6mm3 SON Package
- Fixed 1.8 V eliminates need for external voltage-setting resistors

More information on the Devices can be found from the data sheets.

TPS62260 –SLVS763B

TPS62290 –SLVS764C

TPS62231 –SLVS941

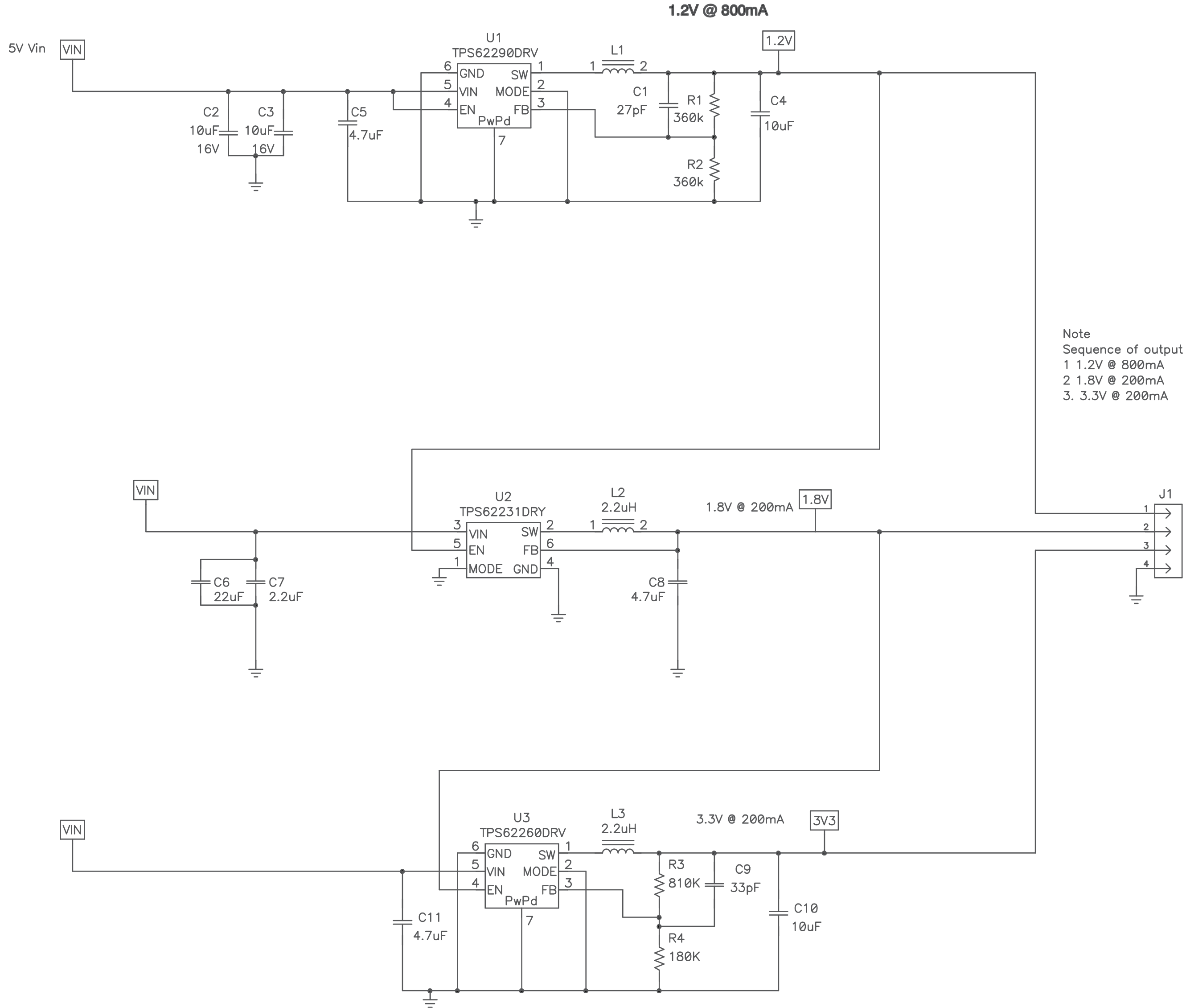

Figure 1. PMP5047 Reference Design Schematic

Proper sequencing is insured in the design with the use of enable pins. The Core 1.2V at 1000mA (TPS62290) comes first, which in turn enable the TPS62231 and output of TPS62231 enables TPS62260 device thus, following the required sequence.

4 List of Material

Table 2. PMP5047 List of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR	Area
1	C1	27 pF	Capacitor, Ceramic, 0.01 µF, 10-V, X7R, 15%	0603	Std	TDK	5650
2	C2	10 µF	Capacitor, Ceramic, 16V, X7R, 20%	1206	C3216X7R1C106M T	TDK	15390
	C3	10 µF	Capacitor, Ceramic, 16V, X7R, 20%	1206	C3216X7R1C106M T	TDK	15390
1	C4	10 µF	Capacitor, Ceramic, 6.3V, X5R, 10%	0603	C0603CH0J106k	TDK	5650
1	C5	4.7 µF	Capacitor, Ceramic, 10V, X5R, 10%	0603	C0603CH1A475K	TDK	5650
1	C6	22 µF	Capacitor, Ceramic, 10V, X5R, 20%	1210	Std	Std	83,600
1	C7	2.2 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0402	JDK105BJ225MV	Taiyo Yuden	2800
1	C8	4.7 µF	Capacitor, Ceramic, 6.3V, X5R, 20%	0402	JDK105BJ475MV	Taiyo Yuden	2800
1	C9	33 pF	Capacitor, Ceramic, 16V, X7R, 15%	0402	Std	TDK	2800
1	C10	10 µF	Capacitor, Ceramic, 6.3V, X5R, 15%	0603	Std	TDK	5650
1	C11	4.7 µF	Capacitor, Ceramic, 6.3V, X5R, 15%	0603	Std	TDK	5650
1	J1	PEC36SAAN	Header, Male 4-pin, 100mil spacing, (36-pin strip)	0.100 inch x 4	PEC36SAAN	Sullins	50000
1	L1	2.2 µH	Inductor, SMT, 2.1A, 0.110Ω	0.118 x 0.118 inch	LPS3015-222ML	Coilcraft	26,560
1	L2	2.2 µH	Inductor, SMT, 0.7A, 230-mΩ	0805	MIPSZ20120D2R2	FDK	10160
1	L3	2.2 µH	Inductor, 1A, 200-mΩ	0.080 x 0.080 inch	EPL2010-222ML	Coilcraft	108,300
2	R1	360k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
	R2	360k	Resistor, Chip, 1/16W, 1%	0603	Std	Std	5650
1	R3	810K	Resistor, Chip, 1/16W, 1%	0402	Std	Std	2800
1	R4	180K	Resistor, Chip, 1/16W, 1%	0402	Std	Std	2800
1	U1	TPS62290DRV	IC, 1A xx V Step Down Converter	SON-6	TPS6229xDRV	TI	16416
1	U2	TPS62231DRY	IC, 3MHz Ultra Small Step Down Converter, x.x V	QFN	TPS62232DRY	TI	6020
1	U3	TPS62260DRV	IC, 2.25MHz 600mA Step-Down Converter	SON-6[DRV]	TPS62260DRV	TI	20736

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.

2. These assemblies must be clean and free from flux and all contaminants.
Use of no clean flux is not acceptable.

3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.

4. Ref designators marked with an asterisk ('**') cannot be substituted.
All other components can be substituted with equivalent MFG's components.

5 Test Result

The startup waveform, shown in Figure 2, demonstrates that the required sequencing order is followed.

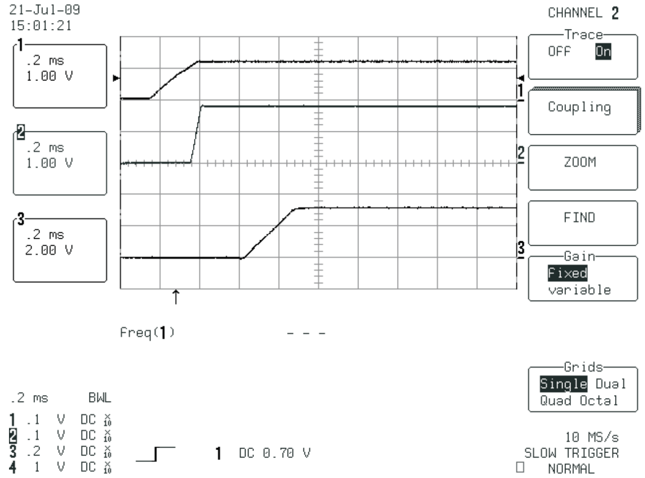

Figure 2. Shows Sequencing in Start up Waveform

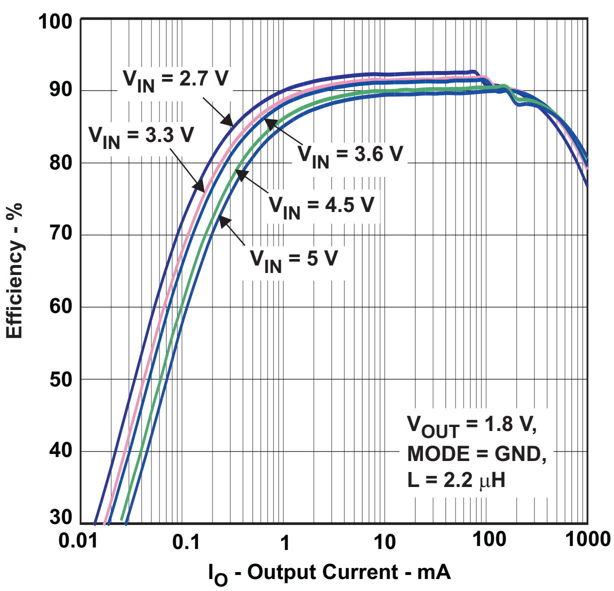

Figure 3. Efficiency vs Output Current (TPS62290)

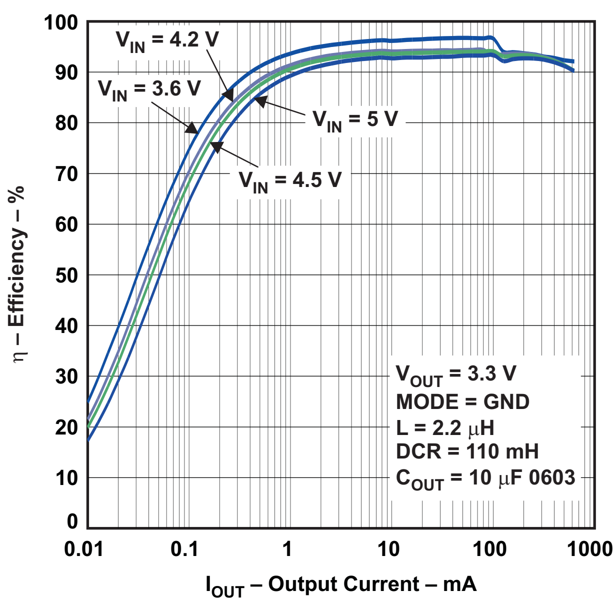

Figure 4. Efficiency vs Output Current (TPS62260)

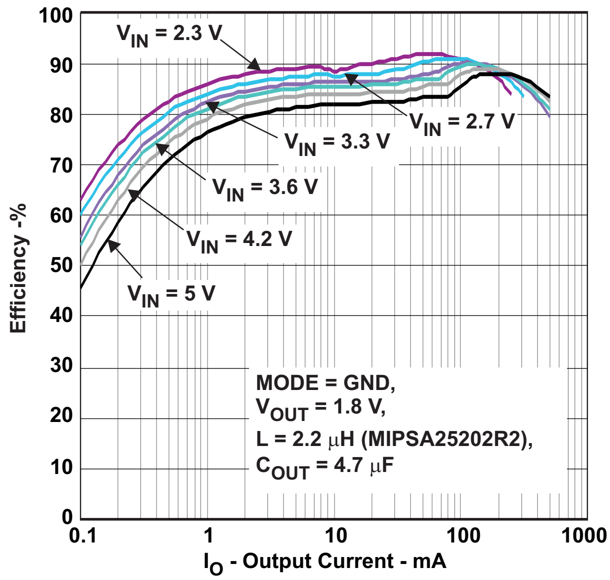

Figure 5. Efficiency vs Output Current (TPS62231)