Optimizing OMAP3630 BOOT Sequence Using the TPS65023-Q1

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ABSTRACT

The TPS65023-Q1 multi-rail power-supply integrated circuit (IC) realizes all necessary features to supply the OMAP3630 processor. The TPS65023-Q1 device is an integrated power-management IC (PMIC). The device is suited for applications powered by one Li-Ion or Li-Polymer cell requiring multiple power rails. The TPS65023-Q1 device provides three highly-efficient 1500-mA step-down DC-DC converters, two general-purpose 200-mA low-dropout voltage regulators (LDOs), and one 30-mA real time clock (RTC) LDO.

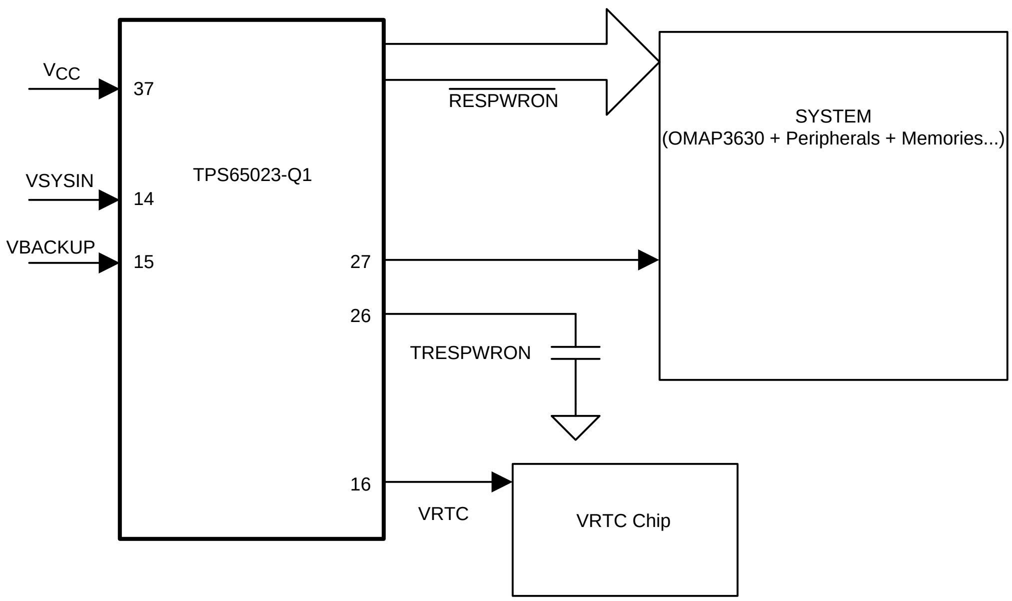


Figure 1.

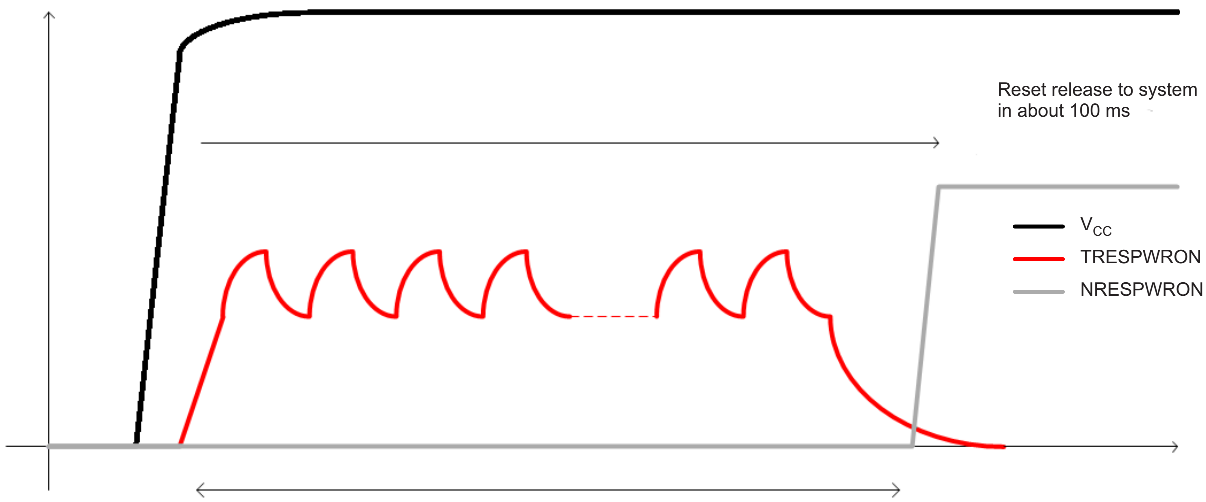
Contents

1 Introduction

The OMAP3630 processor uses the open drain $\overline{\text{RESPWRON}}$ signal from the TPS65023-Q1 device as a global reset for the application. The $\overline{\text{RESPWRON}}$ is held low when power is initially applied to the TPS65023-Q1 device. The RTC voltage is monitored and the $\overline{\text{RESPWRON}}$ signal is maintained low as long as the voltage is below 2.4 V. For proper BOOT sequence, the $\overline{\text{RESPWRON}}$ signal must have an adequate delay. In the event of a non delay, the OMAP3630 device fails its BOOT sequence.

The TPS65023-Q1 device integrates a timer providing the necessary $\overline{\text{RESPWRON}}$ delay by connecting an external capacitor to the TRESPWRON pin (pin 26). A 1-nF capacitor provides a 100-mS delay.

The integrated timer is only activated at power up when the RTC voltage is below 2.4 V (see Figure 2 and Figure 3). When the RTC voltage level is above 2.4 V at power up (the VBACKUP pin is above 2.65 V) the $\overline{\text{RESPWRON}}$ signal bounces from low to high with no delay (see Figure 4 and Figure 5).



Note: The TRESPWRON signal has around 100 charges and discharges to monitor the reset signal releasing in accord with the TPS65023-Q1 specifications.

Figure 2. In 5-V Range

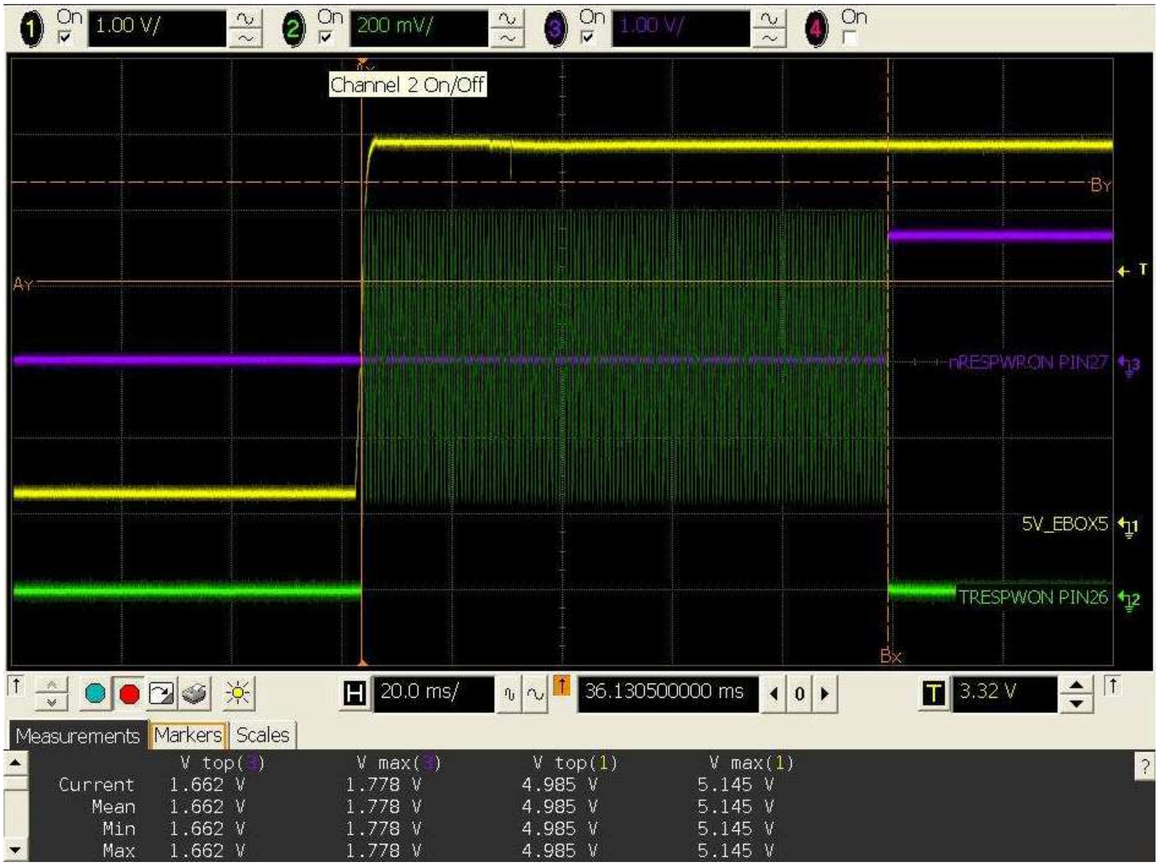
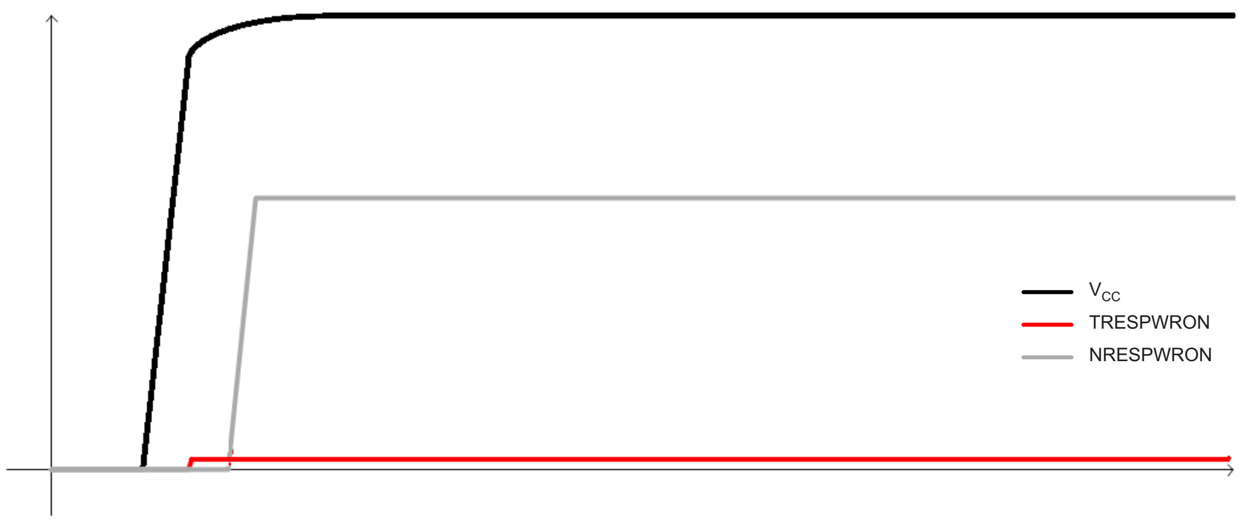


Figure 3. VRTC Level is Lower than 2.4 V at Power Up



Note: No charges or discharges at the TRESPWRON pin and no 100-ms delay.

Figure 4. In 5-V Range

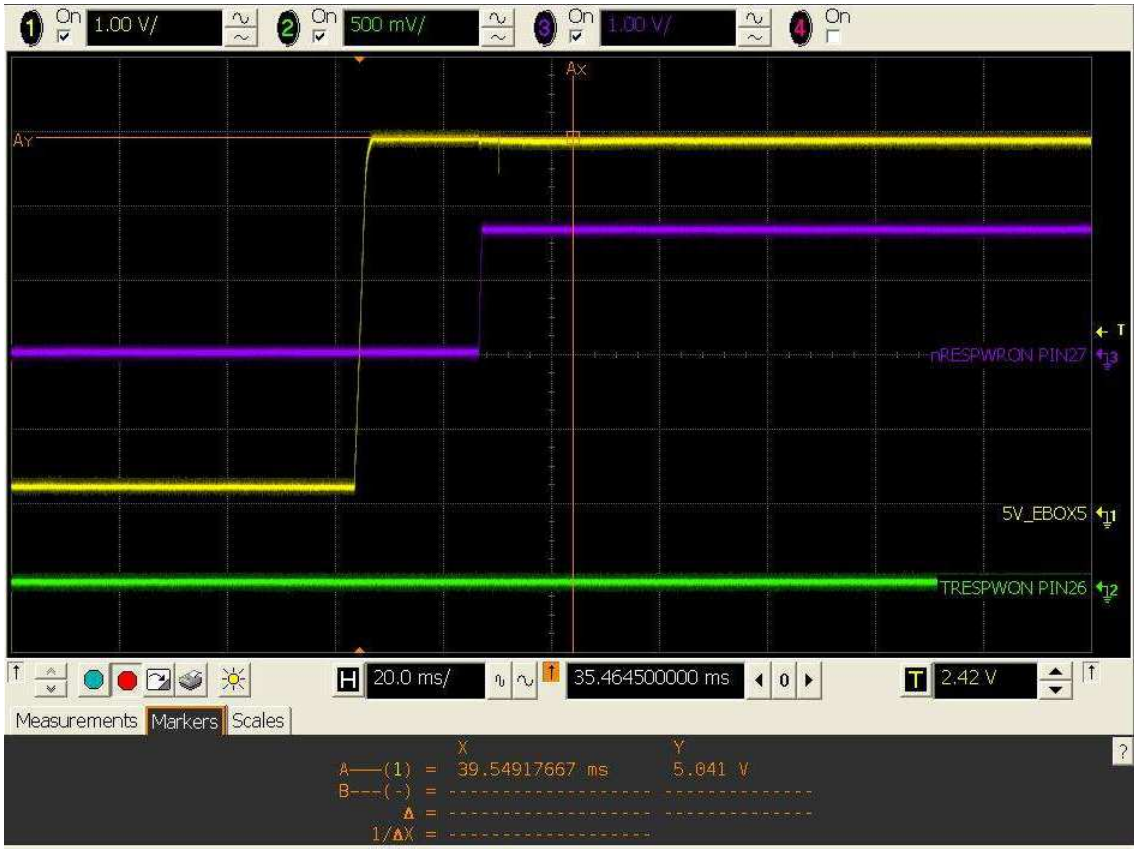


Figure 5. VRTC Level is Higher than 2.4 V at Power Up

For some OMAP3630 applications, when power is down, the real time clock (RTC) chip must always be powered and the battery is required to provide this power. If the battery is connected to the TPS65023-Q1 VBACKUP pin (pin 15), the VRTC level is above 2.4 V and the timer providing the $\overline{\text{RESPWRON}}$ delay cannot be triggered. In these applications the battery must be connected to VRTC chip through external switch.

2 Solution

An external circuit is added because the TPS65023-Q1 VBACKUP internal switch can not be used. The external circuit provides power to RTC chip from the best power source between 3.3 V—diode drop and battery. The RTC chip minimum supply voltage is 1.8 V. In order to keep the information the RTC supply must be disconnected below 1.8 V.

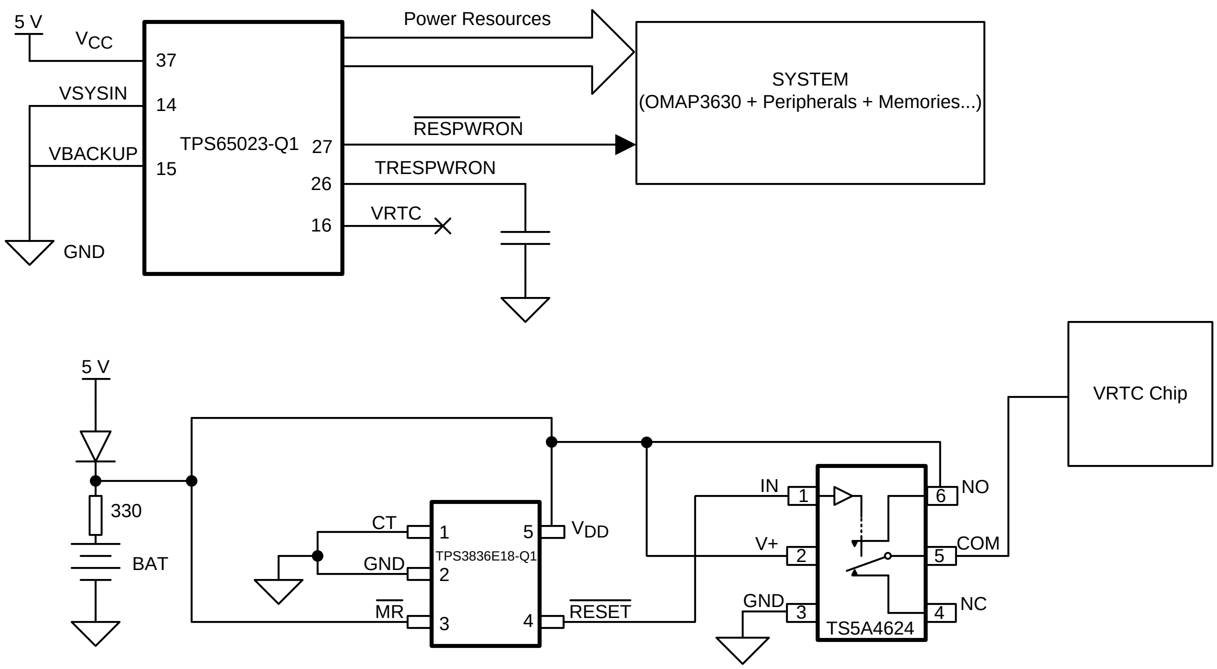


Figure 6. External Circuit Connections

3 Description

The battery is charged from a 3.3-V supply with 330-Ω series resistor. The diode provides charging path to battery and supply to external circuit and VRTC chip when the 3.3-V is present. The battery supplies the external circuit and the VRTC chip when the 3.3-V is absent.

The voltage supervisor TPS3836E18-Q1 $\overline{\text{RESET}}$ pin is low if the battery voltage drops below 1.8 V. The $\overline{\text{RESET}}$ pin is the logic input for the analog switch, the TS5A4624 device. A high $\overline{\text{RESET}}$ level connects the battery to the VRTC chip. A low $\overline{\text{RESET}}$ level disconnects battery form VRTC chip (see Figure 6).

The external circuit current consumption is below 2 µA if the battery voltage is higher than 1.8 V when connected to VRTC. External circuit current consumption is up to 10 µA if battery voltage is below 1.8 V. The 10-µA current consumption is because of the low voltage of the external circuit but does not cause any voltage drainage since the battery is disconnected from VRTC chip.

With this configuration the VRTC chip is never be un-powered except when the battery voltage is below 1.8 V. And also the $\overline{\text{RESPWRON}}$ signal is always delayed (100 mS with 1 nF) at power up.

4 Lab Measurement at All Temperatures

The external circuit was bench tested at all three temperatures. The data was taken for the external circuit voltage thresholds at witch battery is connected or disconnected from VRTC chip (see Table 1, Figure 8, and Figure 9. Also the external circuit consumption current was measured (see Figure 10).

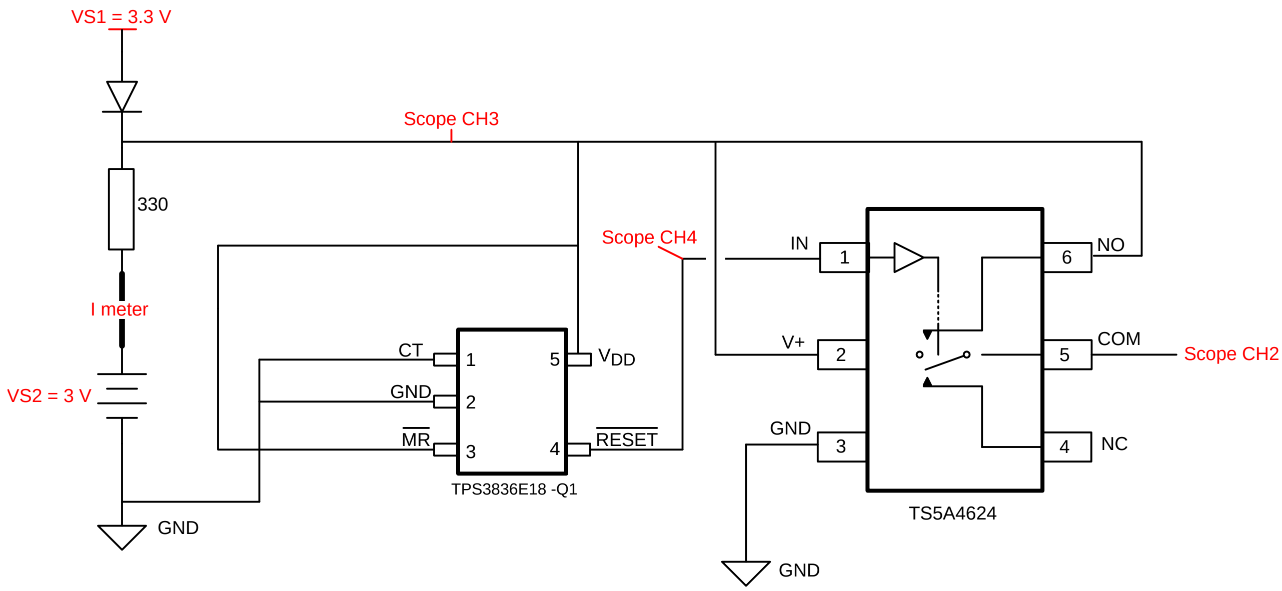


Figure 7. External Circuit Lab Measurements

Table 1. Threshold Conditions at Various Temperatures VRTC Chip Connected and Disconnected from the Battery

TEMPERATURE (°C)	VS2 VOLTAGE (V)	BATTERY CONDITION
–40	> 1.73	VRTC chip connected
	< 1.7	VRTC chip disconnected
25	> 1.74	VRTC chip connected
	< 1.71	VRTC chip disconnected
125	> 1.74	VRTC chip connected
	< 1.7	VRTC chip disconnected

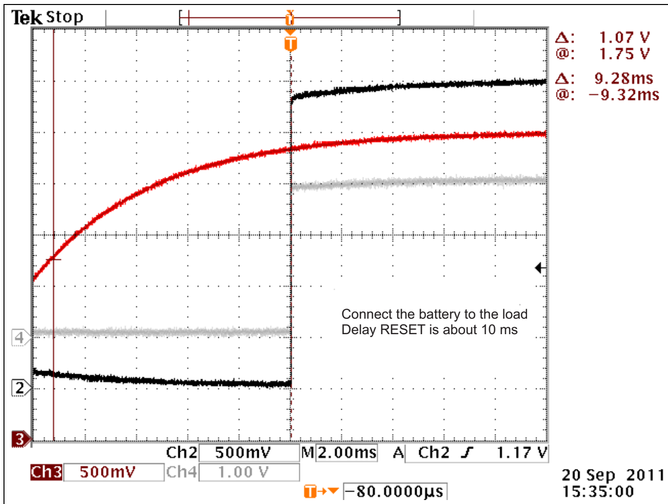


Figure 8.

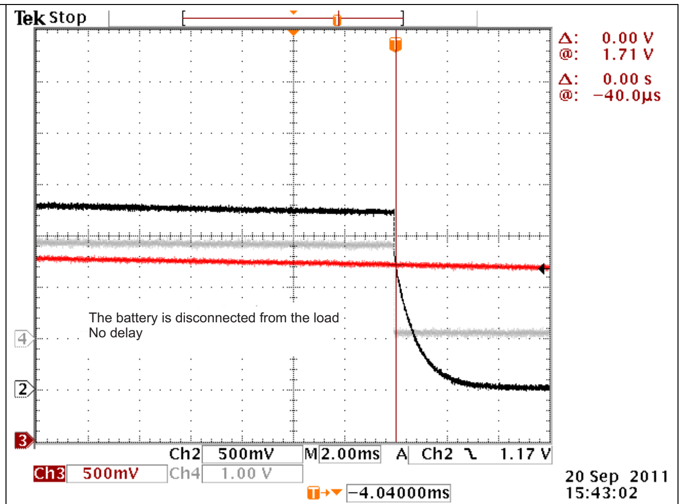


Figure 9.

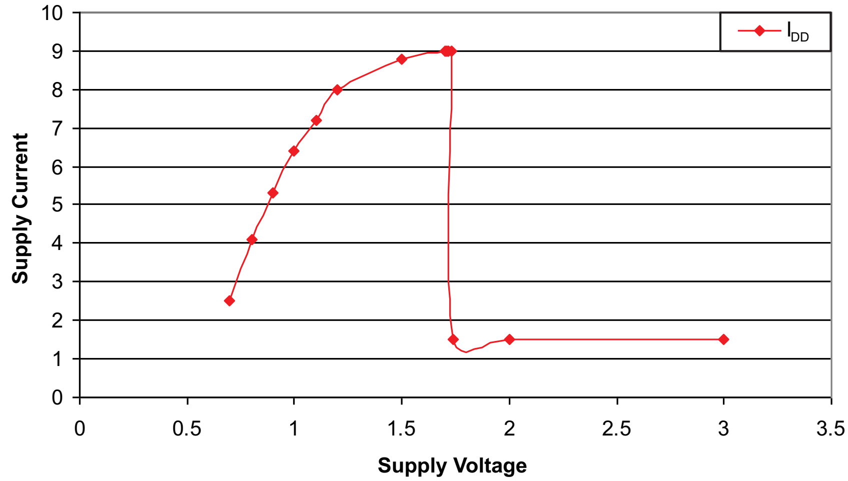


Figure 10. External Circuit Current Consumption I_{DD} (µA) versus Supply Voltage V_{DD} (V) at 125°C Worse Case

5 Conclusion

Based on this bench data and the application examples, the TPS65023-Q1 device implementation above is the ideal answer to provide a solution to OMAP3630 BOOT sequence.

From this solution, the VRTC chip will never be unpowered except when the battery voltage is below 1.8 V which is the level required by the system. Furthermore; the $\overline{\text{RESPWRON}}$ signal is always delayed (100 mS with 1 nF) at power up.

For additional information, see the TPS65023-Q1 data sheet (SLVS927).

Revision History

Changes from Original (March 2012) to A Revision	Page
• Changed the device name from OMAP3630 to OMAP3630 throughout the document and added -Q1 to the TPS65023 device name	2

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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