

# TPS6505x Design Guide

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## ABSTRACT

This document is a guide for designers to use when designing with the TPS6505x PMU. The application report has 3 sections: an overview, schematic checklist, and PCB checklist.

### Contents

1	TPS6505x Overview .....	2
1.1	Quick Checklist.....	2
2	Schematic Checklist .....	3
2.1	VCC Input Filter .....	3
2.2	RESET and Threshold .....	3
2.3	LDOs .....	3
2.4	DCDC Regulators.....	3
3	PCB Checklist .....	5
4	References .....	5

### List of Figures

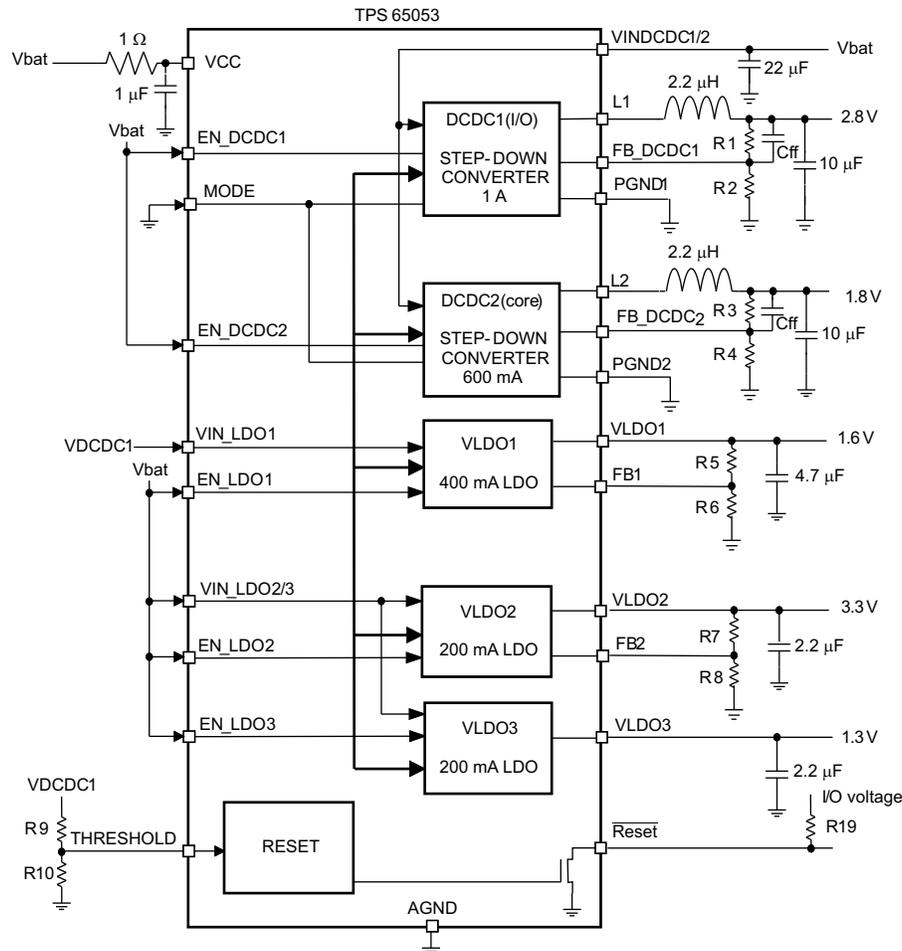
1	TPS6505x PCB .....	5
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### List of Tables

1	Typical Resistor Values .....	4
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## 1 TPS6505x Overview

The TPS65053x has 2 DCDC buck regulators, 3 LDOs, and a reset output signal. The TPS6505x has 2 DCDC buck regulators, 4 LDOs, and a reset output signal.



### 1.1 Quick Checklist

- VCC input filter
- RESET pull-up
- Threshold resistor divider, if applicable
- LDOs
  - Input capacitor
  - Output Capacitor
- DCDCs
  - Input capacitor
  - Output Capacitor
  - Output Inductor
  - Feedback Resistors

## 2 Schematic Checklist

### 2.1 VCC Input Filter

The VCC pin supplies the digital and internal analog reference. The buck regulators will inject switching noise as is the nature of buck regulators; therefore, the VCC pin should be a filtered input. Use a 1-Ω resistor and 1-μF capacitor to form an RC low-pass filter.

### 2.2 RESET and Threshold

RESET is an output logic signal for supplying a reset or a power good signal to an external circuit or IC. RESET is an open-drain output and requires a pull-up resistor to any desired voltage. A 100-kΩ resistor is typical for most applications.

Threshold sets the voltage at which RESET comparator transitions from LOW to HIGH. To set the voltage, use a resistor divider from the desired voltage rail. Care should be taken in selecting the magnitude of the resistors. Larger resistance decreases the power loss through the divider while smaller resistance decreases noise susceptibility. Resistors between 20 kΩ and 300 kΩ are recommended.

### 2.3 LDOs

The LDOs require an input and output capacitor for proper regulation.

#### 2.3.1 Capacitors

A ceramic 2.2-μF capacitor is recommended for both VINLDO1 and VINLDO2/3 for TPS65053x and VINLDO1, VINLDO2, and VINLDO3/4 for TPS6505x. For each output, a ceramic 4.7 μF capacitor is recommended.

Be sure to take into account the DC bias derating, thermal derating and manufacturing variance. It is recommended to use a ceramic capacitor of at least 2x the voltage rating as the voltage applied to the capacitor. Also, either X5R or X7R and ±10% or ±20% capacitors are recommended.

#### 2.3.2 Feedback

If feedback resistors are required to set the LDO output voltage, use the following equation to calculate the recommended resistors for the divider input. For most applications, the feedback resistors should be in the 100-kΩ range.

$$R3 = R4 \times \left( \frac{V_{out}}{V_{REF\_LDO}} \right) - R4 \quad (1)$$

Where:

$$V_{REF\_LDO} = 1 \text{ V}$$

$$R4 \approx 100 \text{ k}\Omega$$

### 2.4 DCDC Regulators

The DCDC regulators require an input and output filter for proper regulation.

#### 2.4.1 Capacitors

A ceramic 22-μF capacitor is recommended for both VINDCDC1/2. For each output, a ceramic 10 - 22 μF capacitor is recommended.

Be sure to take into account the DC bias derating, thermal derating and manufacturing variance. It is recommended to use a ceramic capacitor of at least 2x the voltage rating as the voltage applied to the capacitor. Also, either X5R or X7R and ±10% or ±20% capacitors are recommended.

### 2.4.2 Feedback

If feedback resistors are required to set the DCDC output voltage, use the following equation to calculate the recommended resistors for the divider input. For most applications, the feedback resistors should be in the 100-k $\Omega$  range.

$$R3 = R4 \times \left( \frac{V_{out}}{V_{REF\_LDO}} \right) - R4 \quad (2)$$

Where:

$$V_{REF\_LDO} = 0.6 \text{ V}$$

$$R4 \approx 100 \text{ k}\Omega$$

A feed forward capacitor maybe required for proper stability for the DCDC converter. [Table 1](#) provides calculated feedback resistors and appropriate feed forward capacitors for several output voltages.

**Table 1. Typical Resistor Values**

OUTPUT VOLTAGE	R1	R2	NOMINAL VOLTAGE	TYPICAL CFF
3.3 V	680 k $\Omega$	150 k $\Omega$	3.32 V	47 pF
3.0 V	510 k $\Omega$	130 k $\Omega$	2.95 V	47 pF
2.85 V	560 k $\Omega$	150 k $\Omega$	2.84 V	47 pF
2.5 V	510 k $\Omega$	160 k $\Omega$	2.51 V	47 pF
1.8 V	300 k $\Omega$	150 k $\Omega$	1.80 V	47 pF
1.6 V	200 k $\Omega$	120 k $\Omega$	1.60 V	47 pF
1.5 V	300 k $\Omega$	200 k $\Omega$	1.50 V	47 pF
1.2 V	330 k $\Omega$	330 k $\Omega$	1.20 V	47 pF

### 2.4.3 Inductor

The two converters operate typically with 2.2- $\mu\text{H}$  output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operating conditions. For output voltages higher than 2.8 V, an inductor value of 3.3  $\mu\text{H}$  minimum should be selected, otherwise the inductor current will ramp down too fast causing imprecise internal current measurement and therefore increased output voltage ripple under some operating conditions in PFM mode.

The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductance will directly influence the efficiency of the converter. Therefore, an inductor with the lowest DC resistance should be selected for highest efficiency.

[Equation 3](#) calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with [Equation 3](#). This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = V_{out} \times \left( \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f_{sw}} \right)$$

$$I_{L_{max}} = I_{out_{max}} + \frac{\Delta I_L}{2} \quad (3)$$

Where:

$\Delta I_L$  = Peak-to-peak inductor ripple current

fsw = Switching Frequency (2.25-MHz typical)

L = Inductor Value

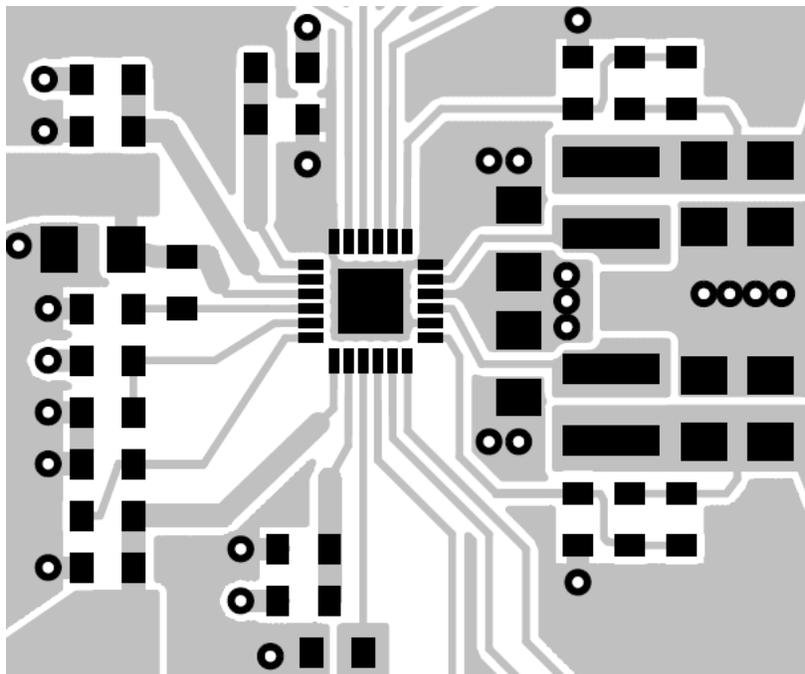
$I_{L_{max}}$  = Maximum Peak Inductor current

$I_{out_{max}}$  = Maximum DC Inductor current

### 3 PCB Checklist

Use the following list to ensure a high-performance and efficient PCB:

- The input capacitors for the DCDC converters should be placed as close as possible to the VINDCDC1/2 pin and the PGND1 and PGND2 pins.
- The inductor of the output filter should be placed as close as possible to the device to provide the shortest switch node possible, reducing the noise emitted into the system and increasing the efficiency.
- Sense the feedback voltage from the output at the output capacitors to ensure the best DC accuracy. Feedback should be routed away from noisy sources such as the inductor. If possible, route on the opposing side as the switch node and inductor and place a GND plane between the feedback and the noisy sources or keep out from underneath them entirely.
- Place the output capacitors as close as possible to the inductor to reduce the feedback loop as much as possible. This ensures best regulation at the feedback point.
- Place the device as close as possible to the most demanding or sensitive load. The output capacitors should be placed close to the input of the load. This ensures the best AC performance possible.
- The input and output capacitors for the LDOs should be placed close to the device for best regulation performance.
- A common ground plane is recommended for the device layout. The AGND can be separated from the PGND but, a large low parasitic PGND is required to connect the PGNDx pins to the CIN and external PGND connections.



**Figure 1. TPS6505x PCB**

### 4 References

1. *TPS6505xx 5-Channel Power Management IC With Two Step-Down Converters and Three Low-Input Voltage LDOs* datasheet ([SLVS754](#))
2. *6-Channel Power MGMT IC With Two Step-down Converters and 4 Low-input Voltage LDOs* datasheet ([SLVS710](#))

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