

# Optimizing High Side FET Voltage Ringing of Multiphase Voltage Regulators Part 2

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## ABSTRACT

With the rapid demand growth of the server and communication market, high-current CPUs and ASICs are popular in server and communication system design. Multiphase power solutions are widely adopted for supplying CPUs and ASICs. However, to achieve high power density, each power stage must deliver more energy to the load. This makes optimizing the voltage ringing of the high-side FET a challenge. This serial application report demonstrates the challenges of a low-voltage ringing design.

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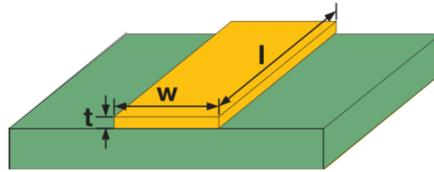
## 1 Introduction

To reduce the FET voltage ringing, system designers usually add an RC snubber between the switching node and ground. However, these only reduce the low-side FET voltage ringing. High-side FET voltage ringing still depends on the parasitic parameters of the input capacitors, and the PCB layout. Improper layout and input capacitors can result in excessive voltage ringing. This serial application report shows the voltage ringing mechanism of the formation, and discusses how to reduce the high-side voltage ringing in the design with appropriate input bypass capacitor selection, and layout design, that improves system reliability.

## 2 Copper and Via Parasitic Parameter Introduction

Ideally, the PCB copper trace and via are just a 0  $\Omega$  wire that connects different parts on the board. However, when considering a high-frequency signal, the parasitic parameters of the copper trace and via significantly impact the MOSFET voltage stress.

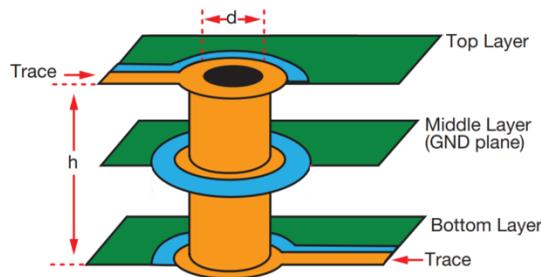
A PCB trace is made up of the parasitic resistor, inductance, and capacitor. Parasitic inductance is the focus when decreasing the voltage ring of the FET, as the FET has a high-impedance feature in high-frequency ranges. See [Figure 1](#) for a formula that calculates the approximate parasitic inductance of the copper trace.



**Figure 1. PCB Trace Parasitic Inductance**

As shown in [Figure 1](#), the length has more influence than the width when considering the parasitic inductance of the PCB trace. Thus, the bypass cap must be placed close to the Vin pin.

See [Figure 2](#) to view the parasitic inductance of the PCB via.



**Figure 2. Parasitic Inductance of the PCB Via**

To decrease via inductance effects, add more vias near the bypass cap pads. The parallel vias can lower the impedance, and the high-frequency noise can be easily absorbed.

An alternative to the experience formula shown in [Figure 1](#) is software. Software can also be used to calculate the parasitic parameter. The software extraction process can usually consider more practice parameters.

The example shown in [Section 3](#) uses software to extract the PCB trace, and the parameters of the vias.

### 3 Improper PCB Layout Example

#### 3.1 Improper PCB Layout and Related Parasitic Parameters

[Figure 3](#) illustrates an improper PCB layout example. The bypass cap is connected to the inner GND plane through a via and a single wire, which leads to high parasitic inductance. This inductance can make the bypass cap ineffective, and increase the FET voltage stress.

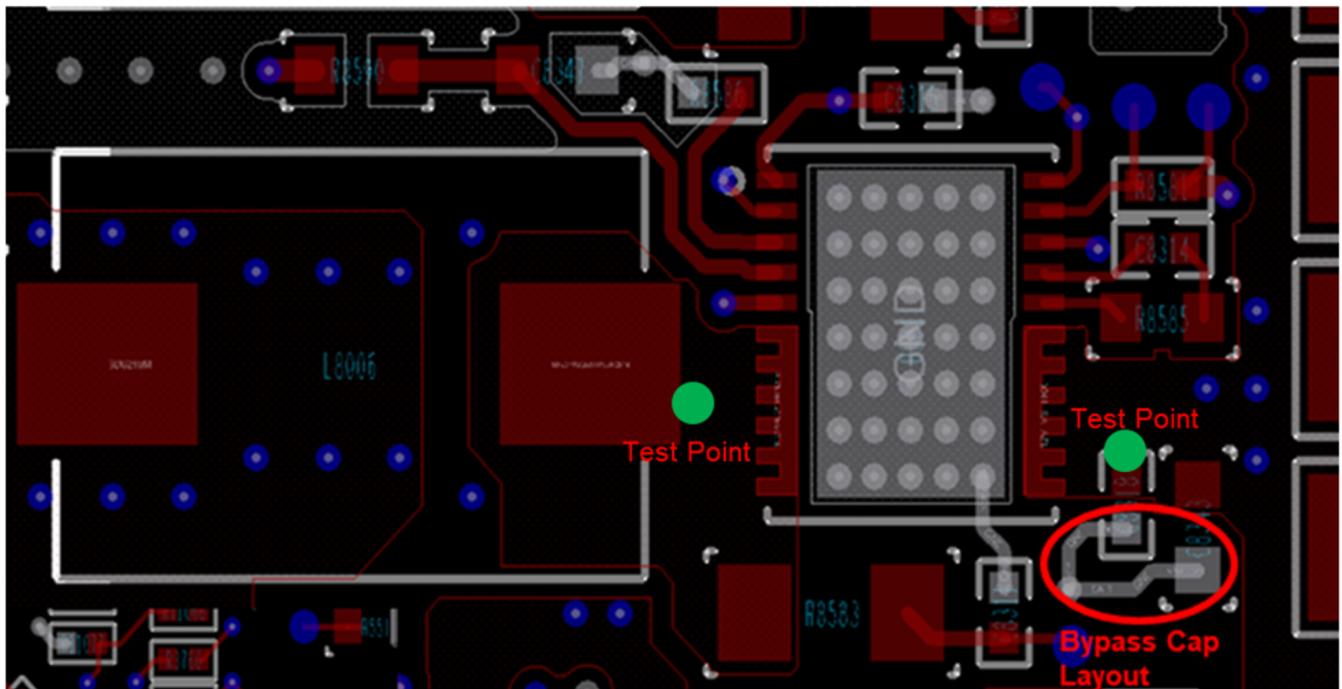


Figure 3. Improper PCB Layout Sample

As seen in Figure 4, the previously discussed parasitic parameters of the PCB can be extracted. Figure 4 also shows equivalent circuits.

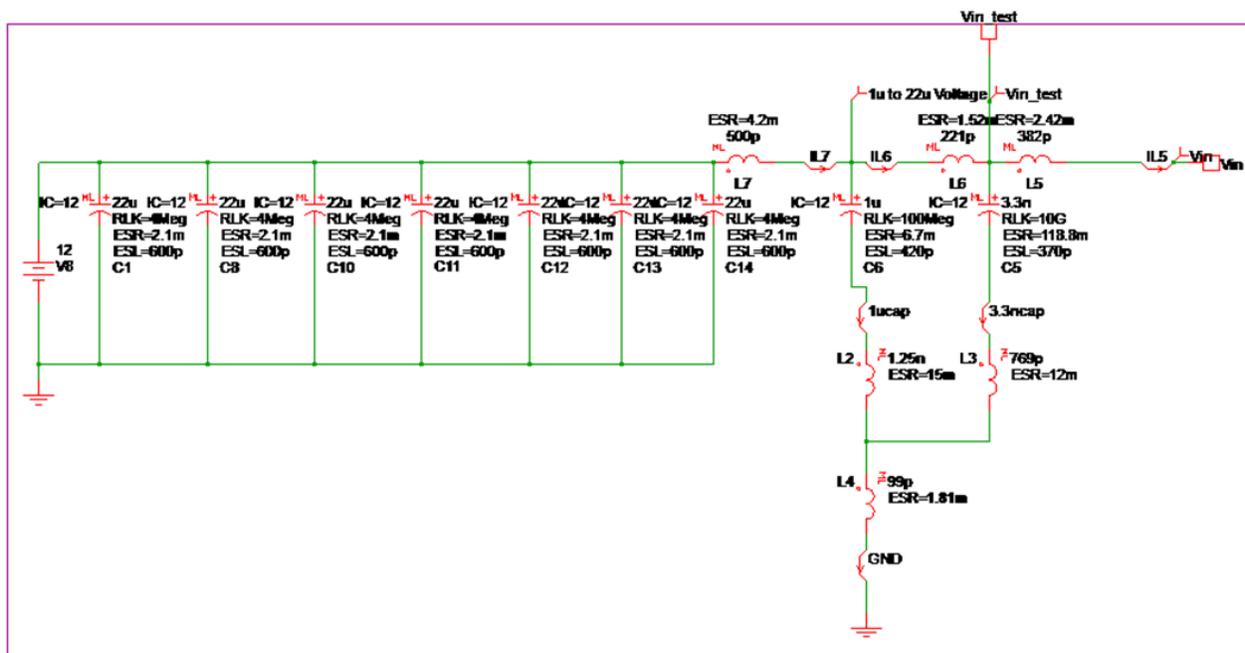


Figure 4. Equivalent Simulation Circuit of an Improper PCB layout

### 3.2 The Comparison Between Test Waveform and Simulation

Since the test probe can hardly touch the FET pin, the parasitic inductance is divided into two portions in the following discussion. The first one is above the equivalent circuit, and the second one is the parasitic inductance between the test point and FET pin. It is extracted as 382 pH.

Figure 5 displays test results on the real board. The high-side FET voltage stress is 17.45 V, and is not the normal dampened oscillation waveform. This is because the parasitic parameter causes different oscillation frequencies.

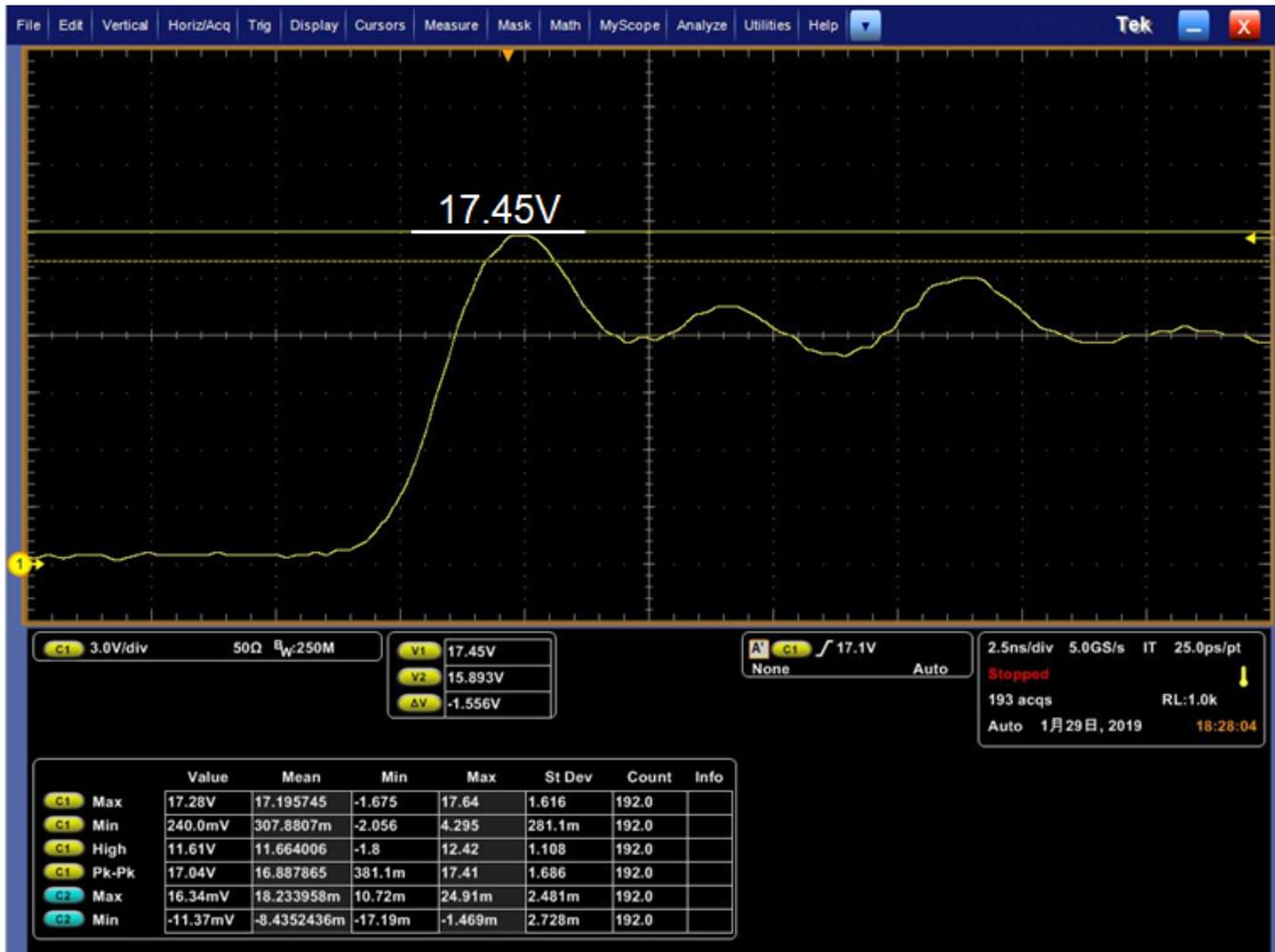


Figure 5. On-Board Test High-Side FET VDS Waveform

Figure 6 shows the simulation results after setting the simulation test point with the same test condition. The FET voltage stress is 17.68 V in simulation.

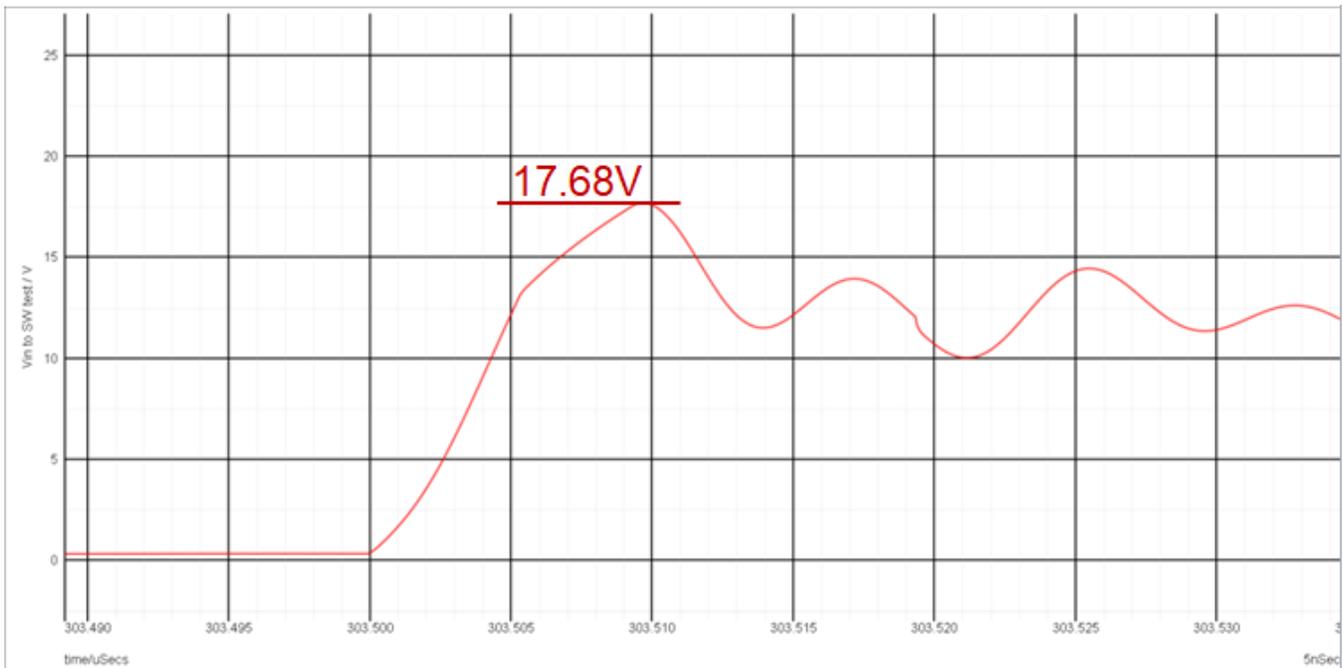


Figure 6. Simulation Waveform

Between Figure 5 and Figure 6, both the shape and peak values are well-correlated.

### 3.3 Layout recommendation

To decrease the peak ringing voltage, optimize the PCB layout, and change the bypass cap from 3.3 nF to 47 nF with the same package (0402). Figure 7 is the detailed layout recommendation for this case.

As more vias are added near the bypass caps, and with good GND-plane layout, the inductances decrease. A bigger bypass cap with the same package can also help decrease the bypass path impedance. Moreover, the bypass cap must be placed on the same side as the Vin and ground. Otherwise, the bypass path impedance becomes larger.

Figure 7 shows the changed parasitic inductance of the PCB trace and vias after optimization.

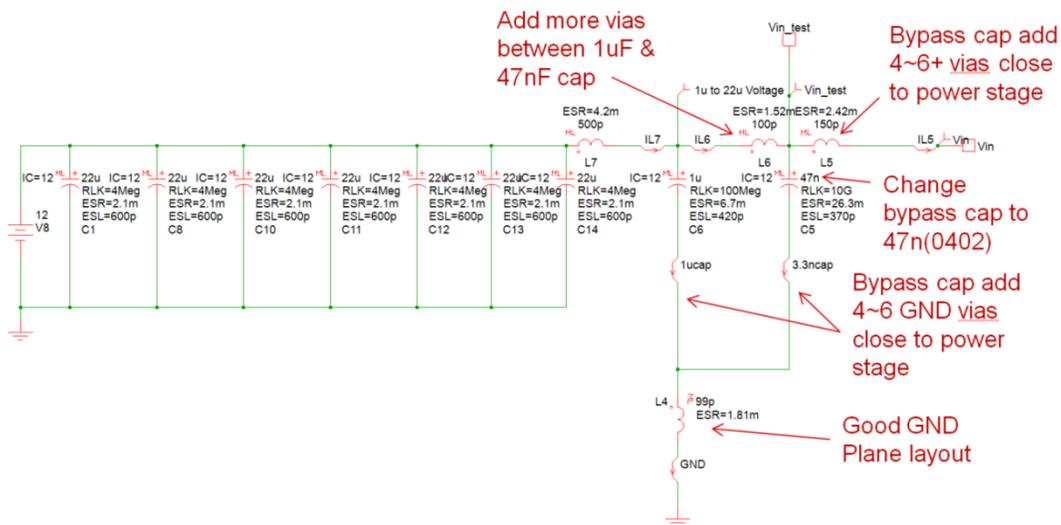
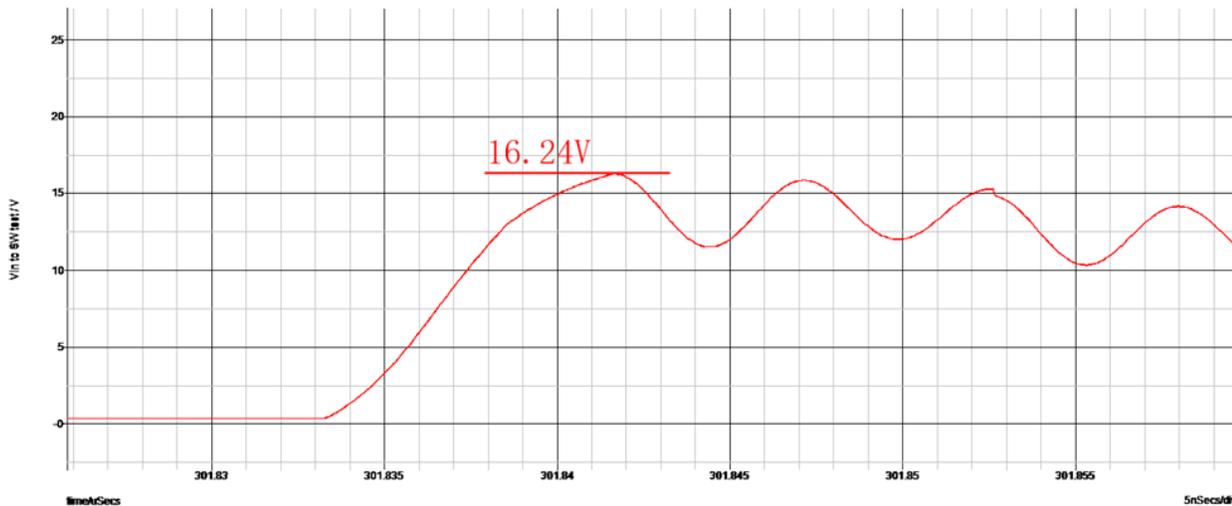


Figure 7. Layout Recommendation

### 3.4 Optimizing Result

Figure 8 shows the simulation results with a modified PCB. With the same test conditions, the peak, high-side FET VDS voltage can be reduced from 17.68 V to 16.24 V, which is a 1.44 V (or 8.2%) improvement.



**Figure 8. Simulation Results Based on Layout Recommendation**

Consequently, PCB layout and bypass cap play an important role in reducing high-side FET voltage ringing.

## 4 Conclusion

High-side FET voltage ringing in high-current, multiphase applications can be optimized by:

- PCB layout Optimization
  - The bypass cap must be placed on the same side of the power stage to reduce parasitic inductance from the via
  - The bypass cap must be connected through solid VIN and GND placement to reduce parasitic inductance from the trace
- Choosing the correct bypass cap type, package, and capacitance is also crucial in reducing the FET voltage ringing.

## 5 References

- [Home - TDK Electronics](#)
- Texas Instruments, [Analog Engineer's Pocket Reference](#)
- Texas Instruments, [Optimizing High Side FET Voltage Ringing of Multiphase Voltage Regulators Part 1](#)

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