Pad Configuration Tool

Texas Instruments Family of Products

User's Guide



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Read This First

Community Resources

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TI Embedded Processors Wiki — Texas Instruments Embedded Processors Wiki

Established to assist developers using the many Embedded Processors from Texas Instruments to get started, help each other innovate, and foster the growth of general knowledge about the hardware and software surrounding these devices.

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About This Manual

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Information About Cautions and Warnings

This book may contain cautions and warnings.

CAUTION

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

WARNING

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.



Register, Field, and Bit Calls

The naming convention applied for a call consists of:

- For a register call: < Module name>.< Register name>; for example: UART.UASR
- For a bit field call:
 - <Module name>.<Register name>[End:Start] <Field name> field; for example, UART.UASR[4:0]
 SPEED bit field
 - <Field name> field <Module name>.<Register name>[End:Start]; for example, SPEED bit field UART.UASR[4:0]
- For a bit call:
 - <Module name>.<Register name>[pos] <Bit name> bit, for example, UART.UASR[5] BIT_BY_CHAR bit
 - <Bit name> bit <Module name>.<Register name>[pos]; for example, BIT_BY_CHAR bit UART.UASR[5]

To help the reader navigate the document, each register call is hyperlinked to its register description in the register manual section. After each register description, a table summarizes all hyperlinked register calls.

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Coding Rules

Coding Rules

The programming models or code listings follow the rules:

Туре	Definition	Example				
File	Starts with the module name	PRCM_test1.c MCBSP1_init.h				
Variable	Global variables are prefixed by "g_" Pointers are prefixed by "p" Global pointers are prefixed by "g_p"	g_SDMA_LogicalChan pAddrCounter g_pSDMA_LogicalChan				
Function	Starts with the module name	PRCM_SetupClocks() ArmIntC_MaskInterrupts()				
Typedef	Ends with "_t"	PRCM_Struct_t				
Definition	Starts with the module name and is followed by the register name	#define SMS_ERR_TYPE *((volatileUint32*)0x680080F4) #define MCBSP2_RCR1_REG *((volatile Uint32*)0x4807401C)				
Enumeration	Starts with the module name	Typedef enum DMA_Mode_Label { INPUT_MODE OUTPUT_MODE } DMA_Mode_t;				



Flow Chart Rules

Flow charts follow the following rules:

Shape	Name	Definition
	Process	Any computational steps or processing function of a program; defined operation(s) causing change in value, form, or location of information
\diamond	Decision	A decision or switching-type operation that determines which of a number of alternate paths is followed
	Predefined process or sub- process	One or more named operations or program steps specified in a subroutine or another set of flow charts
	Data or I/O	General I/O function; information available for processing (input) or recording of processed information (output)
Start/Stop	Terminator	Terminal point in a flow chart: start, stop, halt, delay, or interrupt; may show exit from a closed subroutine
The high of the lact hose and the associated free increases or decomments as the based of the comment day when the comment day the day the comment day the day the comment day	Annotation	Additional descriptive clarification, comment
\bigcirc	On page connector (reference)	Exit to, or entry from, another part of chart in the same page
	Off page connector (reference)	The flow continues on a different page.
\otimes	Summing Junction	Logical AND
\bigcirc	Or	Logical OR
	Parallel mode (ISO)	Beginning or end of two or more simultaneous operations
	Flow Line	Lines indicate the sequence of steps and the direction of flow.

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Trademarks

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Pad Configuration Tool

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PCT Installation

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1 PCT Installation

CAUTION

Java[™] Runtime Environment, Standard Edition (v 1.7 or higher) must be installed before Pad Configuration Tool is installed.

The Pad Configuration Tool (PCT) installation procedure is composed of following steps.

1.1 PCT Installation Steps

To install the Pad Configuration Tool double click (java -jar in terminal for Linux users) on the "Installer-PCT-*xxxx*SR*x.x*-v*x.x.x.x*" file. The installer will execute and display the License Agreement window shown in Figure 1. You must either accept the conditions of the license or have a signed SLA to proceed further. Select an option.

When the conditions of the license agreement are accepted or the SLA option is selected, the "Next" button will become active. In the "Export Control Notice" window, the "Install" button is enabled. Click on the "Install" button to proceed to the "Destination Directory Selection" window

When the installation is complete the "Installation completed" message is displayed. Click on "OK" button to proceed to the last window.

Figure 1. PCT Installation License Agreement Window

SINSTALLER: Clock Tree Tool vX.X for معتبد المعتبي الم	
To install Clock Tree Tool vX.X for xxxx ESx.x Device you must accept all the conditions of this License Agreement OR have signed an SLA with TI	
License Agreement	<u> </u>
DO NOT CLICK "I AGREE" UNLESS 1. YOU ARE AUTHORIZED TO AGRE THE TERMS OF THIS LICENSE OF BEHALF OF YOURSELF AND Y COMPANY; AND 2) YOU INTEND TO ENTER THIS LEGALLY BIN AGREEMENT ON BEHALF OF YOURSELF AND YOUR COMPANY. Important - Read carefully: THIS LICENSE AGREEMENT IS A L AGREEMENT ("AGREEMENT") BETWEEN YOU (EITHER AN INDIVIDUA ENTITY) AND TEXAS INSTRUMENTS INCORPORATED ("TI"). THE "LICE MATERIALS" SUBJECT TO THIS AGREEMENT INCLUDE THE SOFTA PROGRAMS TI HAS GRANTED YOU ACCESS TO DOWNLOAD AND ANY LINE" OR ELECTRONIC DOCUMENTATION ASSOCIATED WITH T PROGRAMS, OR ANY PORTION THEREOF, AS WELL AS ANY UPDATE UPGRADES TO SUCH SOFTWARE PROGRAMS AND DOCUMENTATIO ANY, OR ANY PORTION THEREOF, PROVIDED TO YOU AT TI'S	YOUR IDING IL OR NSED WARE Y "ON- HESE S OR DN, IF
I accept all the conditions of this license agreement	
I do not accept the conditions of this license agreement	
C An SLA has been signed with Texas Instruments	
< <u>Back</u> <u>N</u> ext> <u>Cancel</u> <u>Install</u>	

1.2 PCT running when multiple versions of JRE are installed (Under MS-WINDOWS)

WARNING

JRE version 1.7 or higher is required. The default JavaTM update should install version 1.7 or higher by default. If not, please refer to the JavaTM update web page for downloading the 1.7 or higher version. Then verify the installation by checking the version from the command line (type *java -version*; Message such as the following should appear: Java(TM) SE Runtime Environment (build 1.7.0_11-b21)).

2 PCT Overview

The Pad Configuration Tool (PCT) is a Java[™] based stand-alone application. It is an interactive pad configuration software for the device. It allows the user to:

- visualize the device pad multiplexing and additional functionality
- □ interact with the pad elements and view the effect on the Control Module registers
- □ interact with the Control Module registers and view the effect on the device pad configuration
- view a trace of all the device registers affected by the user interaction with pad configuration
- extract padconf register C header and register dumps for Code Composer Studio and Lauterbach.
- optimize configuration based pad configuration register settings vs. the outside device (PCB layout) settings.
- schematics review a given configurations and automatically detect inconsistency between board design and pad configuration.
- □ configure existing virtual and/or manual required timing and switching characteristics.
- □ configure IOSETs and cross check configuration for errors and warnings.

The advantage of the tool is that the user can visualize the device pad configuration state on power-on reset and then customize the configuration of the pads for the specific use-case and identify the device register settings associated to that configuration.

Being an interactive visual tool, the PCT gives the user a global view of the device pad architecture and allows determining the exact register settings to obtain the specific configuration.

3 PCT System and Running Requirements

- □ Java[™] JRE v 1.7 or higher (Can be downloaded from http://www.oracle.com/technetwork/java/index.html).
- □ Microsoft Windows7©) or later. Ubuntu 12.04 or later. Mac OSX Yosemite or later.
- □ The ideal screen resolution is 1440x900 or higher.
- Derived Processor: 1 gigahertz (GHz) or faster
- □ RAM: 1 gigabyte (GB) or more
- Hard disk space: 100 MB or more
 Bup the tool by:

Run the tool by:

- 1. Unzip the project zipped folder. (NOTE: Do not change the name of the unzipped folder, e.g., PCT-XXXX)
- 2. Double-click on the PCT-[version].jar file. If you are using a console, navigate to the installation folder and run the tool by typing *java -jar* PCT-[version].jar



4 PCT Start-up and View Refresh Timing

NOTE: The performance data given below is for the test machine used with Intel® Core ™ i3 @ 3.3GHz with 8 GB of RAM.

The PCT starts with the window shown in Figure 2. There are options for the user to select the desired Device Package and Silicon Revision.

XXXXXx Devices Pad Configuration Tool (PCT)	
XXXXXx Devices Pad Configuration Tool (PC	:т)
Select Device Package and Silicon Revision:	Select
TI Confidential – NDA Restrictions	
👋 Texas Ins	STRUMENTS

Figure 2. PCT Start Window

The start-up sequence of the PCT consists of reading an entire pad associated description database files. This would normally take about 10 to 20 seconds.

Similarly, the View Refresh function that updates the main view, covers all software functional pad of the device and takes as well about 10 to 20 seconds.

NOTE: In same cases, due to OS platform dependency, the PCT may not display correctly. In this case, a simple "View>Refresh Main view" from the drop-down menu will fix the coordination of the main view window.



5 PCT Graphical User Interface Description

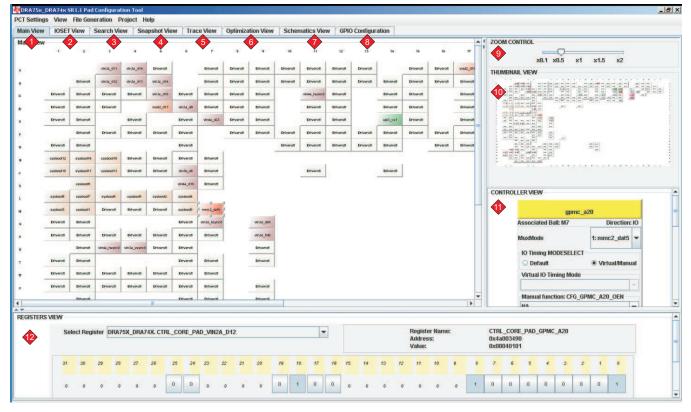


Figure 3. PCT Views

The PCT GUI is composed of a dozen sub-views which give the user different leverages for optimizing their work. The existing views are as follow :

- 1. Main View
- 2. IOSET View
- 3. Search View
- 4. Snapshot View
- 5. Trace View
- 6. Optimization View
- 7. Schematics View
- 8. GPIO View
- 9. Zoom Control
- 10. Thumbnail View
- 11. Controller View
- 12. Registers View

5.1 PCT Main View

The Main View presents a focused view of a section of the device pad configuration.

lain View	IOSET View	Search View	Snapshot View	Trace View	Optimizatio	III AIGAA	Schematics 1	AIGM	GPIO Configu	auun		
			vinsa_u++	vinsa_uro	priveron		DUAG	er on	onveron	briveron	briveron	DITY
3		Driveroff	vin3a_d12	vin3a_d13	vin3a_d14		Drive	eroff	Driveroff	Driveroff	Driveroff	Drive
	Driveroff	Driveroff	Driveroff	Driveroff	vin3a_d10	Driver	off Drive	eroff	Driveroff	Driveroff		vin4a_l
1	Driveroff	Driveroff	Driveroff		vout2_d11	vin3a_	_d9 Drive	eroff	Driveroff	Driveroff		Drive
	Driveroff	Driveroff		Driveroff		Driver	off vin4a	_d23	Driveroff	Driveroff		Drive
8		Driveroff	Driveroff	Driveroff	Driveroff	Driver	off		Driveroff	Driveroff	Driveroff	Drive
9	Driveroff	Driveroff				Driver	off				Driveroff	Drive
	sysboot12	sysboot14	sysboot15	Driveroff	Driveroff	Driver	off Drive	eroff				
6	sysboot10	sysboot11	sysboot13	Driveroff	Driveroff	vin3b_	_d6 Drive	eroff				Drive
< .		sysboot9				vin4a_	d15 Drive	erott				
Ú.	sysboot8	sysboot7	sysboot6	sysboot5	sysboot2	sysboo	nt4		2			
M	sysboot3	sysboot1	Driveroff	Driveroff	Driveroff	sysboo	ot0 mmc2_	_dat5				
4	Driveroff	Driveroff				Driver	off vin3a_t	nsyncü		vin3a_de0		
	Driveroff	Driveroff	Driveroff	Driveroff	Driveroff	Driver	off Drive	eroff		vin3a_fld0		

Figure 4. PCT Main View

The device pad configuration is represented as an XY coordinate system of pads (i.e., the rectangular elements).

The user can use the slide bars or drag with the mouse cursor on the view to move about. The view highlights the state of the blocks and their current configuration visually. For example, the mux mode of the pads is color coded. User will notice that for all pads that are set in muxmode 15 (driver off) the colors stay the same.

5.2 PCT IOSET View

An IO signal may have multiplexing options across two or more device pads. In many cases, the user is allowed to select any combination of IO signal multiplexing options to use for an interface. But in some cases, specific combinations of multiplexing options must be selected to guarantee the Timing and Switching Characteristics in the Data Manual. These specific combinations are called IOSETs, and they generally represent layout-friendly groups of pads that are pinned-out in close proximity to each other. IOSETs are defined in the Data Manual for interfaces that require them.

This view is created from and aligned with device Data Manual. Therefore the user will see the groups of IOSETs when selecting the desired module.



Figure 5. PCT IOSET View

Main View IOSET View Search View	Snapshot View Trace View	Optimization View	Schematics Vie	ew GPIO	Configura	ation				
A COMPANY AND A COMPANY	IO Set configuration	1940				0		2082.00.00		
Available Peripherals		IOSE	r1		IOSET2			IOSET3		
RMII mdio			vin4a_d0	R6	-	✓ vin4a_d0	B7	vin4a_d0	B14	
miiO			vin4a_d1	T9	1	✓ vin4a_d1	88	vin4a_d1	J14	
mii1			vin4a_d2	TG	-	✓ vin4a_d2	A7	vin4a_d2	G13	
rgmii0			vin4a_d3	17	1	₩ vin4a_d3	AB	vin4a_d3	J11	
rgmii1 rmii0			vin4a_d4	P6	-	⊮ vin4a_d4	C9	vin4a_d4	E12	
rmii1			vin4a_d5	R9	1	₩ vin4a_d5	A9	vin4a_d5	F13	
spi3			vin4a d6	R5		⊮ vin4a d6	B 9	and the second sec	C12	
spi4 usb3			vin4a_d7	P5		✓ vin4a_d7	A10	vin4a_d7	D12	
usb4			vin4a_d8	U2		₽ vin4a_d8	E8	vin4a_d8	E15	
vin2a			vin4a d9	UI		₽ vin4a d9	D9	vin4a d9	A20	
vin2b			vin4a_da	P3		vin4a_d11	D8	vin4a_d10	B15	
vin3a vin3b			vin4a_d11	R2		vin4a_d12	AS	vin4a_d11	A15	
vin4a			Contraction - Contraction	K7		and the second second			D15	
vin4b			vin4a_d12			✓ vin4a_d13	C6	vin4a_d12		
vout2 vout3			vin4a_d13	M7		✓ vin4a_d14	C8	vin4a_d13	B16	
voucs			vin4a_d14	J5		✓ vin4a_d15	C7	vin4a_d14	B17	
			vin4a_d15	K6		✓ vin4a_d16	F11		A17	
			vin4a_hsync			✓ vin4a_d17	G10		C18	
			vin4a_hsync		-	✓ vin4a_d18	F10	vin4a_d17	A21	
			vin4a_de0	H6	-	✓ vin4a_d19	G11	vin4a_d19	D17	
			vin4a_de0	P7	-	✓ vin4a_d20	E9	vin4a_d20	AA3	
			vin4a_fld0	P9	~	✓ vin4a_d21	F9	vin4a_d21	AB9	
			vin4a_fld0	J7	-	✓ vin4a_d22	FB	vin4a_d22	AB3	
			vin4a_clk0	P4	1	⊭ vin4a_d23	E7	vin4a_d23	AA4	
			vin4a_vsync	:0 T2	1	✓ vin4a_hsync	0 C11	vin4a_hsync0	E21	
					-	✓ vin4a_vsync	0 E11	vin4a_vsync0	F20	
					1	₽ vin4a_de0	B10	vin4a_de0	C23	
					~	⊭ vin4a_fld0	D11	vin4a_fld0	F21	
					-	✓ vin4a_clk0	B11	vin4a_clk0	B26	
					1	✓ vin4a_d10	D7	vin4a_d18	G16	

This view and in fact all views are in synch with register configuration. Therefore, user can either click the check boxes to configure the desired signals IOSET, read in register configuration, or use another view and configure register there. Either way, changes will be propelled here as seen in the above screenshot. Besides the general visual easiness of seeing and configuring IOSETS with a simple click, the view provides some helpful errors and warnings based on particular hardware requirements. One of these requirements, is that only a single IOSET must be used at a time per peripheral. If not the tool will display an error as shown below

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Figure 6. PCT IOSET View

lain View IOSET View	Search View	Snapshot View	Trace View	Optimization Viet	w Schematics	s View	GPIO Configuration			
	10 Se	t configuration								
Available Peripherals				IOSET	1		IOSET2		IOSET3	
RMII					vin4a_d0	R6	✓ ✓ vin4a_d0	87	vin4a_d0	B14
miiO					vin4a_d1	Т9	🖌 🗹 vin4a_d1	88	vin4a_d1	J14
mii1					vin4a_d2	T6	✓ ✓ vin4a_d2	A7	vin4a_d2	G13
rgmiiO					vin4a_d3	17	✓ ✓ vin4a_d3	AB	vin4a_d3	J11
rgmii1 rmii0					vin4a_d4	P6	✓ ✓ vin4a_d4	C9	vin4a_d4	E12
rmii1					vin4a_d5	R9	✓ ☑ vin4a_d5	A9	vin4a_d5	F13
spi3					vin4a_d6	R5	✓ ☑ vin4a_d6	B 9	vin4a_d6	C12
spi4 usb3					vin4a_d7	P5	✓ ☑ vin4a_d7	A10	vin4a_d7	D12
usb4					vin4a_d8	U2	vin4a_d8	E8	🗶 🗹 vin4a_d8	E15
vin2a					vin4a d9	U1	vin4a d9	D9	🗙 🔽 vin4a d9	A20
vin2b vin3a					vin4a_d10	P3	✓ ✓ vin4a_d11	D8	vin4a d10	815
vin3b					vin4a d11	R2	🖌 🖌 vin4a_d12	A5	vin4a_d11	A15
vin4a					vin4a_d12	K7	🖌 🖌 vin4a d13	C6	vin4a d12	D15
vin4b vout2					vin4a_d13	M7	✓ ✓ vin4a_d14	C8	vin4a_d13	B16
vout3					vin4a d14	J5	✓ ✓ vin4a_d15	C7	vin4a d14	B17
					vin4a d15	KG	✓ ✓ vin4a d16	F11	vin4a d15	A17
					vin4a_hsyne		✓ ✓ vin4a_d17	G10	vin4a_d16	C18
					vin4a hsyn		✓ ✓ vin4a d18	F10	vin4a_d17	A21
					vin4a_de0	H6	✓ ✓ vin4a_d19	G11	vin4a_d19	D17
					vin4a_de0	P7	✓ inita_d20	E9	vin4a_d20	AA3
					vin4a_dd0	Pg	✓ vin4a_d21	F9	vin4a_d21	AB9
					vin4a_fid0	J7	 ✓ in4a_d21 ✓ vin4a_d22 	FB	vin4a_d22	AB3
					vin4a_clk0	P4	✓ vin4a_d22	E7	vin4a_d23	AA4
					vin4a_ciku		✓ ✓ vin4a_u23		vin4a_hsync	
					Villed_voyin	10 12	✓ ✓ vin4a_vsyn		vin4a_vsync	
							1	B10	vin4a_de0	C23
							✓ ✓ vin4a_de0 ✓ ✓ vin4a_fld0	D11	vin4a_de0	F21
							✓ ✓ vin4a_nuo	B11	vin4a_nuu	B26
							✓ vin4a_ciku	D7	vin4a_cito	G16

For details on the error itself, the user can simply hover the error icon with the mouse

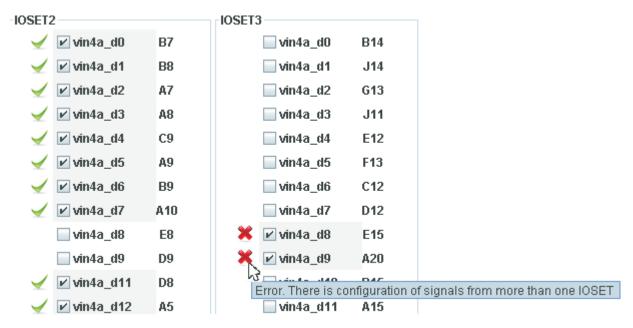


Figure 7. PCT IOSET Error cross-check

Another typical error would be when same signal is set on 2 different balls in two different IOSETs



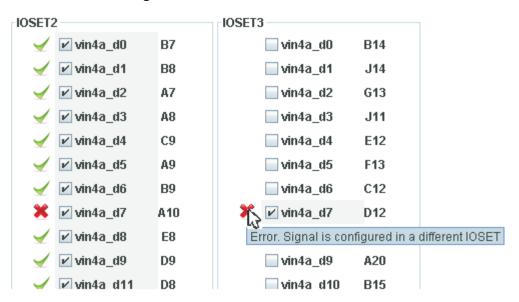


Figure 8. PCT IOSET Error cross-check 2

On some occasions, same signal(in same mux mode) on same ball is included in 2 or more IOSETs. This time the tool assumes these signals/balls as shared and does not display an error as shown in the following example:



Figure 9. PCT IOSET Error cross-check 3

Lastly, the tool will show caution next to an available but not configured signal if the ball is already used in another IOSET. In this case, the user is notified not to configure the ball since it has been used in another configuration.



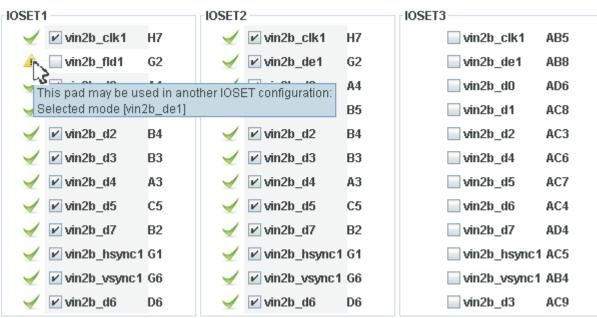


Figure 10. PCT IOSET Warning/Caution message

Limitation: Note that, as stated in the beginning of this subsection, all views are in synch across the entire tool. This means that views are being updated asynchronously when an action event has occurred. If pad is also associated to a different peripheral IOSET than the current selected, the view may refresh and show the IOSETs of the peripheral that has lastly updated the pad. If this occurs, a quick workaround for the user will be to reselect the needed peripheral from the left list menu.

5.3 PCT Search View

The Search view allows the user to navigate to the needed pad and pad controller. Simply by selecting the desired module associated to the pad the corresponding controller will be displayed.

	CONTROLLER VIEW
Modules	
usb1	vin2a clk0
usb2	Associated Ball: E1 Direction: IO
usb3	
usb4 vin1a	MuxMode 0: vin2a_clk0 💌
an ta ain 16	IO Timing MODESEI ECT
vina	to thing modeballest
99.69	O Default O Virtual/Manual
	Virtual IO Timing Mode
Signals	· · · · · · · · · · · · · · · · · · ·
vin2a_clk0	Manual IO Timing Mode: CFG_VIN2A_CLK0
vin2a_d0	MA VA
vin2a_d1	
vin2a_d10	Enable Pull
vin2a_d11	
vin2a_d12	Pull Type
vin2a_d13	Pull-Up Pull-Down
	Enable Input
Pads	/ / / / / / / / / / / / / / / /
mdio_mclk	Enable Wakeup
vin2a_clk0	
	Slew Control
	Fast Slow

Figure 11. PCT Search View



PCT Graphical User Interface Description

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5.4 PCT Snapshot View

The Snapshot view allows the user to see a clear list of all device pads, their padconf register address, value, selected muxmode, and driveroff availability. This view is dynamically refreshed and all changed done in other views are also present here.

Main View	IOSET View	Search View	Snapshot View	Trace View	Optimization View	Schematics View	GPIO Configura	uon		
Registers S	napshot								1	CONTROLLER VIEW
	PAD		ADDRESS		VALUE	SELEC	TED MODE	Driver off AVAILABL	E	Normal T 1992 Across a
gpmc_ad0		0x4A0034	100	0x5000F		sysboot0			-	gpmc ad0
gpmc_ad1	-	0x4A0034	104	0x5000F		sysboot1				
gpmc_ad2		0x4A0034	108	0x5000F		sysboot2			_	Associated Ball: M6 Direction: IO
gpmc_ad3		0x4A0034	10C	0x5000F		sysboot3				
pmc_ad4		0x4A0034	10	0x5000F		sysboot4			_	MuxMode 15: sysboot0 💌
pmc_ad5		0x4A0034		0x5000F		sysboot5				
pmc_ad6		0x4A0034		0x5000F		sysboot6				IO Timing MODESELECT
gpmc_ad7		0x4A0034		0x5000F		sysboot7				Default Ovirtual/Manual
gpmc_ad8		0x4A0034		0x5000F		sysboot8				
pmc_ad9		0x4A0034		0x5000F		sysboot9				Virtual IO Timing Mode
gpmc_ad10		0x4A0034		0x5000F		sysboot10				-
gpmc_ad11		0x4A0034		0x5000F		sysboot11				
gpmc_ad12		0x4A0034		0x5000F		sysboot12				Enable Pull
gpmc_ad13		0x4A0034		0x5000F		sysboot13				Enable Pull
gpmc_ad14		0x4A0034		0x5000F		sysboot14				Pull Type
gpmc_ad15		0x4A0034		0x5000F		sysboot15				
gpmc_a0		0x4A0034		0x4000F		Driveroff		v		O Pull-Up Pull-Down
pmc_a1		0x4A0034		0x4000F		Driveroff		2		
gpmc_a2		0x4A0034		0x4000F		Driveroff		v		Enable Input
gpmc_a3		0x4A0034		0x4000F		Driveroff		v		
gpmc_a4		0x4A0034		0x4000F		Driveroff		v		
gpmc_a5		0x4A0034		0x4000F		Driveroff		v		Enable Wakeup
gpmc_a6		0x4A0034		0x4000F		Driveroff		v		
gpmc_a7		0x4A0034		0x4000F		Driveroff		v		Slew Control
gpmc_a8		0x4A0034		0x4000F		Driveroff		×		
gpmc_a9		0x4A0034		0x4000F		Driveroff		×		Fast Slow
gpmc_a10		0x4A0034		0x4000F		Driveroff		×		
gpmc_a11		0x4A0034		0x4000F		Driveroff		×		
gpmc_a12		0x4A0034		0x4000F		Driveroff		×		
gpmc_a13		0x4A0034		0x4000F		Driveroff		×		
gpmc_a14		0x4A0034		0x4000F		Driveroff		×		
gpmc_a15		0x4A0034		0x4000F		Driveroff		×		
anme a16		0v44003/	IRN	0v4000E		Driveroff				

Figure 12. PCT Snapshot View

5.5 PCT Trace View

The Trace View is composed of a multi-column table. The successive changes of the register bitfields as a result of the user interaction with the pad (via the Controller View, Register View, or other user interactions such as readin configuration) are recorded in the rows of the Trace View table.

This view allows the user to find a trace of all the register bitfields affected and the values associated to these bitfields, as a result of the current interactions. Also, for step-by-step debug configuration, there is a "View -> Reset Trace View" command from the top menu which will clear the log table and start recording new events.

View	set Trace View	ı View	Snapshot View	Trace View	Optimization View	Schematics View	GPIO Configuration		
Ref	resh Main View								
EVENT			REGISTER			BITFIELD	1	ALUE	DESCRIPTION
	CTRL_COR	E PAD V	IN2A FLD0		[3:0] VIN2A_FLD0_M	UXMODE	0x2		
	CTRL_COR				[3:0] VIN2A_DE0_MU		0x3		
	CTRL_COR				[3:0] VIN2A_D23_MU		0x2		
	CTRL COR				[3:0] VIN2A D22 MU		0x2		
	CTRL CORE PAD VIN2A D21				[3:0] VIN2A D21 MU		0x2		
	CTRL COR				[3:0] VIN2A D20 MU		0x2		
	CTRL COR				[3:0] VIN2A D19 MU		0x2		
	CTRL COR				[3:0] VIN2A D18 MU		0x2		
	CTRL COR				[3:0] VIN2A D16 MU		0x2		
			IN2A HSYNCO		[3:0] VIN2A HSYNCI		0x3		
			IN2A_VSYNC0		[3:0] VIN2A_VSYNCO		0x3		
	CTRL COR				[3:0] VIN2A_D17_MU		0x2		
	CTRL COR				[3:0] RGMII0 TXD1		0x6		
			GMIIO TXDO		[3:0] RGMII0 TXD0		0x6		
	CTRL COR	RE PAD RGMIIO RXC			[3:0] RGMIIO RXC N	IUXMODE	0x6		
	CTRL COR	E PAD F	GMIIO RXCTL		[3:0] RGMII0 RXCTL	MUXMODE	0x6		
	CTRL COR	E PAD F	GMIIO RXD2		[3:0] RGMII0 RXD2	MUXMODE	0x6		
	CTRL COR	E PAD F	GMIIO RXD3		[3:0] RGMII0 RXD3	MUXMODE	0x6		
	CTRL COR	E PAD F	GMIIO RXD0		[3:0] RGMII0 RXD0	MUXMODE	0x6		
	CTRL COR	E PAD F	GMIIO TXCTL		[3:0] RGMII0 TXCTL	MUXMODE	0x6		
	CTRL COR	E PAD F	GMIIO TXC		[3:0] RGMII0 TXC M	UXMODE	0x6		
	CTRL COR	E PAD F	GMII0_TXD3		[3:0] RGMII0 TXD3	MUXMODE	0x6		
			GMII0 TXD2		[3:0] RGMII0 TXD2	MUXMODE	0x6		
	CTRL COR	E PAD F	GMIIO RXD1		[3:0] RGMII0 RXD1	MUXMODE	0x6		
	CTRL COR	E PAD C	PMC AD12		[8:8] GPMC AD12 N	IODESELECT	0x1		Selects between default and another IO delay different than the default one. This new IO delay
	CTRL COR	E PAD C	PMC AD13		[8:8] GPMC AD13 N	IODESELECT	0x1		Selects between default and another IO delay different than the default one. This new IO delay
	CTRL COR	E PAD V	IN2A VSYNCO		[8:8] VIN2A VSYNCO	MODESELECT	0x1		Selects between default and another IO delay different than the default one. This new IO delay
	CTRL COR	E PAD V	IN2A FLD0		[8:8] VIN2A FLD0 M	ODESELECT	0x1		Selects between default and another IO delay different than the default one. This new IO delay
	CTRL COR	E PAD V	IN2A DE0		[8:8] VIN2A DE0 MC	DESELECT	0x1		Selects between default and another IO delay different than the default one. This new IO delay
	CTRL COR	E PAD V	IN2A_HSYNC0		[8:8] VIN2A_HSYNCI	MODESELECT	0x1		Selects between default and another IO delay different than the default one. This new IO delay
	CTRL COR				[8:8] VIN2A D17 MC		0x1		Selects between default and another IO delay different than the default one. This new IO delay
	CTRL COR	E PAD V	IN2A D18		[8:8] VIN2A D18 MC	DESELECT	0x1		Selects between default and another IO delay different than the default one. This new IO delay
	CTRL_COR	E_PAD_V	IN2A_D21		[8:8] VIN2A_D21_MC	DESELECT	0x1		Selects between default and another IO delay different than the default one. This new IO delay
	CTRL_COR	E_PAD_V	IN2A_D22		[8:8] VIN2A_D22_MC	DESELECT	0x1		Selects between default and another IO delay different than the default one. This new IO delay
	CTRL_COR	E_PAD_V	IN2A_D20		[8:8] VIN2A_D20_MC	DESELECT	0x1		Selects between default and another IO delay different than the default one. This new IO delay
	CTRL_COR				[8:8] VIN2A_D16_MC	DESELECT	0x1		Selects between default and another IO delay different than the default one. This new IO delay
	CTRL_COR				[8:8] VIN2A_D19_MC	DESELECT	0x1		Selects between default and another IO delay different than the default one. This new IO delay
	CTRL_COR				[8:8] VIN2A_D19_MC		0x1		Selects between default and another IO delay different than the default one. This new IO delay
	CTRL COR				[8:8] VIN2A D23 MC	DESELECT	0x1		Selects between default and another IO delay different than the default one. This new IO delay

Figure 13. PCT Trace View

5.6 PCT Optimization View

The Optimization view gives the user the ability to verify pad configuration register settings vs. the outside device (PCB layout) needed configuration (that is configured from the Schematics View described later). When data is entered in the schematics view or register is updated, this view will automatically do the checks and will output errors or warnings if any. The logic will also try to scan additional patterns and try to find tips on how these errors may be fixed. The columns are as follow:

- □ Mux 0: This column contains the name of the signal for Mux 0. Mux 0 is also the name of the pad.
- □ Mode: This column contains the current configured mux mode from the main view or pad conf register.
- □ fn dir: This column checks the schematic configuration vs the pad configuration. If schematic vs register configuration IO direction does not match, an error will occur.
- □ IO type: This column contains the C variable for the current configuration.
- padconf Pull: This column contains information of the register configuration pull direction. It can be PU for pull-up or PD for pull-down.
- padconf OFF config: This column contains information of the register configuration OFF mode pullUD enabled.
- Schematics pull: This column contains information of the schematics configuration and whether the pull is present or not on the outside.
- padconf IO: This column contains information of the register configuration and whether the pad is configured as input(input is enabled) or only as an output.
- Schematics IO: This column contains information of the register configuration and whether the pad is configured as input(input bit is enabled) or only as an output.
- GPIO: This column gets updated automatically if the pad is register configured in GPIO mode and it is based on the input from the GPIO Configuration view. Values are in/0, in/1, out/0, and out/1.
- Pull Contention: This column gets updated automatically and it gives an error (contention) if pull configuration has an discrepancy between internal and schematic pulls. Again, this is based on the two configurations - register and schematic input.
- External Driver: This column gets updated automatically and it gives an error based on the two configurations - register and schematic input. See Figure 15

- Manual Status: This column gets updated when manual status is filled in the schematics view. The user can fill a comment "OK" or a comment "TBC" and the logic checks will be ignored and the result in the driver column will be OK or TBC depending on the entered comment.
- First Customer feedback: This column gets updated when comments are entered by the user in the "First customer feedback" column in the Schematics View. This feature can be used for tracking/commenting purposes. It means no value for the logical checks.
- □ TI Initial Comments: Same as "First Customer feedback"
- Additional Comments: Same as "First Customer feedback" and "TI Initial Comments"

CAUTION

Schematic and Register configuration are two different scopes which are matched to determine errors/warning if any. Register configuration is internal for the device, while the schematics is devices external configuration. Settings that are same for both (such as pull configuration) does not get updated for both register and schematic views. For example, if pull direction is configured from a register it does not get propagated to the schematics view, but rather used to match schematic configuration in order to give errors/warnings if mismatches are present.

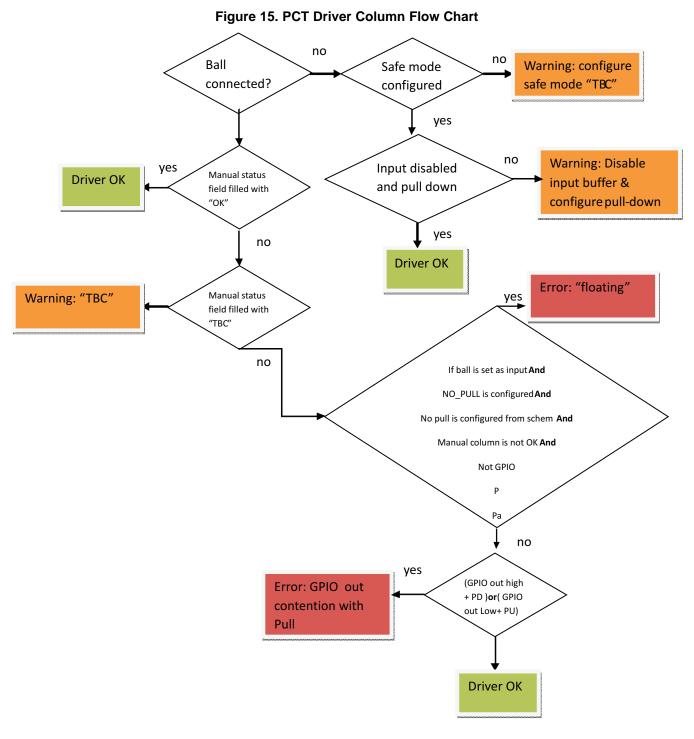
Figure 14 is read-only view and cannot be modified directly, but rather it will get updated when new register reconfiguration and/or schematics input is entered and verified for errors.

Main View	OSET View Search View	Snapshot View	Trace View	Optimiz	ation View	Schemat	tics View	GPIO Cor	nfiguratio	n						
Optimization vie	ew															
Mux O	Mode	fn IO Type dir		padconf Pull	padconf OFF	Schematic pull	padconf IO	schema tic IO	GPIO	Pull Contentior	External driver	Manual Status	First Customer feedback	TI Initial Comments	Additional Comments	
pmc_ad0	sysboot0	IO PIN_INPUT		NO_PULL	YES	N	in	10	NOT_G	NO OK	TBC					
pmc_ad1	sysboot1	IO PIN_INPUT		NO_PULL	YES	N	in	10	NOT_G	PIO OK	TBC					
pmc_ad2	sysboot2	IO PIN_INPUT		NO_PULL		N	in	10	NOT_G		TBC					
pmc_ad3	sysboot3	IO PIN_INPUT		NO_PULL			in	10	NOT_G		TBC					
pmc_ad4	sysboot4	IO PIN_INPUT		NO_PULL	YES	N	in	10	NOT_G		TBC					
pmc_ad5	sysboot5	IO PIN_INPUT		NO_PULL			in	10	NOT_G		TBC					
pmc_ad6	sysboot6	IO PIN_INPUT		NO_PULL			in	10	NOT_G		TBC					
pmc_ad7	sysboot7	IO PIN_INPUT		NO_PULL			in	10	NOT_G		TBC					
gpmc_ad8	sysboot8	IO PIN_INPUT		NO_PULL			in	10	NOT_G		TBC					
gpmc_ad9	sysboot9	IO PIN_INPUT		NO_PULL			in	10	NOT_G		TBC					
gpmc_ad10	sysboot10	IO PIN_INPUT		NO_PULL			in	10	NOT_G		TBC					
gpmc_ad11	sysboot11	IO PIN_INPUT		NO_PULL			in	10	NOT_G		TBC					
gpmc_ad12	sysboot12	IO PIN_INPUT		NO_PULL			in	10	NOT_G		TBC					
gpmc_ad13	sysboot13	IO PIN_INPUT		NO_PULL			in	10	NOT_G		TBC					
gpmc_ad14	sysboot14	IO PIN_INPUT		NO_PULL			in	10	NOT_G		TBC					
gpmc_ad15	sysboot15	IO PIN_INPUT		NO_PULL			in	10	NOT_G		TBC					
gpmc_a0	Driveroff	IO PIN_INPUT_I		PD			in	10	NOT_G		TBC					
gpmc_a1	Driveroff	IO PIN_INPUT_I		PD			in	10	NOT_G		TBC					
gpmc_a2	Driveroff	IO PIN_INPUT_I		PD			in	10	NOT_G		TBC					
pmc_a3	Driveroff	IO PIN_INPUT_I		PD			in	10	NOT_G		TBC					
gpmc_a4	Driveroff	IO PIN_INPUT_I		PD PD			in in	10	NOT_G		TBC TBC					
gpmc_a5	Driveroff Driveroff	IO PIN_INPUT_		PD			in	10	NOT_G		TBC					
gpmc_a6 gpmc_a7	Driveroff	IO PIN INPUT I		PD			in	10	NOT G		TBC					
gpmc_a/ gpmc_a8	Driveroff	IO PIN INPUT		PD			in	10	NOT G		TBC					
gpmc_a0	Driveroff	IO PIN INPUT I		PD			in	10	NOT G		TBC					
gpmc_as	Driveroff	IO PIN INPUT		PD			in	10	NOT_G		TBC					
	Delveron			00		N NI	in .	10	NOT_O		TDO					
Carl Warning: Carl Passed Carl Sourier Sourier	(557 Items) cc: (in/32_d15) Passed type: cc: (gpmc_ad3) Passed type: cc: (mcta_d1) Passed type: pc: (gmc_a5) Passed type: pc: (gpnc_a5) Passed type: pc: (gpnc_a13) Passed type: cc: (gpmc_a13) Passed type: cc: (gpmc_a15) Passed type:	direction, Descriptio direction, Descriptio all, Description: Inte e: pull, Description: Inte irection, Description pull, Description: Int direction, Descriptio	n: IO direction m: IO direction rnal pull config : Internal pull co rnal pull config n: IO direction C ternal pull config nn: IO direction	OK. ured, no ext onfigured, n jured, no ex OK. OK.	o external ternal pull	pull presente presented.	d.									
— 🗋 Sour	rce: [gpmc_an5] Passed type: rce: [vin1a_vsync0] Passed type: rce: [vout1_d17] Passed type:	e: direction, Descrip	ation: IO direction	on OK.												

Figure 14. PCT Optimization View

The following flow chart describes the logic behind showing errors/warnings.





5.7 PCT Schematics View

CAUTION

Schematic configuration is not stored/set into registers. Schematic configuration must be saved before exiting the tool and can be reloaded on the next run from Project>Save/Load Schematic View configuration menu. See Section 5.13.4

The Schematics view gives the user the ability to enter board design data and thus automatically detect of inconsistency between board design and pad configuration which is then displayed in the Optimization View. The columns are as follow:

- □ Ball ID: Contains the Ball ID coordinates
- Connected/not connected: User can state whether the ball is connected or not. If connected the tool proceeds and starts checking for errors/warnings. If not connected then the configuration is checked to make sure it is in a "safe" state. See Figure 15.
- □ MUXX0: Presents the mux 0 name for the pad. This field is read-only and is for reference purposes.
- □ Selected Mux: Shows the current configured mux mode from register setting. This field is read-only and is for reference purposes.
- □ External Pull on board: User can state whether an external pull is present on board.
- **L** External Pull Type: User can state the type of pull present on board.
- External Direction: User can state the direction needed.
- □ Off mode override needed: User can state whether an off mode is needed.
- □ Off mode override output en: User can state whether an off output is enabled.
- □ Off mode pull needed: User can state whether an off mode pull is needed.
- □ Off mode pull value: User can state the pull value in off mode.
- □ PadConf output: TBD in future versions of the tool.
- Manual status: This column can be filled by user to override the logical check of the tool. Valid comments are "OK" and "TBD". See Figure 15.
- First Customer feedback: This column gets updated when comments are entered by the user in the "First customer feedback" column in the Schematics View. This feature can be used for tracking/commenting purposes. It means no value for the logical checks.
- □ TI Initial Comments: Same as "First Customer feedback"
- Additional Comments: Same as "First Customer feedback" and "TI Initial Comments"

The following figure is for the sake of presenting the view, not be taken as an example configuration.

Main View	N IOSET	View Search	View Snapsho	t View Tr	ace View	Optimizat	ion View	Schemat	ics View	GPIO Con	figuratio	n				
Scheman	tic Review															
Ball ID	Connecte d/not connecte d?	MUXO	Selected Mux (from register config)	External Pull on board?	External Pull type	External Direction	offmode override needed?	offmode override, output en		offmode Pull Value	fOutput		First Customer Feedback	Initial comments from TI	Additional Comments	
46	C	gpmc_ad0	sysboot0	N	NA	10	N					OK	test comment 1	none	none	
M2	C	gpmc_ad1	sysboot1	N	NA	10	N	N	N	PD		OK	a second and a second second			
L5	C	gpmc_ad2	sysboot2	N	NA	ю	N					OK				
M1	C	gpmc_ad3	sysboot3	N	NA	10	N					OK	asd			
L6	C	gpmc_ad4	sysboot4	N	NA	10	N					TBC	test comment 2	none	none	
L4	C	gpmc_ad5	sysboot5	N	NA	10	N					TBC	The second second second second			
L3	C	gpmc_ad6	sysboot6	N	NA	10	N					TBC			1	
L2	C	gpmc_ad7	sysboot7	N	NA	10	N					TBC				
L1	C	gpmc_ad8	sysboot8	Y	NA	10	N					TBC				
K2	C	gpmc_ad9	sysboot9	Y	NA	10	N					TBC				
J1	C	gpmc_ad10	sysboot10	Y	NA	10	N	N	N	PD		TBC	test comment 3	none	none	
J2	C	gpmc_ad11	sysboot11	N	NA	10	N	1.12				20-80 (AD)	a second and a second sec			
H1	C	gpmc_ad12	sysboot12	N	NA	10	N									
J3	C	gpmc_ad13	sysboot13	N	NA	10	N									
H2	C	gpmc_ad14	sysboot14	N	NA	10	N								0	
H3	C	gpmc_ad15	sysboot15	N	NA	10	N									
R6	C	gpmc_a0	Driveroff	Y	NA	10	N					OK				
T9	C	gpmc_a1	Driveroff	Y	NA	10	N					OK				
T6	C	gpmc_a2	Driveroff	Y	NA	10	N					OK				
17	C	gpmc_a3	Driveroff	Y	NA	10	N					OK				
P6		gpmc_a4	Driveroff	N	NA	10	N									
		gpmc_a5	Driveroff	N	NA	10	NU									

Figure 16. PCT Schematics View

5.8 PCT GPIO Configuration View

This view enables the user to enter GPIO configuration for pads. The view consists of two tables. The left one is read-only with columns stating GPIO instance, name, bit number, whether output is enabled, and in/out values. The right column is filled by the user. For example "OE (register value)" column is filled with the GPIO instance register value. The valid inputs are 32bit hex strings (e.g. 0xFFFFFFF). Furthermore, when all information is entered, and if the pad is configured in GPIO mode, the tool starts cross checking and gives errors/warnings if any. See Figure 15.

The following figure is for the sake of presenting the view, not be taken as an example configuration.



PCT Graphical User Interface Description

Main View	IOSET View	Search View	Snapsho	t View T	race View	Optimization View	Schematics View	GPIO Configura	tion							
Instance	Name	Bit	oe	in/out	in value		summary	wake_0	wake 1	-	1 Instance	OE (register val	DATA_IN (register	DATA OUT		
GPIO1		0 1		in	1		n/1		N Narke_1	- L	GPI01		0xFFFFFFFF	DATA_001	INGRANCEN	INGWINKEN.
GPI01		1 1		in	1		in/1	•	0		GPI02	FFFFFFF	UXFFFFFFF			
GPI01		10 1		in	1		in/1		0	-11	GPI02 GPI03					
GPI01		11 1		in	1		in/1		0	-11	GPI04					
GPI01		12 1		in	1		in/1		0	-11	GPI05					
GPI01		13 1		in	1		in/1		0		GPI06					
GPI01		14 1		in	1		in/1		0	-111	GPI07					
GPI01		15 1		in	1		in/1	~	0	-11	GPI08					
GPIO1		16 1		in	1		in/1		0	-11	OT IOU					
GPI01		17 1		in	1		in/1		0	-Ш						
GPI01		18 1		in	1		in/1		0	-						
GPI01		19 1		in	1		in/1		0	-						
GPI01		2 1		in	1		in/1		0	-						
GPIO1		20 1		in	1		in/1		0	-						
GPIO1		21 1		in	1		in/1	0	0	-						
GPI01		22 1		in	1		n/1		0	-						
GPI01		23 1		in	1		n/1		0	-						
GPI01		24 1		in	1		n/1		0	-						
GPI01		25 1		in	1		n/1	0	0							
GPI01		26 1		in	1		n/1	0	0							
GPI01		27 1		in	1		in/1	0	0							
GPI01		28 1		in	1		in/1	0	0							
GPI01		29 1		in	1		in/1	0	0							
GPI01		3 1		in	1		in/1	0	0							
GPI01		30 1		in	1		in/1	0	0							
GPIO1		31 1		in	1	0	in/1	0	0							
GPIO1		4 1		in	1		in/1	0	0							
GPIO1		5 1		in	1	0	in/1	0	0							
GPI01		6 1		in	1		in/1	0	0							
3PI01		7 1		in	1	0	in/1	0	0							
GPI01		8 1		in	1	0	in/1	0	0							
GPI01		9 1		in	1	0	in/1	0	0							
GPIO2		0 0)	out	0	0	out/0	0	0							
GPIO2		1 0	1	out	0	0	out/0	0	0							
GPI02		10 0	1	out	0	0	out/0	0	0							
GPIO2	gpio2_11	11 0		out	0		out/0		0							
0100		10			-				-	_	2					

Figure 17. PCT GPIO Configuration View

5.9 PCT Zoom Control

The Zoom Control allows the user to change the zoom level of the Main View. By default the zoom level is set to x1. The user can zoom in by shifting the slider to the right hand side (towards x2) and zoom-out by shifting the slider to the left hand side (towards x0.1). The user can also use the mouse scroll wheel to zoom in/out.



COOM C	ONTROL			
x0.1	x0.5	×1	x1.5	x2

5.10 PCT Thumbnail View

The Thumbnail View highlights a global view of the device pad configuration. It also highlights the region of the tool visible in the Main View by a bounding rectangle. As the slide bars of the Main View are displaced the bounding rectangle in the Thumbnail View also moves accordingly.



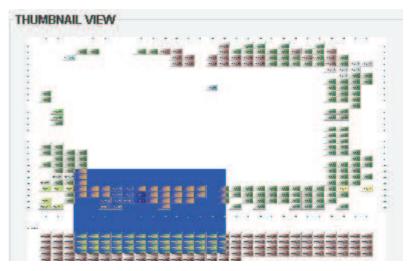


Figure 19. PCT Thumbnail View

5.11 PCT Controller View

The Controller View represent a menu of configurable options associated to pad's padconf and iodelay registers.. The user selects (i.e., clicks on) the block in the Main View and its corresponding controller is displayed.



Figure 20. PCT Controller View

CONTROLLER V	1EW		
	mmc1_da		
	Associated Ball: Y4	Direction:	: 10
	MuxMode	0: mmc1_dat1	-
	IO Timing MODESELECT		
	 Default 	Virtual/Manu	ial
	Virtual IO Timing Mode		
	10: MMC1_VIRTUAL2		•
	Manual function: CFG_MM		
	MMC1_DDR_MANUAL1	-	
	Manual function: CFG_MM		
	MMC1_DDR_MANUAL1		•
	Manual function: CFG_MM	IC1_DAT1_OEN	
	MMC1_DDR_MANUAL1		-
	Enable Pull		V
	Pull Type		
	ell-Up	🔾 Pull-Dov	vn
	Enable Input		~
	Enable Wakeup		~
	Slew Control		
	⊖ Fast	Slo	W

5.11.1 PCT Controller Fields Description

There are several available options for the user to configure the bitfields of a padconf register. Refer to device TRM Control Module chapter for functional description of the padconf bitfields. Moreover, the following list describes available controller options and their corresponding bitfields from top to bottom:

- MuxMode drop down menu [3:0] MUXMODE
- IO timing MODESELECT [8] MODESELECT, also see Section 5.11.2
- Virtual IO Timing Mode [7:4] DELAYMODE, also see Section 5.11.2
- Manual Function N/A, see Section 5.11.2
- Enable Pull [16] PULLUDENABLE
- Pull Type [17] PULLTYPESELECT
- Enable Input [18] ACTIVE or [18] INPUTENABLE
- Enable Wakeup [24] WAKEUPENABLE



• Slew Control - [19] SLEWCONTROL

NOTE: If a bitfield is not available for a given pad, its corresponding controller option is greyed out and not available for the user to click.

5.11.2 PCT Manual /Virtual Function Description

Some of the timings described in the device Data Manual section "Virtual and Manual IO Timing Modes" require the use of Virtual or Manual IO Timing Modes. See DM and TRM for detail description. The Pad Configuration Tool on its end, gives the user the ability to configure these timing modes.

First, the user needs to have the MODESELECT enabled for Virtual/Manual modes. If not configured, PCT will not display the available configuration menus.

When enabled, depending on whether there are available manual/virtual modes, tool will display virtual or manual drop down menu, or both.

Manual function

Manul function is a straight forward configuration. By selecting the mode name, its prefix value is the value that will be set into the [7:4] DELAYMODE padconf bitfield

Virtual function

Virtual configuration is a bit more complex that manual mode. Depending on available registers, there are up to 3 registers associated to a pad - IN, OUT, and OEN registers. Therefore, the controller will display up to 3 drop down menus. From there the user can select the desired manual mode.

CAUTION

Although there may be up to 3 different drop down menus for manual mode (each configuring the IN, OUT, or OEN register), the same mode must be selected for IN, OUT, and OEN. That is, the same mode name must be set in all 3 menus.

CAUTION

Unlike virtual mode, manual mode configuration is not directly written into registers when configured due to a chip specific variable which is not know by the PCT. User must save their configuration from the "Project -> Save manual IODELAY configuration" before exiting the tool, or their configuration will be lost. On the next run, user can do "Project -> Load manual IODELAY configuration" respectively to upload their old or somebody else's configuration. See Section 5.13.4

5.11.3 PCT Pad Block

NOTE: For detail description on Control Module, pads, and I/O cell logical functionality, refer to the device Technical Reference Manual (TRM)

NOTE: For detail description on electrical characteristics and I/O cell performance, refer to the device Data Manual (DM)

The PCT pad block is mainly composed of the associated pad conf register and additional control module registers. In the PCT there are various combinations of registers associated to a pad (pad conf register and additional functionalities). These types of pads are split into classes in the pad conf tool. For detail description of the different functional pad classes refer to device TRM chapter Control Module.

Driveroff	Driveroff	Driveroff	/ mmc1	dat1
Driveroff	Driveroff	Driveroff	Associated Ball: Y4	Direction
			MuxMode	0: mmc1_dat1
Driveroff	mmc1_dat1		IO Timing MODESELEC	Virtual/Manu
Driveroff	Driveroff	Driveroff	10: MMC1_VIRTUAL2 Manual function: CFG_I	
Driveroff	Driveroff	Driveroff	MMC1_DDR_MANUAL1 Manual function: CFG_I MMC1_DDR_MANUAL1	MMC1_DAT1_IN
Driveroff	Driveroff	Driveroff		

Figure 21. PCT Pad Block

5.12 PCT Registers View

The Registers View is composed of a Register Selector list box, on the left hand side. The name of the currently selected register is highlighted in this box.

On the upper right hand side of the Register View is the Register Address/Value indicator. It presents the address and the current hexadecimal value of the register.

Below these two is a Register Bits view. The register bits view lists all the bits of the selected register (e.g., 0 to 31 bits for a 32 bits register of the Control Module). Each bit is identified by the bit number (0 for the LSB). Below the bit number is the current value of the bit (1/0).

A toggle button below the bit number of the user configurable (i.e. read/write) bits allows the user to toggle the bit value. Pressing the button sets the bit value to 1 and in the released state the bit value is 0.

There is no button associated to the RESERVED bits of the register (i.e., the user cannot modify the states of these bits).

When the user selects a register in the Register Selector list box, its contents (i.e., bits and value) are shown in the Register Bits view and the Register Value indicator.

When the user changes a parameter of a block in the Controller View, the associated bitfield is updated in the register and the Register View highlights the affected register.

When the value of a bit/ bitfield of a register changes in the register view, the Trace view captures this change also.

NOTE: When the user changes a parameter of a block which affects bitfields of more than one register, the Registers View only shows the last register updated. The Trace view shows the complete list of registers affected by this change.



Figure 22. PCT Register View

Select Register DRA75X_DRA74X. CTRL_CORE_PAD_VIN1A_D3											-					Regist Addre Value:	ss:	1e:		0x4a	CORE 003500 040104	0	_VIN1A	_D3							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	o
0	0	0	0	0	0	0	0	0	0	0	0	0	1	ο	0	0	o	0	0	0	0	0	1	0	0	0	0	0	1	0	0

When user positions the pointer on the number of a register bit a pop-up displays the name of that bit.

Figure 23. PCT Register View Pop-up CTRL_CORE_PAD_VIN1A_D3 0x4a003500



5.13 PCT Menu Commands Description

The PCT menu has following commands:

Figure 24. PCT Menu

PCT Settings	View	File Ge	eneration	Proje	ct Help
Main View	IOSET	View	Search	View	Snapshot Vie

1. PCT Settings

(a) Power-on Reset

- 2. View
 - (a) Reset Trace View
 - (b) Refresh Main View
- 3. File Generation
 - (a) C Header
 - (b) C Header (XLoader)
 - (c) Android Conf Macro
 - (d) Pad Conf Macro (modified pads only)
 - (e) Pad Conf Macro (all pads)
 - (f) Syscfg.h (Device Sys config header)
 - (g) Bios C header manual mode IODELAY config
 - (h) Generic file format Modified PADCONF only registers
 - (i) Generic file format ALL PADCONF registers
 - (j) Generic file format Only Modified manual IODELAY values
 - (k) Generic file format ALL manual IODELAY values
 - (I) Pads Listing



PCT Graphical User Interface Description

- 4. Project
 - (a) Save Registers
 - (b) Load Registers
 - (c) Save manual IODELAY configuration
 - (d) Load manual IODELAY configuration
 - (e) Save Schematic View configuration
 - (f) Load Schematic View configuration
- 5. Help
 - (a) About PadConf Tool
 - (b) User Manual
 - (c) Licence Agreement
 - (d) Export Control Notice

5.13.1 PCT Settings

1. Power-on Reset

Triggers a power-on reset for all the registers of the Control Module. All the registers are set to their reset values. As a result, the state of the pads is updated and reflects the state after power-on reset. (Note: When the PCT starts, the power-on reset is automatically triggered. Hence, the initial pad state is that of the device after power-on reset).

5.13.2 PCT Trace

1. Reset Trace View

Resets (clears) the Trace View table.

2. Refresh Main View

This command refreshes the Main View representation of the pad configuration tool. It is used if the pad representation is visually positioned sketchy, not aligned to a grid, etc. and the view needs to be refreshed.

5.13.3 PCT File Generation

The File Generation menu gives the user options to export all sorts of file formats, thus helping them to create a quick data files to be used in their code or for reference.

1. C Header This menu allows to export the settings set in the PCT in a C header file. For details of the C header functionality, refer to the comments in an exported C header file from the PCT.

2. C Header (XLoader) This menu allows to export the settings set in the PCT in a C header file XLoader format.

3. Android Conf Macro This menu allows to export the settings set in the PCT in a C header android configuration file format.

4. Pad Conf Macro (modified pads only) This menu allows to export macro definition used by software for only modified pads. Refer to inside file comments for details.

5. Pad Conf Macro (all registers) This menu allows to export macro definition used by software for all pads within the PCT. Refer to inside file comments for details.

6. Syscfg.h (Device Sys config header) This menu allows to export a device level system configuration header file (compatible with L2 software teams environment and test cases.)

7. Bios C header manual mode IODELAY config This menu allows to export a BIOS C header file for configured manual mode IODELAY A/G delay values.

8. Generic file format - Modified PADCONF only registers This menu allows to export a generic C header file for configured only padconf registers. Refer to inside file comments for details.

9. Generic file format - ALL PADCONF registers This menu allows to export a generic C header file for all padconf registers. Refer to inside file comments for details.

10. Generic file format - Only Modified manual IODELAY values This menu allows to export a generic C header file for only configured manual mode IODELAY A/G delay values. Refer to inside file comments for details.

11. Generic file format - ALL manual IODELAY values This menu allows to export a generic C header file for all IODELAY A/G delay values. Refer to inside file comments for details.

12. Pads Listing: This menu allows to export the list of pads with the associated padconf registers and settings in a given xml format.

5.13.4 PCT Project

Save Registers This menu allows to save the PCT register configuration to a file, in order the user to be able to reload it on next run. The tool can save two different file formats as given below.
 Save Format: ADD DATA. This menu selection allows to write to file in format where each line consists of two hex values as given below : ADDRESS_OF_REGISTER DATA_VALUE_OF_REGISTER
 Save Format: [ADD] DATA. This menu selection allows to write to file in format where each line consists of two hex values as given below : [ADDRESS_OF_REGISTER] DATA_VALUE_OF_REGISTER

NOTE: The ADD DATA format is saved to / read from file with .rd1 (register dump1) extension.

The [ADD] DATA format is saved to / read from file with .rd2 (register dump2) extension.

2. Load Registers This menu allow to load register setting from a file in order to set registers in the PCT. The tool can load two different file formats as given below.

2.1 Load Format: ADD DATA. This menu selection allows to load a file in which each line consists of two hex values in following format : ADDRESS_OF_REGISTER DATA_VALUE_OF_REGISTER
2.2 Load Format: [ADD] DATA. This menu selection allows to load a file in which each line consists of two hex values in following format :[ADDRESS_OF_REGISTER] DATA_VALUE_OF_REGISTER

In case of mismatch between the Device Packages or Silicon Revisions of the PCT settings and the loaded Registers the warning window shown in Figure 25 appears.

Figure 25. PCT Mismatch Warning Window



NOTE: The Register Load may be used to read-in the registers dump file generated by the Register Dump script (GEL in Code Composer Studio or CMM in Lauterbach) or by any function respecting the format described below. This allows to read the current state of the pad conf at any break-point in the code and obtain a visual representation of its state in the PCT. A gel and a cmm files can be found in *<PCT-Install-path>/Scripts/*

3. Save Manual IODELAY configuration: This option allows the user to save their IODELAY manual mode current configuration.

4. Load Manual IODELAY configuration: This option allows the user to load an IODELAY manual mode configuration.

5. Save Schematic View configuration: This option allows the user to save their configuration entered from the Schematics view.

6. Load Schematic View configuration: This option allows the user to load their configuration into the Schematics view.

5.13.5 PCT Help

1. About PadConf Tool: This option highlights the tool, model and view versions.

2. User Manual: This option opens the user manual document. (For Linux users, navigate to the "Docs" folder and open document with appropriate application manually.)

3. Licence Agreement: This option displays the licence agreement window.



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4. Export Control Notice: This option displays the export control notice window.

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