

1 2 3 4 5 6

A A

B B

C C

D D

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric	FR-4	59.20mil	4.8	
5	Bottom Layer	Copper	1.40mil		
6	Bottom Solder	Solder Resist	0.40mil	3.5	
7	Bottom Overlay				

Symbol	Quantity	Finished Hole Size	Plated	Hole Type
○	5	5.91mil (0.150mm)	PTH	Round
▽	3	14.00mil (0.356mm)	PTH	Round
✕	7	37.99mil (0.965mm)	PTH	Round
⊙	1	38.00mil (0.965mm)	PTH	Round
	16 Total			

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24 MIL
 MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER _____
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER _____
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/- _____

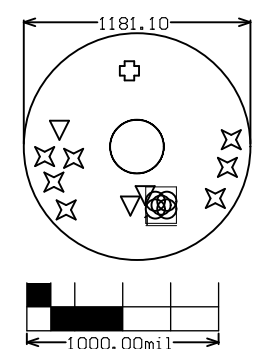
DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH MIN COPPER THICKNESS: 1MIL OTHER _____

BOARD FINISH:
 SILKSCREEN: TOP BOTTOM
 SILKSCREEN COLOR: WHITE OTHER _____
 SOLDER RESIST COLOR: GREEN BLUE OTHER _____
 SURFACE FINISH: IMMERSION GOLD (ENIG) ENEPIG
 IMM. TIN/SILVER OR EQUIV OTHER _____

ARRAY/PANEL: CUT AND TRIM PER MECH LAYER 1
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 UL 94V-0 RoHS OTHER PER ORDER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 MANUFACTURER'S UL: RAIL METAL SILK



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00578	REV: rev001	SUN REV: Not In VersionControl	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.	ENGINEER: Vish Nadarajah	LAYOUT BY: Vish Nadarajah
LAYER NAME = 000578.dwg	TID #: 00578				SCALE: 1.00	ALTIM DESIGNER VERSION: 14.3.14.34663
PLOT NAME = Fabrication Drawing	GENERATED : 6/12/2015 2:11:21 PM	TEXAS INSTRUMENTS				

1 2 3 4 5 6

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