TI Designs Optimized Sensor Linearization for Thermocouple

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Design Overview

This TIDA-00468 reference design shows how to build an isolated, thermocouple-sensing front end with optimized power consumption for loop-powered applications. This design reduces the footprint caused by using the classic approach of a look-up table. The design also maintains the fast response time of the linear piecewise interpolation.

Design Resources

TIDA-00468	Tool Folder Containing Design Files
ADS1220	Product Folder
MSP430FR5949	Product Folder
REF5020	Product Folder
TPS71733	Product Folder
TI LaunchPad	Tools Folder



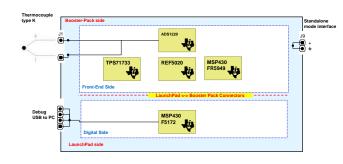
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Design Features

- Sensor Input: K-Type Thermocouple
- Temperature Range: -270°C to 1372°C
- Thermocouple Accuracy: ±0.02K
- Memory Footprint for Linearization: 320B
- BoosterPack Form Factor for Rapid Prototyping

Featured Applications

- Factory Automation and Process Control
- Sensors and Field Transmitters
- Building Automation
- Portable Instruments







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1 System Overview

1.1 Key System Constraints

Field transmitters are typically low-power systems, which is especially true for loop-powered field transmitters. Field transmitters are used to sense parameters such as pressure, temperature, flow, and so forth. They can sense a combination of many different parameters and transmit their values to a central point, such as a programmable logic controller (PLC), distributed control system (DCS), and so forth.

The low-power constraints of field transmitters often indicate that the frequency of the MCU is limited to a fraction of the maximum frequency at which the core can run (power scales linearly with frequency). This limitation can result in significant delays for complex computations.

This design provides an innovative way to keep the processing time to an absolute minimum while significantly reducing the footprint from classical look-up table approaches and maintaining the low-power aspects.

The goal of the TIDA-00468 design solves the following challenges that Table 1 proposes.

INDUSTRY CHALLENGE	TIDA-00468 SOLUTION
Fast reaction time	Faster than linear piecewise
Low footprint	Smaller than look-up tables, polynomial, and splines
Low power	Smaller power than linear piecewiese

Table 1. TIDA-00468 Solutions for Industry Challenges

1.2 System Specification

Table 2	. Key System	s specifications
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PARAMETER	SPECIFICATION	VALUE	DETAILS	
Sensor type	K-type thermocouple			
Temperature Range	T _{RANGE}	-270°C to 1372°C		
Cold junction compensation (CJC) type	CJC	PT100		
Power supply voltage range	VCC	3.3 V		
	INL	< 0.02°K	See Section 3.5, See Section 5.2.1	
Thermocouple temperature linearization	DNL	<0.02°K	See Section 3.5, See Section 5.2.1	
Responsiveness	tr	< 25 ms	See Section 5.2.4 (in absence of any software damping and any diagnostic functions)	
Designed to test	14-pin JTAG BoosterPack form factor			

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2 Theory of Operation

2.1 Spline

In mathematics, a spline is a polynomial function that is piecewise defined. In other words, the numeric function is defined as different polynomial equations over non-overlapping segments.

The International Temperature Scale of 1990 (ITS-90) is the latest revision of the International Temperature Scale (dating back to 1990). The ITS-90 shows the following splines for a thermocouple type K [1]:

Temperature range from -270° C to 0° C with n = 10:

Use Equation 1 to plug in the following parameters:

$$\mathsf{E} = \sum_{i=0}^{n} \mathsf{d}_{i} \left(\mathsf{t}_{90} \right)^{i}$$

d0 = 0.0

d1 = $3.945\ 012\ 802\ 5\ x\ 10^{-2}$ d2 = $2.362\ 237\ 359\ 8\ x\ 10^{-5}$ d3 = $-3.285\ 890\ 678\ 4\ x\ 10^{-7}$ d4 = $-4.990\ 482\ 877\ 7\ x\ 10^{-9}$ d5 = $-6.750\ 905\ 917\ 3\ x\ 10^{-11}$ d6 = $-5.741\ 032\ 742\ 8\ x\ 10^{-13}$ d7 = $-3.108\ 887\ 289\ 4\ x\ 10^{-15}$ d8 = $-1.045\ 160\ 936\ 5\ x\ 10^{-17}$ d9 = $-1.988\ 926\ 687\ 8\ x\ 10^{-20}$ d10 = $-1.632\ 269\ 748\ 6\ x\ 10^{-23}$

Temperature range from 0°C to 1372°C:

Use Equation 2 to plug in the following parameters:

$$\mathsf{E} = \sum_{i=0}^{9} \mathsf{d}_{i} \left(t_{90} \right)^{i} + \mathsf{b}_{0} \exp \left[\mathsf{b}_{1} \left(t_{90} - 126.9686 \right)^{2} \right]$$

The parameters are:

 $d0 = -1.760\ 041\ 368\ 6\ x\ 10^{-2}\ d5 = -5.607\ 284\ 488\ 9\ x\ 10^{-13}$ $d1 = 3.892\ 120\ 497\ 5\ x\ 10^{-2}\ d6 = 5.607\ 505\ 905\ 9\ x\ 10^{-16}$ $d2 = 1.855\ 877\ 003\ 2\ x\ 10^{-5}\ d7 = -3.202\ 072\ 000\ 3\ x\ 10^{-19}$ $d3 = -9.945\ 759\ 287\ 4\ x\ 10^{-8}\ d8 = 9.715\ 114\ 715\ 2\ x\ 10^{-23}$ $d4 = 3.184\ 094\ 571\ 9\ x\ 10^{-10}\ d9 = -1.210\ 472\ 127\ 5\ x\ 10^{-26}$ $b0 = 1.185\ 976\ x\ 10^{-1}$ $b1 = -1.183\ 432\ x\ 10^{-4}$

NOTE: All tables are for a reference temperature of 0°C.

(1)

(2)

Theory of Operation

2.2 Practical Considerations for Temperature Linearization

Table 3 lists the different options with their relative benefits.

TECHNIQUE	ACCURACY	POWER	REACTIVITY	CODE SIZE	COMMENTS
Arithmetic	Highest	Highest	Lowest	Lowest	Consider this technique for ease of software reading and when power is not a limitation. The computation time can under power limited processing become too long. The possibility to do arithmetic to achieve highest accuracy is dependant on the availability of a computable mathematical function (some complex physical phenomena are not well modeled by equations).
Spline (with polynomial degree > 1)	Variable	Variable	Variable	Variable	Splines performances are a compromise between the quality of the fit and the degree of the polynomials used.
Linear	Poorest	Lowest	Highest	Lowest	Consider this technique when the maximum error is within the total system budget.
Piecewise linear (look-up table)	Undefined	Low	Good	Highest	Look-up tables are often designed with the constant-step approach, which leads to the highest code size.
Optimized sensor linearization	As desired	Low	Good	As desired	An optimized look-up table, like the table in TIDA-00468, allows the user to define the digital error budget contribution from sensor linearization, reducing the memory footprint to the lowest required amount.

Table 3. Overview of Different Options for Sensor Linearization

2.2.1 General Introduction to Interpolation

The first use of linear interpolation can be traced as far back as the times of the Babylonian astronomers [1]; however, the method is still widely used in modern systems, such as sensor transmitters, where computing resources do not allow for complex computations on-the-fly.

Thousands of years of research have been focused on improving the accuracy of interpolation as the computation capabilities continuously improve. However, the focus of this guide is to explore how to design a look-up table for a given system target. By actively designing the look-up table instead of reusing pre-existing ones, the user can significantly reduce the software footprint and significantly improve the accuracy. Over the millennium of research in the field of interpolation, the science has progressed from first-order interpolation (linear) to higher orders of interpolation (reaching third-order interpolation by 1280AD), and later progressing to classes of functions beyond polynomials, while also improving the spacing of interpolation points, or Chebyshev nodes [1]. This reference guide uses the Chebyshev node approach but focuses on the practical aspects for defining how many and how far apart the interpolation nodes for a linear interpolation must be placed to achieve a level of accuracy compatible with the noise budget (assigned at the system level). Upon establishing the theoretical basis, the user can study a practical example for a look-up table of the thermocouple type K, note the benefits of a look-up table with a reduced size, and highlight the increase of accuracy at the system level.

2.2.1.1 Mathematical Definition of Interpolation

Consider that there is an unknown function, f(x), for which its exact values at (n + 1) are provided at distinct points (see Equation 3).

$$x_0 < x_1 < ... < x_n$$
, i.e., $f(x_0)$, ..., $f(x_n)$

The interpolation problem is to construct a function I(x) that passes through these points, that is, to find a function I(x) such that can meet the interpolation requirements. To solve the interpolation problem, construct a function I(x) that passes through these points (see Equation 4).

$$\forall i \in [0, n] f(x_i) = I(x_i)$$

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(4)

(3)



2.2.1.2 Interpolation Function Classes

The I(x) function has historically been polynomial or piecewise polynomial, and for many centuries the function was purely linear approximation. However, recently users have begun considering the use of trigonometric or more complex functions. Going beyond the interpolation of the values of function, the question of the minimum order required to guarantee matching n points, guaranteeing not only the value at given points, but also that the nth derivative also matches the function were also investigated (Hermite interpolation). The question of selecting the interpolation points was investigated by Chebyshev [1].

NOTE: In mathematics, a spline is a numeric function that is piecewise-defined by polynomial functions. A spline also has a sufficiently high degree of smoothness in places where the polynomial pieces connect, which are known as knots.

Given the function f in :

 $f(x): \mathbb{R} \to \mathbb{R}$

Now define $I_{[a;b]}(t)$, which is the linear interpolation of f on the segment [a,b] as Equation 5:

$$\forall (a, b) \in \mathbb{R}^{2}, \forall t \in [a, b] |_{[a, b]}(t) = \frac{t - b}{a - b} \times f(a) - \frac{t - a}{a - b} \times f(b)$$
(5)

Now define $\mathcal{E}_{[a;b]}(t)$, which is the error function introduced when using the interpolated function $(I_{[a;b]})$ instead of function f (see Equation 6):

$$\forall (\mathbf{a}, \mathbf{b}) \in \mathbb{R}^{2}, \forall \mathbf{t} \in [\mathbf{a}, \mathbf{b}]$$

$$\in_{[\mathbf{a}, \mathbf{b}]}(\mathbf{t}) = f(\mathbf{t}) - I_{[\mathbf{a}, \mathbf{b}]}(\mathbf{t})$$
(6)

This error function E can be modeled with a Taylor series or with a generic solution.

2.2.1.3 Small Signal Error Bounding

Under the conditions set by Taylor's theorem, the Taylor series is able to provide a good approximation. Assuming these conditions are met, the calculations can be written as Equation 7 and Equation 8:

$$f(a) = f(t) + (a-t) \times f'(t) + \frac{1}{2} \times (a-t)^2 \times f''(t) + O(f^3)$$

$$f(b) = f(t) + (b-t) \times f'(t) + \frac{1}{2} \times (b-t)^2 \times f''(t) + O(f^3)$$
(8)

Equation 7 and Equation 8 are replaced in Equation 6:

$$\begin{split} &\in [a,b] (t) = f(t) - I_{[a,b]}(t) \\ &= f(t) - \frac{t-b}{a-b} \times f(a) + \frac{t-a}{a-b} \times f(b) \\ &= f(t) - \frac{t-b}{a-b} \times \left[f(t) + (a-t) \times f'(t) + \frac{1}{2} \times (a-x)^2 \times f''(t) + O(f^3) \right] + \frac{t-a}{a-b} \times \left[f(t) + (b-t) \times f'(t) + \frac{1}{2} \times (b-x)^2 \times f''(t) + O(f^3) \right] \\ &= f(t) - \frac{(t-b) - (t-a)}{a-b} \times f(t) + \frac{(t-b)(a-t) - (t-a)(b-t)}{a-b} \times f'(t) + \frac{1}{2} \times \left[\frac{(t-b)(a-t)^2 - (t-a)(b-t)^2}{a-b} \right] \times f''(t) + O(f^3) \end{split}$$

Given that:

$$\frac{(t-b)(a-t)^{2}-(t-a)(b-t)^{2}}{a-b} = (t-a)\times(t-b)$$
(11)

(10)

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Equation 11 can be simplified into Equation 12:

$$\in_{[a,b]} (t) = \frac{1}{2} \times (t-b) \times (t-a) \times f''(t) + O(f^3)$$
(12)

Note that Equation 13 is always true after computing the maximum of the first variable of Equation 11 over the segment [a,b]:

$$\forall t \in [a,b]$$

$$(t-a) \times (b-t) \le \frac{(b-a)^2}{4}$$
(13)

Applying the inequality in Equation 13 to Equation 12 leads to Equation 14:

$$\in_{[a,b]} (t) \le \frac{(b-a)^2}{8} \times \max f''(t)$$
(14)

A practical aspect of Equation 14 is that the user can now provide a bounded error for a linear interpolation if the error budget is small (in that the Taylor's theorem is applicable). The side effect, however, is that the step size is small and small-setup sizes often result in a look table with a significant memory footprint.

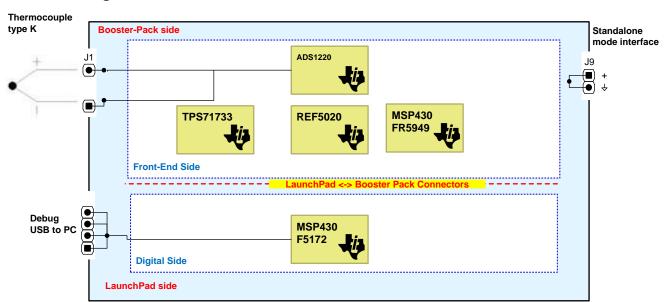
2.2.1.4 Generic Solution

The generic solution is based on unpublished math and has been implemented on a tool running on a standard Windows (or Linux) PC. These details are only available to customers by request from a local TI sales representative.

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3 Block Diagram





3.1 Input Filter Design

Summarizing all of the above contributions:

- 1. Noise due to $R_{\scriptscriptstyle F}$: 0.029 μV
- 2. Noise due to R_B : 0.0872 μV
- 3. Inaccuracy of capacitor : 0.001 μ V
- 4. Filter error : 11 μV
- 5. R_F mismatch : 0.18 μ V
- 6. Inaccuracy of R_{F} : 0.11 μV
- 7. Drift of R_F : 0.123 μ V
- 8. Offset error : 0.86 µV
- 9. Inaccuracy of R_B : 0.529 μ V

Total filter error = $\sqrt{0.029^2 + 0.0872^2 + 0.001^2 + 11^2 + 0.18^2 + 0.11^2 + 0.123^2 + 0.86^2 + 0.529^2} = 11.05 \,\mu\text{V}$ (15)

The total filter error corresponds to a temperature error of approximately 0.279°C.

Most of this filter error is deterministic and can be calibrated out. After calibrating out this filter error, only the drift and noise remain.

Block Diagram

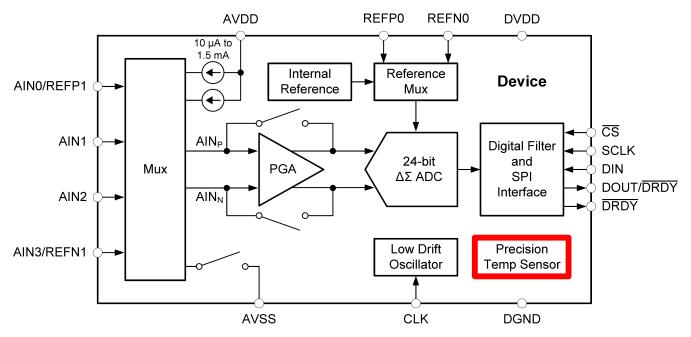
3.2 Cold Junction Compensation (CJC)

Using Internal Temperature Sensor for CJC

The ADS1220 device integrates a high-precision temperature sensor that is useful when measuring the temperature of the cold junction as shown in Figure 2. To measure the internal temperature of the ADS1220 device, set the device mode to internal temperature sensor by adjusting the bit test set (TS) to '1' in the configuration register. A precise board layout is critical to achieve sufficient thermal conductivity between the cold junction and the ADS1220 package as shown in Figure 4; a careful consideration of board layout also ensures optimal performance of the device.

The ADS1220 device does not perform automatic cold-junction compensation of the thermocouple. This compensation must be done in the microcontroller that interfaces with the ADS1220 device. The microcontroller requests one or more readings of the thermocouple voltage from the ADS1220 and then sets the device to internal temperature sensor mode (TS = 1) to acquire the temperature of the cold junction. Use the microcontroller to implement calculations that can compensate for the cold junction temperature.

Using the integrated temperature sensor is not possible in every application (for example, if the accuracy is not sufficient or if the ADS1220 device cannot be placed close enough to the cold junction). When using the integrated temperature sensor is impossible, use the additional analog input channels of the ADS1220 device with a thermistor or RTD to measure the cold junction temperature. Figure 3 shows a table of the applicable ADS1220 internal temperature sensor specifications.





TEMPERATURE SENSOR	· · ·				
	Conversion resolution		14		Bits
Temperature sensor resolution	Temperature resolution		0.03125		°C
	$T_A = 0^{\circ}C$ to +75°C	-0.5	±0.25	0.5	°C
Temperature sensor accuracy	$T_{A} = -40^{\circ}C$ to +125°C	_1	±0.5	1	°C
	vs analog supply voltage		0.0625	0.25	°C/V

Figure 3. ADS1220 Internal Temperature Sensor Specifications





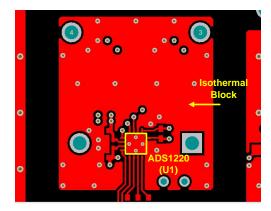


Figure 4. Placement of ADS1220 In the Isothermal Block for CJC

3.2.1 Using RTD for CJC

An RTD can be used for CJC. To measure the temperature of the cold junction, place the Pt100 RTD (in a TO-92 package) inside the transistor retainer clip of the thermocouple connector, as shown in Figure 5. The voltage measured across the RTD is proportional to the temperature (which is determined by characteristics of the RTD). The reference voltage for the ADC is also derived from the IDAC and external precision reference resistor. This external precision resistor determines the reference voltage to the ADC in addition to the input common-mode of the PGA. This ratiometric approach ensures a more effective number of bits (ENOB) because the noise in the IDAC reflects in the reference as well as in the input, and thus tends to cancel-off. This design uses a three-wire RTD configuration despite the close proximity between the ADS1220 device and RTD Pt100 sensor. Therefore, IDAC1 = IDAC2 = 250 μ A.

Choosing $R_{REF} = 3.24 \text{ k}\Omega$, a ±0.1% tolerance or better, and a 25-ppm/°C drift or less results in a common-mode voltage close to the mid-supply (AVDD + AVSS) / 2.

 $V_{REF} = 2 \times IDAC \times R_{REF} = 2 \times 250 \ \mu A \times 3.24 \ K\Omega = 1.62 \ V$

The operating temperature range for the circuit is -40° C to 85° C, which corresponds to a resistance of 84.27 Ω to 130.9 Ω when referring to the PT100 RTD table. The resulting minimum and maximum voltage inputs are:

 $V_{RTD (MIN)}$ at -40 °C = 84.27 Ω × 250 μ A = 21.0675 mV

V_{RTD (MAX)} at 85 °C = 130.9 Ω × 250 μA = 32.725 mV

PGA GAIN =
$$\frac{V_{\text{REF}}}{V_{\text{RTD}(\text{MAX})} \text{ at } + 85^{\circ}\text{C}} = \frac{+1.62 \text{ V}}{+32.725 \text{ mV}} = 49.5 \text{ V/V}$$

A 32-V/V PGA gain is the minimum that can be selected for the ADS1220 device. Achieve this PGA gain by setting GAIN [2:0]: Gain Configuration bits to 101 bits in configuration register 0.

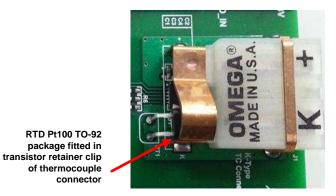


Figure 5. Placement of RTD Pt100 Sensor Inside Transistor Retainer Clip

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3.3 Analog Chain Error Budget Estimation

3.3.1 Thermocouple Channel Error Calculation

As for the filters, the main design target is to keep initial error contribution to the total error comparable or smaller than the initial error of the thermocouple sensor itself. Considering the manufacturing limitations of the Type K thermocouple (mainly related to the purity of materials), the initial error of the Thermocouple sensor (tolerance class 1) is typically smaller than 1.5°C between –200°C and 375°C and then better than 0.4% up to 1375°C (maximum thermocouple temperature range). See Section 5.1 *Thermocouple Fundamentals* – "*Back to Basics*" of the <u>TIDU449</u> User's Guide.

The error calculation is then split in two parts. Low temperature (-200° C to 375° C) and high temperature (from 375° C to 1375° C) to make a direct comparison with the sensor initial accuracy. Considering the low temperature range, the maximum differential input signal is 15.34 mV and the minimum is -3.554 mV.

So in this range:

sensitivity = [15.34 mV - (-3.554 mV)] / [375°C - (-100°C)] = 39.77 µV

Based on that, the ADS1220 specifications can be translated into temperature (typical values).

3.3.1.1 Error in Typical Corner

The initial errors at 25°C (those that can be corrected by calibrating the system) are:

1. Offset error: 4 μV

Corresponding to 4 μ V / (39.77 μ V/°C) = 0.10°C

2. Gain error: 150ppm

Corresponding to (150 ppm × 15.34 mV) / (39.77 μ V/°C) = 0.06°C

3. **Reference voltage accuracy** can be calculated as follows:

Inaccuracy = [(2.048 - 2.045) / ((2.048 + 2.045) / 2)] × 100% = 0.1465%

Considering that for an ADC:

$$CODE = V_{IN} \times (2^{24} / V_{REF})$$

This will translate into an additional gain error:

error (μ V) = (V_{IN} / (1 – 0.1465%)) – V_{IN} = 22.5 μ V

Corresponding to 22.5 μ V / (39.77 μ V/°C) = 0.566°C

4. INL (Integral nonlinearity): 6 ppm

The error of INL with respect to the input signal is:

error (
$$\mu$$
V) = 6 ppm × full scale = 6 ppm × ((2 × V_{REF}) / PGA)) = 0.77 μ V

Corresponding to 0.77 µV / (39.77 µV/°C) = 0.02°C

In addition, there are **all drift errors and non-deterministic errors** (for example, noise) that cannot be corrected by calibration. Being the initial or nominal operating temperature of the system is 25° C while the temperature range is from -40° C to 85° C, maximum temperature span is Δ **T** = $25 - (-40) = 65^{\circ}$ C.

1. **Offset drift:** 0.08 μ V/°C

The offset drift in ADS1220 temperature span is:

$$V_{\text{offset drift}} = (0.08 \ \mu\text{V/}^{\circ}\text{C}) \times 65^{\circ}\text{C} = 5.2 \ \mu\text{V}$$

Corresponding to 5.2 μ V / (39.77 μ V/°C) = 0.13°C

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2. Gain drift: 1 ppm/°C

The gain drift in ADS1220 temperature span is:

 $V_{\text{gain drift}} = V_{\text{IN}}((1 \text{ ppm/°C}) \times 65^{\circ}\text{C}) = V_{\text{IN}} \times 65 \text{ ppm} = 0.996 \text{ }\mu\text{V}$

Corresponding to 0.996 μV / (39.77 $\mu V/^{\circ}C)$ = 0.025 $^{\circ}C$

3. **Reference drift:** 5 ppm/°C

$$\begin{split} V_{\text{reference drift}} &= V_{\text{REF}}((5 \text{ ppm/°C}) \times 65^{\circ}\text{C}) = V_{\text{REF}} \times 325 \text{ ppm} = 665.6 \ \mu\text{V} \\ \text{CODE} &= V_{\text{IN}} \times (2^{24} / (V_{\text{REF}} + V_{\text{reference drift}})) \\ \text{CODE} &= V_{\text{IN}} \times (2^{24} / (V_{\text{REF}}(1 + \text{drift}\%))) \\ \text{drift}\% &= (V_{\text{reference drift}} / V_{\text{REF}}) \times 100\% = 0.0325\% \end{split}$$

So

error (
$$\mu$$
V) = V_{IN} - (V_{IN} / (1 + 0.0325%)) = 4.98 μ V

Corresponding to 4.98 μ V / (39.77 μ V/°C) = 0.125°C

4. ADC-PGA noise: $0.23 \ \mu V$

Corresponding to 0.23 μ V / (39.77 μ V/°C) = 0.006°C

Add up the errors and then get the total un-calibrated errors from –100°C to 375°C (considering a maximum ambient temperature span $\Delta T = 25 - (-40) = 65$ °C).

 $Typ \ non-calibrated \ error < \sqrt{0.1^2 + 0.06^2 + 0.566^2 + 0.02^2 + 0.13^2 + 0.025^2 + 0.125^2 + 0.006^2} = 0.61^{\circ}C$

After system calibration, only offset drift, Gain drift, and Reference drift are left. So:

Typ IDEAL CALIBRATED = $\sqrt{0.13^2 + 0.025^2 + 0.125^2 + 0.006^2} = 0.18^{\circ}C$

Looking at the high temperature (375°C to 1375°C), the maximum differential input signal is 54.886 mV in the look-up table for 1375°C.

Sensitivity of the thermocouple: 39.543 μ V/°C, so: sensitivity = (54.886 - 15.343) / (1375 - 375) = 39.543 μ V/°C

1. Offset error: 4 µV

Corresponding to 4 μ V / (39.543 μ V/°C) = 0.10°C

- Gain error: 150 ppm Corresponding to (150 ppm × 54.886 mV) / (39.543 μV/°C) = 0.21°C
- 3. Reference voltage accuracy: 0.1465%

error (μ V) = (V_{IN} / (1 – 0.1465%)) – V_{IN} = 80.34 μ V

Corresponding to 80.34 μ V / (39.543 μ V/°C) = 2.03°C

4. INL (Integral nonlinearity): 6 ppm

The error of INL with respect to the input signal is

error (μ V) = 6 ppm × full scale = 6 ppm × ((2 × V_{REF}) / PGA) = 0.77 μ V

Corresponding to 0.77 μ V / (39.543 μ V/°C) = 0.02°C

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Block Diagram

As before, all **drift errors and non-deterministic** errors can be calculated as follows (maximum temperature span is $\Delta T = 25 - (-40) = 65^{\circ}$ C.

1. Offset drift: 0.08 µV/°C

 $V_{\text{offset drift}} = (0.08 \ \mu\text{V/}^{\circ}\text{C}) \times 65^{\circ}\text{C} = 5.2 \ \mu\text{V}$

Corresponding to 5.2 μ V / (39.543 μ V/°C) = 0.13°C

2. Gain drift: 1 ppm/°C

 $V_{gain drift} = V_{IN}((1 \text{ ppm/°C}) \times 65^{\circ}\text{C}) = V_{IN} \times 65 \text{ ppm} = 3.57 \text{ }\mu\text{V}$

Corresponding to 3.57 μ V / (39.543 μ V/°C) = 0.09°C

3. Reference drift: 5 ppm/°C

$$\begin{split} V_{\text{reference drift}} &= V_{\text{REF}}((5 \text{ ppm/}^{\circ}\text{C}) \times 65^{\circ}\text{C}) = V_{\text{REF}} \times 325 \text{ ppm} = 665.6 \ \mu\text{V} \\ &\quad \text{CODE} = V_{\text{IN}} \times (2^{24} / (V_{\text{REF}} + V_{\text{reference drift}})) \\ &\quad \text{CODE} = V_{\text{IN}} \times (2^{24} / (V_{\text{REF}}(1 + \text{drift}\%))) \\ &\quad \text{drift}\% = (V_{\text{reference drift}} / V_{\text{REF}}) \times 100\% = 0.0325\% \end{split}$$

So

error (μ V) = V_{IN} - (V_{IN} / (1 + 0.0325%)) = 17.83 μ V

Corresponding to 17.83 μ V / (39.543 V/°C) = 0.451°C

4. ADC-PGA noise: $0.23 \ \mu V$

Corresponding to 0.23 μ V / (39.543 μ V/°C) = 0.006°C Now add up the errors and then get the **total un-calibrated** errors from **375°C to 1375°C** (considering maximum ambient temperature span Δ T = 25 – (-40) = 65°C.

$$\textit{Typ non-calibrated error} < \sqrt{0.1^2 + 0.21^2 + 2.03^2 + 0.02^2 + 0.13^2 + 0.09^2 + 0.451^2 + 0.006^2} = 2.10^{\circ} C$$

While

Typ IDEALCALIBRATED =
$$\sqrt{0.13^2 + 0.09^2 + 0.451^2 + 0.006^2} = 0.478^{\circ}C$$

From the above, it is evident that the value of gain error, reference voltage accuracy, gain drift, reference drift is related to the value of V_{IN} , and the value of offset error, INL, offset drift is fixed. It means that the total error is a functional of V_{IN} .

Figure 6 summarize all the results in a graph comparing the Thermocouple sensor accuracy to the one of the front end for calibrated and non-calibrated systems at maximum ΔT and typical and worst-case conditions. This shows that the acquisition system is not the dominant contributor to the total accuracy even when no calibration is performed.

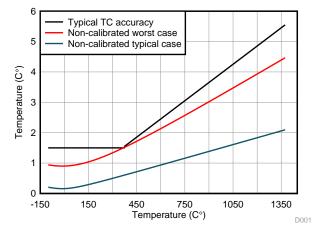


Figure 6. Calculated Error in °C as Function of Measured Temperature

3.3.1.2 Error in Worst-Case Corner

Considering the worst-case corners specifications:

- Offset error: 30 µV
- Gain error: 1000 ppm
- INL: 15 ppm
- Offset drift: 0.3 µV/°C
- Gain drift: 4 ppm/°C
- Reference drift: 40 ppm/°C (characterization suggest this number is more likely in the range of 25 ppm/°C)

Based on the same calculations explained before:

- Temperature range (-100°C to 375°C)
- Offset error: 0.754°C
- Gain error: 0.386°C
- Reference voltage accuracy: 0.556°C
- INL: 0.05°C
- Offset drift: 0.49°C
- Gain drift: 0.10°C
- Reference voltage drift: 1.0°C
- ADC-PGA noise: 0.006°C

Block Diagram

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All the errors are added up as ideal un-calibrated.

 $\textit{Max non-calibrated error} < \sqrt{0.754^2 + 0.386^2 + 0.556^2 + 0.05^2 + 0.49^2 + 0.10^2 + 1.0^2 + 0.006^2} = 1.51^{\circ}\text{C}$

Max IDEAL CALIBRATED = $\sqrt{0.05^2 + 0.49^2 + 0.10^2 + 1.0^2 + 0.006^2} = 1.12^{\circ}C$

- Temperature range (375°C to 1375°C)
- Offset error: 0.754°C
- Gain error: 1.39°C
- Reference voltage accuracy: 2.03°C
- INL: 0.05°C
- Offset drift: 0.49°C
- Gain drift: 0.361°C
- Reference voltage drift: 3.60°C
- ADC-PGA noise: 0.006°C

$$\textit{Max non-calibrated error} < \sqrt{0.754^2 + 1.39^2 + 2.03^2 + 0.05^2 + 0.49^2 + 0.361^2 + 3.60^2 + 0.006^2} = 4.47^{\circ} \text{C}$$

Max IDEAL CALIBRATED =
$$\sqrt{0.05^2 + 0.49^2 + 0.361^2 + 3.60^2 + 0.006^2} = 3.65^{\circ}C$$

Typical calibrated thermocouple sensors can be as accurate as 0.25°C up to 150°C and better than 0.2% at higher temperatures (see the blue curve in Figure 7). This front-end typical error stays below 0.12°C up to 150°C and below 0.03% in the higher temperature range.

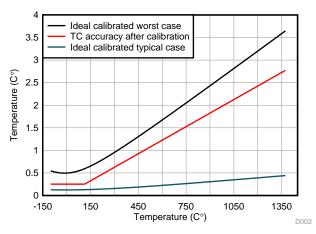


Figure 7. Calculated Error in °C as Function of Measured Temperature in Calibrated System



3.3.2 RTD Channel Error Calculation

As mentioned already, an RTD is used as cold junction compensation in the range of -40° C to 85°C. A two-wire connection with one current source of 250 µA is implemented. The reading is a ratiometric reading. The ADS1220 uses an external reference that is built injecting the same excitation current used for the RTD in a precise, low drift reference resistor (R_{REF} = 6490 Ω). By doing that, the measured value is independent form the precision of the current itself but is only related to the ratio of the two resistors (RTD and reference resistor). Please refer to TIDA-00165 for a detailed description.

From the RTD (Pt100) look-up table (see), the minimum and maximum resistance values in the temperature range can be found. These are, respectively, **84.27** Ω to **130.9** Ω (–40°C to 85°C).

So minimum and maximum voltage input are:

$$\begin{split} V_{min} &= 84.27 \ \Omega \times 250 \ \mu A \ / \ 1000 = 21.0675 \ mV \\ V_{max} &= 130. \ 9\Omega \times 250 \ \mu A \ / \ 1000 = 32.725 \ mV \end{split}$$

So, the ADC input voltage to temperature relation is:

 $V_{change} = (32.725 \text{ mV} - 21.0675 \text{ mV}) / (85^{\circ}\text{C} - (-40^{\circ}\text{C})) = 0.09326 \text{ mV/}^{\circ}\text{C}$

1. Offset error: 4 µV

Corresponding to 4 μ V / (93.26 μ V/°C) = 0.043°C

2. Gain error: 150 ppm

32.725 mV × 150 ppm / 1000 = 4.9087 µV

Corresponding to 4.9087 μ V / (93.26 μ V/°C) = 0.052°C

3. Reference resistor accuracy: 0.1%

maximum variation of $R_{\rm ref}$ = 6490 Ω × 0.1% = 6.49 Ω

The maximum change in voltage is: 6.49 $\Omega \times 250 \mu A = 1.6225 \text{ mV}$

$$\begin{split} \text{CODE} &= \text{V}_{\text{IN}} \times (2^{24} / (\text{V}_{\text{REF}} + \text{V}_{\text{reference change}})) \\ \text{CODE} &= \text{V}_{\text{IN}} \times (2^{24} / (\text{V}_{\text{REF}}(1 + \text{accuracy}\%))) \\ \text{accuracy} &= (\text{V}_{\text{reference change}} / \text{V}_{\text{REF}}) \times 100\% = 0.1\% \end{split}$$

So

error (μ V) = V_{IN} - (V_{IN} / (1 + 0.1%)) = 32.69 μ V

Corresponding to 32.69 µV / (93.26 µV/°C) = 0.35°C

4. INL (Integral nonlinearity): 6 ppm

The error of INL with respect to the input signal is error (μ V) = 6 ppm × full scale = 6 ppm × ((2 × V_{REF}) / PGA) = 0.608 μ V

Corresponding to 0.608 µV / (93.26 µV/°C) = 0.0065°C

All drift errors and non-deterministic errors can be calculated as follows (being a ratiometric measurement, maximum ΔT is at 85°C and is equal to 85°C -25°C = 60°C).

1. Offset drift: $0.08 \ \mu V/^{\circ}C$

$$V_{\text{offset drift}} = (0.08 \ \mu\text{V/}^{\circ}\text{C}) \times (85^{\circ}\text{C} - 25^{\circ}\text{C}) = 4.8 \ \mu\text{V}$$

Corresponding to 4.8 μ V / (93.26 μ V / °C) = 0.0515°C



Block Diagram

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2. Gain drift: 1 ppm/°C $V_{gain drift} = V_{IN}((1 ppm/°C) \times 60°C) = V_{IN} \times 60 ppm = 1.96 \mu V$ Corresponding to 1.96 $\mu V / (93.26 \mu V/°C) = 0.021°C$ 3. Reference drift: 10 ppm/°C $V_{reference drift} = V_{REF}((10 ppm/°C) \times 60°C) = V_{REF} \times 600 ppm = 973.5 \mu V$ $CODE = V_{IN} \times (2^{24} / (V_{REF} + V_{reference drift}))$ $CODE = V_{IN} \times (2^{24} / (V_{REF}(1 + drift%))))$ $drift% = (V_{reference drift} / V_{REF}) \times 100\% = 0.06\%$ So $error(\mu V) = V_{IN} - (V_{IN} / (1 + 0.06\%)) = 19.62 \mu V$ Corresponding to 19.62 $\mu V / (93.26 V/°C) = 0.21°C$ 4. ADC-PGA noise: 0.23 μV

Corresponding to 0.23 μV / (93.26 $\mu V/^{\circ}C)$ = 0.002°C

As a result the total non-calibrated errors is:

 $\textit{Typ non-calibrated error} < \sqrt{0.043^2 + 0.052^2 + 0.35^2 + 0.0065^2 + 0.0515^2 + 0.021^2 + 0.21^2 + 0.002^2} = 0.419^{\circ} C$

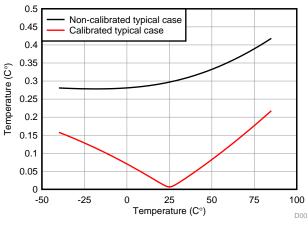
The ideal calibrated system error is obtained summing only offset drift, Gain drift, Reference drift, and noise:

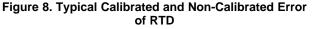
Typ IDEAL CALIBRATED =
$$\sqrt{0.021^2 + 0.0515^2 + 0.21^2 + 0.002^2} = 0.217^{\circ}C$$

Non-calibrated and calibrated error from –40°C to 85°C are shown in Figure 8. Considering now the **worst-case corners specifications:**

 $\textit{Max non-calibrated error} < \sqrt{0.322^2 + 0.351^2 + 0.351^2 + 0.016^2 + 0.19^2 + 0.08^2 + 0.21^2 + 0.002^2} = 0.662^{\circ}C$

Max IDEAL CALIBRATED =
$$\sqrt{0.016^2 + 0.19^2 + 0.08^2 + 0.21^2 + 0.002^2} = 0.298^{\circ}C$$





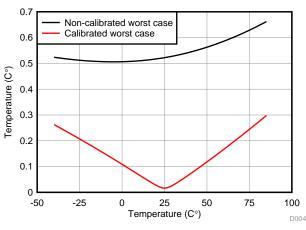


Figure 9. Worst-Case Calibrated and Non-Calibrated Error



Block Diagram

(17)

3.3.3 Total Error Calculation (Filters, Thermocouple, and RTD)

The total error is the result of all the preceding calculations.

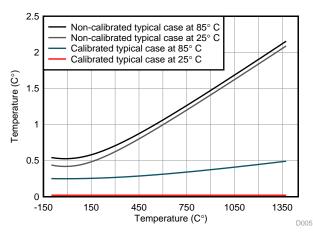


Figure 10. Typical Calibrated and Non-Calibrated Total Front End Error (at 25°C and 85°C)

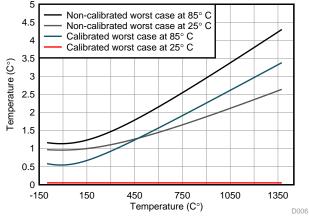


Figure 11. Worst-Case Calibrated and Non-Calibrated Total Front End Error (at 25°C and 85°C)

3.4 Digital Contribution to Noise Budget

The goal of this TIDA-00468 design is to limit the memory footprint while keeping the processing time to a minimum without impacting the system accuracy. In Equation 17, calculate the system error budget to be:

$$\varepsilon_{\text{system}} = \sqrt{\varepsilon_{\text{analog}}^2 + \varepsilon_{\text{digital}}^2}$$

where

- ϵ_{analog} = the error calculated through Section 3.1 to Section 3.3
- $\epsilon_{digital}$ = the error introduced by the signal processing in the "digital" domain

 $\epsilon_{digital}$ = ADC quantization error + LUT quantization error plus interpolation error

NOTE: If the user consults the ADC datasheet to quantify the quantization noise, the result is an ADC quantization error = LSB / 2 = $2.048 \text{ V} / 2^{24} / 2 = 0.06 \mu \text{V} \approx 1$ -mK error (which is negligible per the preceding analog noise estimations).

To achieve a goal of having:

$\varepsilon_{\text{system}} \approx \varepsilon_{\text{analog}}$	(18)
equivalent to: ^ɛ analog ≫ ^ɛ digital	(19)
Make the value specific and set the design target to be such that Equation 20 is verified:	
$\varepsilon_{analog} > 10 \times \varepsilon_{digital}$	(20)

The next step is to evaluate $\epsilon_{digital}$.

When using the look-up table, the table quantization error is prone to further error because published lookup tables are limited in the number of digits due to print reasons. Error due to this lack of data can lead to a significant contribution of quantization error.

18 Optimized Sensor Linearization for Thermocouple

Block Diagram

Figure 12 shows an example of how references on the web, including from the NIST, only have three digits after the period:

ITS-90	Table for	type K the	rmocoupl	е							
°C	0	-1	-2	-3	-4	-5	-6	-7	-8	-9	-10
				Thermo	electric Vo	oltage in m	۱V				
-270	-6.458										
-260	-6.441	-6.444	-6.446	-6.448	-6.450	-6.452	-6.453	-6.455	-6.456	-6.457	-6.458
-250	-6.404	-6.408	-6.413	-6.417	-6.421	-6.425	-6.429	-6.432	-6.435	-6.438	-6.441
-240	-6.344	-6.351	-6.358	-6.364	-6.370	-6.377	-6.382	-6.388	-6.393	-6.399	-6.404
-230	-6.262	-6.271	-6.280	-6.289	-6.297	-6.306	-6.314	-6.322	-6.329	-6.337	-6.344
-220	-6.158	-6.170	-6.181	-6.192	-6.202	-6.213	-6.223	-6.233	-6.243	-6.252	-6.262
-210	-6.048	-6.048	-6.061	-6.074	-6.087	-6.099	-6.123	-6.135	-6.135	-6.147	-6.158
-200	-5.891	-5.907	-5.922	-5.936	-5.951	-5.965	-5.980	-5.994	-6.007	-6.021	-6.035

Figure 12. ITS-90 Table for Type K Thermocouple

Table 4 shows a comparison of the values between the look-up table in the preceding Figure 12 (a table reproduced in many other industrial references and publications), to the actual values when evaluating the splines defined by ITS-90:

Table 4. Comparing the Two Sources

TEMPERATURE	NIST LOOK-UP TABLE VALUES (emf IN mV)	ITS-90 SPLINE EVALUATION (emf IN mV)
–270°C	-6.458	-6.45773795274
–269°C	-6.457	-6.45691755801
–268°C	-6.456	-6.45592235046
–267°C	-6.455	-6.45474680693
–266°C	-6.453	-6.45338583845

The user can define the interpolation error after defining the following:

- typeK.emf(T) is the function which gives the emf of a type-K at a given temperature T (in Celsius)
- typeK.emf⁻¹(E) is the function which gives the temperature of a type-K which generates an emf E (in mV)
- LUT_{NIST}(E) is the function that linearly interpolates between two points of the NIST look-up table
- ϵ_{NIST} is the linear interpolation error if using the values given by the NIST look-up tables (see Equation 21)

 $\epsilon_{NIST}(T) = LUT_{NIST}(emf(T)) - emf^{-1}(emf(T))$

- $\epsilon_{\mbox{\tiny ITS}}$ is the linear interpolation error if using the values given by the evaluation of the spline from the ITS- 90 specifications



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The following Figure 13, Figure 14, and clearly show that $\varepsilon_{\text{NIST}}$ is higher than ε_{ITS} . $\varepsilon_{\text{NIST}}$ leads to a maximum error of 0.25 K, while ε_{ITS} leads to a maximum error of 0.027K; so a tenth of the error is induced by insignificant digits in the lookup tables. For these reasons, the look-up tables must be designed to minimize the quantization noise.

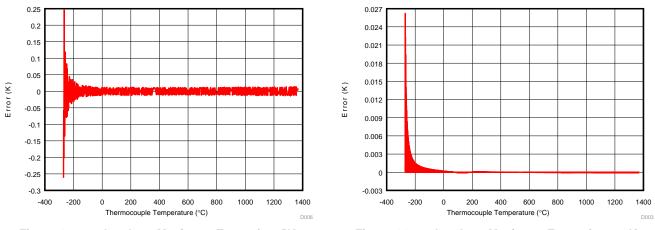


Figure 13. ϵ_{NIST} Leads to Maximum Error of 0.25K

Figure 14. $\epsilon_{\mbox{\tiny HTS}}$ Leads to Maximum Error of 0.028 K

3.5 Optimized Look-Up Table Design

Consulting the data from Section 3.4, the reader can assume that an optimized look-up table must not have an error contribution larger than 0.02 K (20 mK).

Using the PC side tool, the designer can generate such an optimized linearization and validate its total error in a similar way, as inSection 3.4.

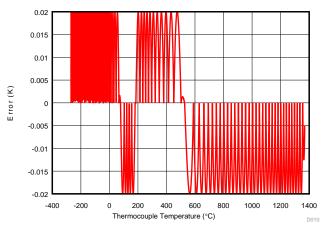


Figure 15. Error in K for Optimized Look-Up Table linearization (Maximal Error Design of 0.02 K—Error Contribution of No More Than 20 mK)

NOTE: The absolute error contribution is lower even though the look-up table size is more than ten times smaller than the "classic" look-up table.



4 Layout Consideration

To achieve the analog section noise budget, consider the instructions for the layout in the following subsection.

4.1 Cold Junction Compensation

To enable the measurement of cold junction compensation (CJC) through the internal temperature of the ADS1220 device, the user must first have a precise board layout, which is critical to achieve sufficient thermal conductivity between the cold junction and the ADS1220 package, as the following Figure 16 shows. Careful consideration of the board layout also ensures optimal performance of the device.

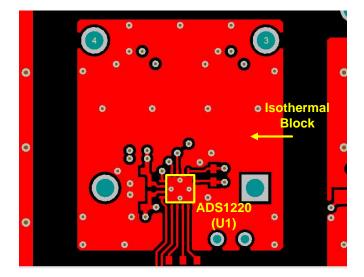


Figure 16. Placement of ADS1220 in Isothermal Block for CJC

5 Verification and Characterization

The following subsections describe how to set up the EVM hardware.

5.1 Test Setup

Consult the *Hardware Test Setup Section* in the *TIDA-00168 User's Guide* for a description of the analog part of the signal chain (TIDU574).

The setup for the digital part of the validation (the signal chain running on the MSP430 device) is as follows:

- 1. Generate on the PC side a list of ADC values (considering the ADC has no offset and no gain error, which is theoretically equivalent to the ADC having been completely calibrated)
- 2. Load those values in a list of long integers in the target
- 3. Run through the list and insert those values in the functions running to the TIDA-00168 hardware (mostly the MSP430 device)
- 4. Output the computed values (in mC) on the UART interface
- 5. Plot the equivalent error on the PC side between the injected ADC value (known values) and the values computed by the MCU



5.2 Test Results

5.2.1 Comparison of Optimized Linearization to All Methods

This section compares the accuracy of different linearization methods to the method known as "optimized linearization" introduced in this TIDA-00468 TI design.



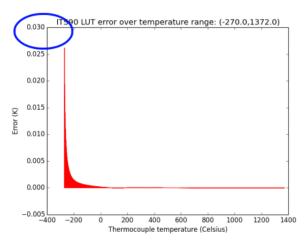


Figure 17. Worst Case: 250 mK

Look-Up Table From Publications (Three Digits)

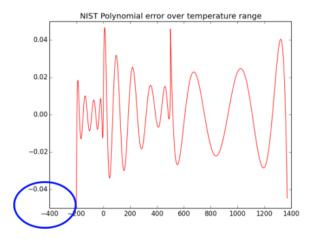


Figure 19. ±40 mK Over Defined Range (Limited to -200°C) Much Worse Down to -270°C

Look-Up Table Generated From ITS-90 Equations

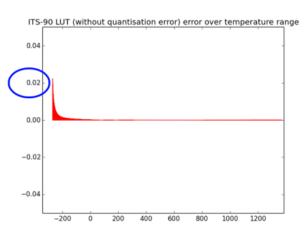


Figure 18. Worst Case: 25 mK

Look-Up Table Generated From ITS-90 Equations

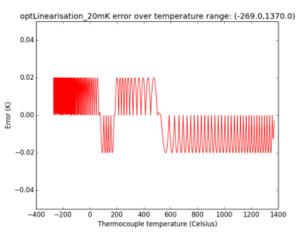


Figure 20. |e| ≤ 20 mK Over Entire Range



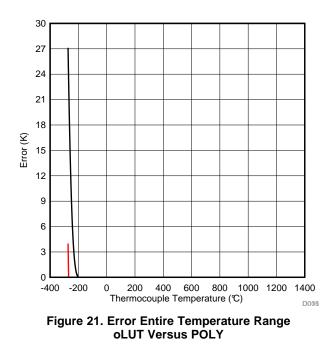
Verification and Characterization

5.2.2 Optimized Linearization Versus Polynomial

Because most modern sensor transmitters currently use polynomial equations, this section focuses on comparing the accuracy of the "optimized linearization" against that of "polynomial linearization".

From the data collected in Section 5.2 Test Results, the two following plots are generated:

- The first one plots the error over the entire temperature range of the Type-K thermocouple. This plots
 obviously leads to significant errors because the polynomials equations are only defined down to -200
 (see Figure 21).
- However, even when restricting the temperature range to the valid one, Figure 21 clearly shows that the polynomial fit is not an accurate modeling of the dual function of the physical response of a thermocouple-to-temperature range. For instance, the maximum error contribution is up to 40 mK (green curve), which is worse than the oLUT data (oLUT in red)



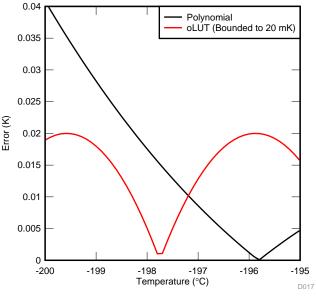


Figure 22. Error Poly Validity Temperature Range oLUT Versus POLY



5.2.3 Memory footprint

To compare the memory footprint the following protocol was observed:

- 1. Compile the SW with "Release" flags (for example: -o2)
- 2. Extract the symbols associated with the different options from the memory map:
 - (a) For the look-up table: The look-up table and the functions
 - (b) For the polynomial: The functions and the floating point library functions
 - (c) For the optimized linearization: All associated symbols

The following bar chart in Figure 23 best summarizes the memory footprint:

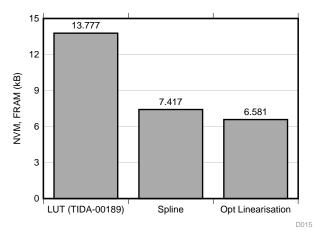


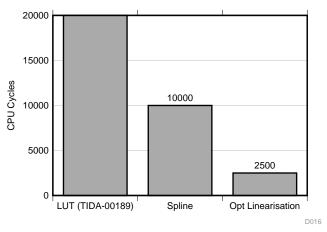
Figure 23. Comparing Footprint Memory

5.2.4 CPU Cycles for Thermocouple Temperature Computation

The number of cycles are calculated by initializing the counter before the linearization function and stopped at the return of the function. The values of the counter were verified to be the same as the clock cycle count from the TI Code Composer Studio[™] (CCS) software.

Note that the function that linearizes (that is, takes a voltage and converts this to a temperature) has a computation time that varies with the data: Using the look-up table, the time to converge to the right entry and for the spline the degree of the polynomial varies with the temperature.

The following bar chart in Figure 24 best summarizes the differences in the CPU cycles:





6 Getting Started

6.1 System Configurations

The TIDA-00468 hardware has two different configurations: Stand-Alone and BoosterPack. The standalone configuration is intended for quick evaluation of the performances mentioned in this document, while the BoosterPack configuration is intended to allow rapid prototyping of solutions leveraging the TI design ecosystem by multiplexing with different MCUs for processing and interfaces (wired or wireless).

6.2 Getting Started With HW in Stand-Alone Node

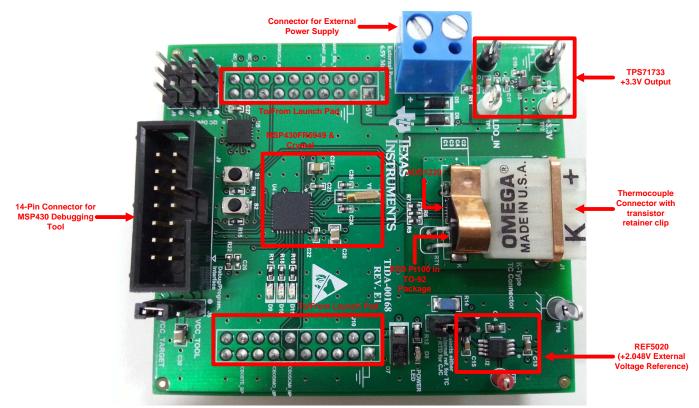


Figure 25. Board Top View

Table 5. Connector, Test Points, and Switches

CONNECTORS, TEST POINTS (TPs), AND SWITCHES	DESCRIPTION
J1	Thermocouple connector
J2	Selects either RTD for CJC or external voltage reference for ADC
J3	External power supply input (must not exceed 6.5 V)
J4, J10	To interface to TI launch pads
J5	Selects either VCC_TOOL or VCC_TARGET
J6, J7, J8	To set the I2C device address for the IO expander
J9	MSP430 debugging tool (SBW) and UART
TP1	LDO input
TP2	3.3-V LDO output
TP3	Temperature output of REF5020
TP4, TP5	GND
TP6	Chassis
S1, S2	General purpose

For the initial board setup the following equipment is required:

- 1. TIDA-00168 board with the MSP430 device pre-programmed
- 2. 6-V battery or power supply
- 3. KEITHLEY™ model 2450 SourceMeter® to provide the temperature equivalent voltage
- 4. HP 3458A 81/2 digit multimeter
- 5. Oscilloscope (optional)

Connections:

- 1. Configure the jumpers on the board as follows:
 - J2: 1-2 to use external voltage reference REF5020 for ADC
 - J2: 2-3 to use RTD in ratiometric configuration for CJC
 - - J5: 1-2 to power up the board from the MSP430 debugging tool
 - J5: 2-3 to power up the board using an external power supply
- 2. Connect a 6-V battery or power supply to J3 make sure the input power supply does not exceed 6.5 V
- 3. Connect the voltage output of the KEITHLEY 2450 SourceMeter (-7 mV to 56 mV) to the thermocouple input J1 (a thermocouple type K can connect to J3, as well)
- 4. Verify the following voltages between
 - - TP2 and (TP4 or TP5): approximately 3.3 V
 - J2 pin-1 and (TP4 or TP5): approximately 2.048 V

6.3 Getting Started With SW in Stand-Alone Mode

6.3.1 Software Update

For MSP430 firmware updates, Code Composer Studio[™] (CCS) or (CCStudio) is recommended. Code Composer Studio is an integrated development environment (IDE) for Texas Instruments (TI) embedded processor families. CCStudio comprises a suite of tools used to develop and debug embedded applications. CCStudio includes compilers for each of TI's device families, source code editor, project build environment, debugger, profiler, simulators, real-time operating system, and many other features. The intuitive IDE provides a single-user interface that guides through each step of the application development flow.

For programming and debugging, the MSP430 implements an embedded emulation module (EEM). The EEM is accessed and controlled through either a 4-wire joint test action group (JTAG) mode or a spy-biwire mode. This reference design supports the spy-bi-wire mode only. For more details on how the features of the EEM can be used in conjunction with (CCS), see the advanced debugging using the enhanced emulation module (SLAA393). The 2-wire interface is made up of the spy-bi-wire test clock (SBWTCK) and the spy-bi-wire test data input/output (SBWTDIO) pins. The SBWTCK signal is the clock signal and is a dedicated pin. In normal operation, this pin is internally pulled to ground. The SBWTDIO signal represents the data and is a bidirectional connection. To reduce the overhead of the 2-wire interface, the SBWTDIO line is shared with the RST/NMI pin of the device. For programming and debugging purposes the SBWTCK, SBWTDIO, VCC, and GND from the debugger must be connected on J5.



Getting Started

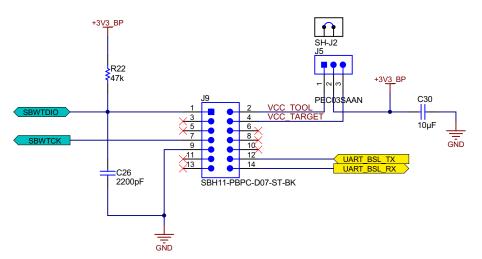


Figure 26. Spy-Bi-Wire Interface for Debugging and Programming of MCU

To program and debug code in the reference design, a MSP430 debugger interface (such as the MSP-FET430UIF) can be used with the proper connections.

Power during debugging

CAUTION

Take special care during debugging operations to avoid damages due to conflicts between different power domains (TPS71733 power and debugger tools power). Read the following section carefully.

If using the locally-generated 3.3-V supply from the TPS71733 during debugging operations, make sure the VCC_Target pin from the debugger interface is connected to the VCC. In the condition that power from the debugger interface is used and there is no local power, make sure that the VCC_Tool pin from the debugger interface is connected to the VCC and disconnect the VCC_Target pin. Refer to Figure 27.

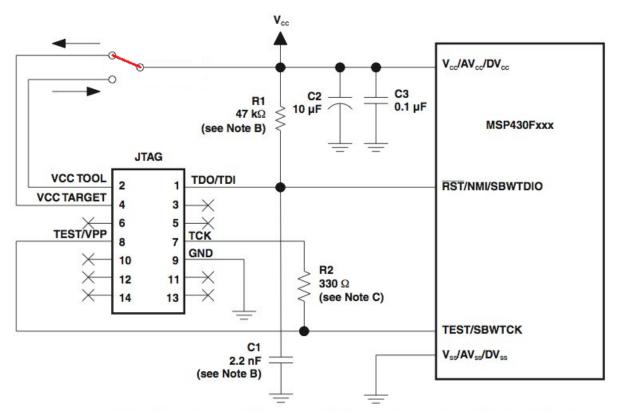


Figure 27. Power Supply Connection During Debugging

6.4 TI LaunchPad[™] Development Kit or TI BoosterPack[™] Plug-In Module Configuration

This configuration either utilizes TI's LaunchPad[™] Development Kit or BoosterPack[™] Plug-in Module to receive over the universal asynchronous receiver/transmitter (UART) lines the temperature, which is then linearized by an on-board TI MSP430[™] MCU. The user can then use the MSP430 in conjunction with the LaunchPad connectors to configure any other BoosterPack that can serve as an interface board, such as:

- TIDA-00339: IO-Link Sensor Transmitter Booster Pack (TIDU681)
- TIDA-00245: Data Isolation for Loop Powered Applications Firmware (TIDC968)
- TIDA-00246: Generic Energy Harvesting Adaptor Module for TEG (TIDU808)



Design Files

7 Design Files

7.1 Schematics

To download the schematic images for each board, see the design files at <u>TIDA-00468</u>.

7.2 Bill of Materials

To download the bill of materials (BOM) for each board, see the design files at TIDA-00468.

7.3 Altium Project

To download the Altium project files for each board, see the design files at TIDA-00468.

7.4 Layout Guidelines

To download the layout guidelines for each board, see the design files at TIDA-00468.

7.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00468.

7.6 Assembly Drawings

To download the assembly files for each board, see the design files at TIDA-00468.

8 References

- 1. Bureau International des Poids et Mesures, *TECHNIQUES FOR APPROXIMATING THE INTERNATIONAL TEMPERATURE SCALE OF 1990*, ITS-90 Techniques Guide (http://www.bipm.org/utils/common/pdf/its-90/ITS-90_Techniques.pdf)
- IEEE.org, A Chronology of Interpolation: From Ancient Astronomy to Modern Signal and Image Processing, IEEE Publication, Vol. 90, No. 3, March 2002, pp. 319-342 (http://www.imagescience.org/meijering/publications/download/pieee2002.pdf)

9 About the Author

MATTHIEU CHEVRIER is a systems architect at Texas Instruments, where he is responsible for defining and developing reference design solutions for the industrial segment. Matthieu brings to this role his extensive experience in embedded system designs in both hardware (power management, mixed signal, and so on) and software (such as low level drivers, RTOS, and compilers). Matthieu earned his master of science in electrical engineering (MSEE) from Supélec, an Ivy League university in France. Matthieu holds patents from IPO, EPO, and USPTO.

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