TI Designs

16-Cell Li-Ion Battery Active Balance Reference Design

TI Designs

The *16-Cell Lithium-Ion Battery Active Balance Reference Design* describes a complete solution for high current balancing in battery stacks used for high voltage applications like xEV vehicles and energy storage systems. The design implements active cell balancing to compensate for both cell charge mismatch and cell capacity mismatch and obtain the optimal efficiency of the pack for the lifetime of the system.

Design Resources

TIDA-00817	Design Folder
EMB1428Q	Product Folder
EMB1499Q	Product Folder
bq76PL455A-Q1	Product Folder

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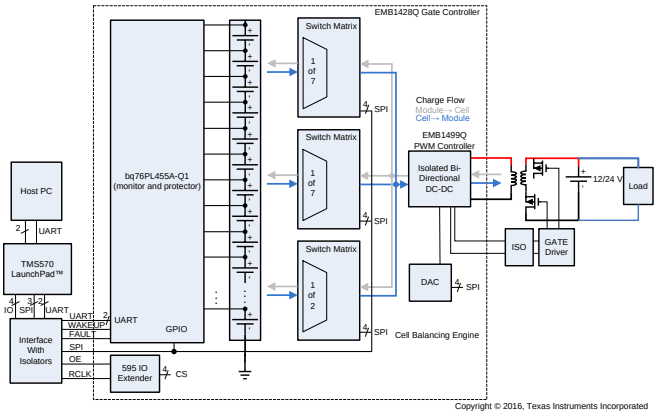
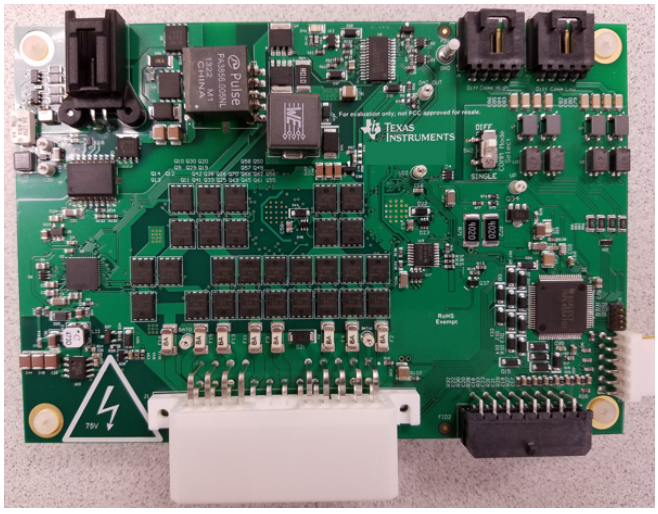
Design Features

- Based on bq76PL455A-Q1 Monitor and Protector
  - Highly Accurate Monitoring of 16 Li-ion Cells
  - Integrated Redundant Protector
- Engineered for High System Robustness
  - 1-Mb/s Stackable Isolated Differential-UART
  - Support for Open Wire Detection
- 2- to 5-A Active Balance
  - Fully Isolated Transfer to External 12-V Supply and Battery
- Capable of Compensating for Charge and Capacity Mismatch
- Up to 16 Stackable Modules

Featured Applications

- Electric and Hybrid Electric Vehicles (EV, HEV, PHEV, Mild Hybrid, Start/Stop)
- 48-V Systems
- Energy Storage (ESS)
- Uninterruptible Power Supplies (UPS)





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1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Series cells	Up to 16 Li-Ion cell batteries (1.8- to 3.8-V nominal voltage)	Section 2
External balance supply	12-V nominal	Section 4.2
Measurement accuracy	See bq76PL455A-Q1 data sheet	—
Cell balance current	2 A to 5 A	—
Shutdown mode current consumption	40 µA	—
Active mode current consumption	10 mA	—
Cell balance converter efficiency	80% to 93%	—
Operating temperature	–30°C to 60°C (limited by Li-Ion cell operating range)	—
Operating humidity	20% to 70%	—
Form factor	3.75- × 5.5-in rectangular PCB	Section 5.3.3.3

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2 System Description

The system is based on the bq76PL455A-Q1 16-channel monitor and protector. The bq76PL455A-Q1 device has been designed with integrated passive balancing field-effect transistor (FET) drivers; however, this design implementation does not use them and instead interfaces to the EMB1428Q and EMB1499Q active balancing chipset to provide high-current active (charge and discharge) balancing. The EMB1428Q switch-matrix gate controller and the EMB1499Q isolated, DC-DC pulse-width-modulation (PWM) controller are used to charge or discharge any one cell in a group of up to 16 cells. Utilizing the isolated daisy-chain communication that is built-in to the bq76PL455A-Q1, this solution can form a battery management system (BMS) module that can be stacked up to 16 modules for very large battery packs.

3 Block Diagram

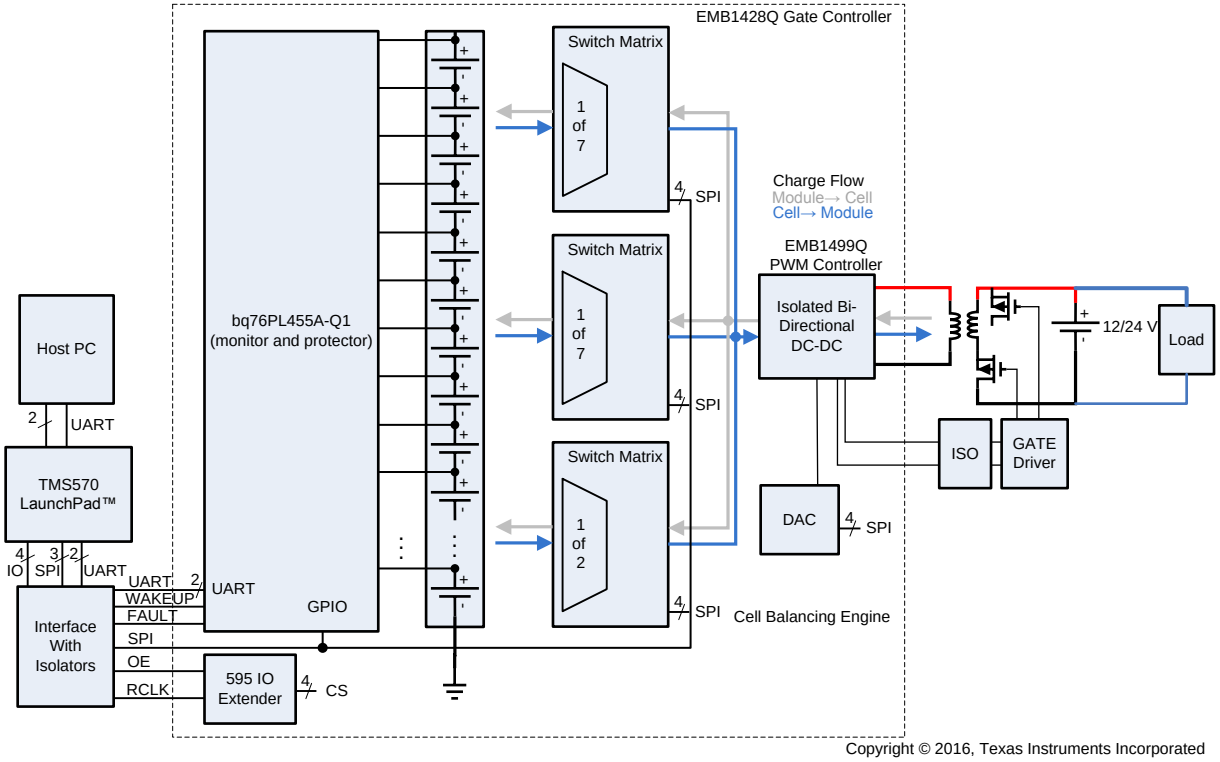

Figure 1. TIDA-00817 Block Diagram

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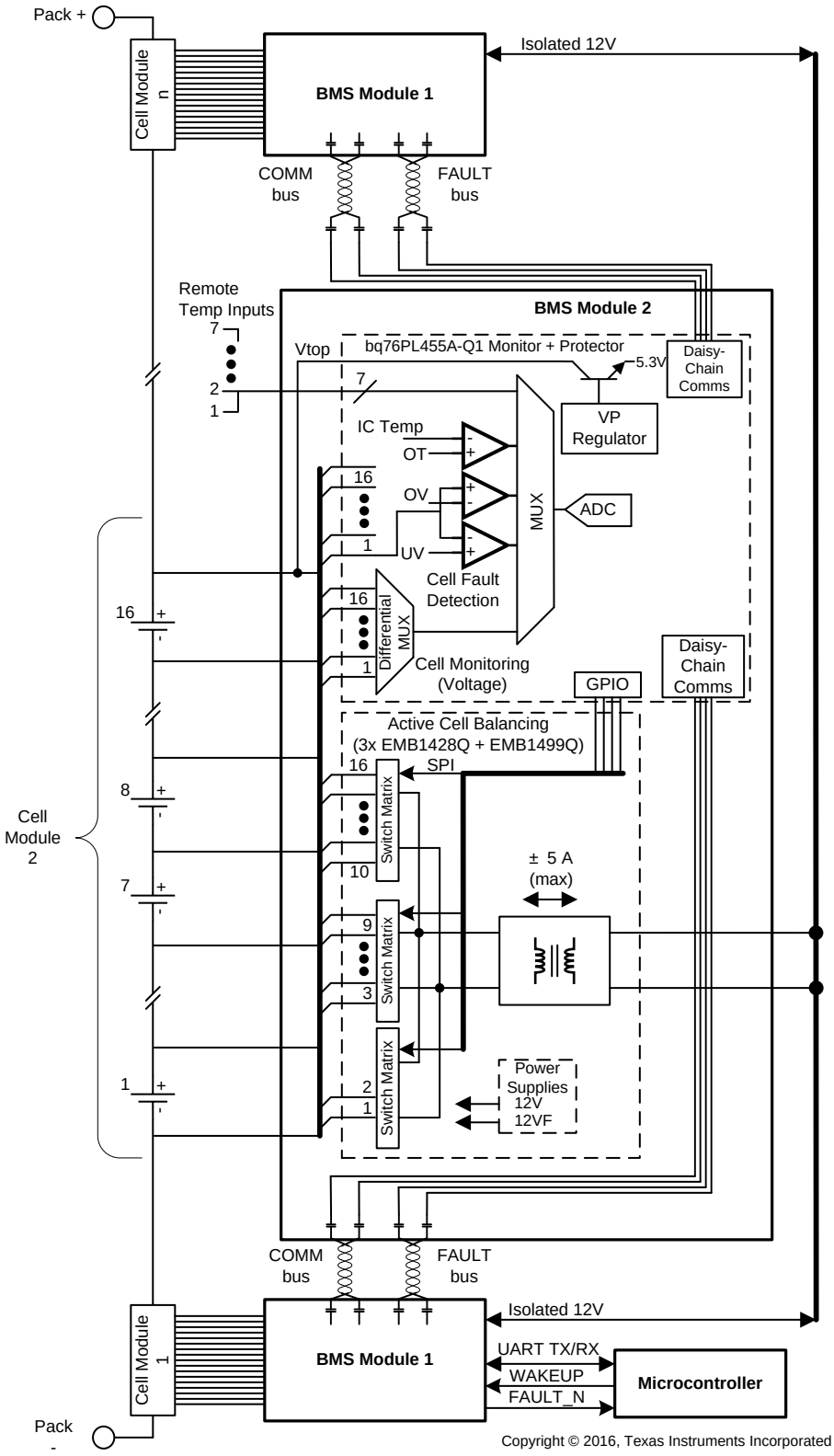

Figure 2. Detailed System Diagram in Stack

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3.1 Highlighted Products

The TIDA-00817 reference design features the following devices:

- EMB1428Q
- EMB1499Q
- bq76PL455A-Q1

For more information on each of these devices, see their respective product folders at www.ti.com.

3.1.1 EMB1428Q Features

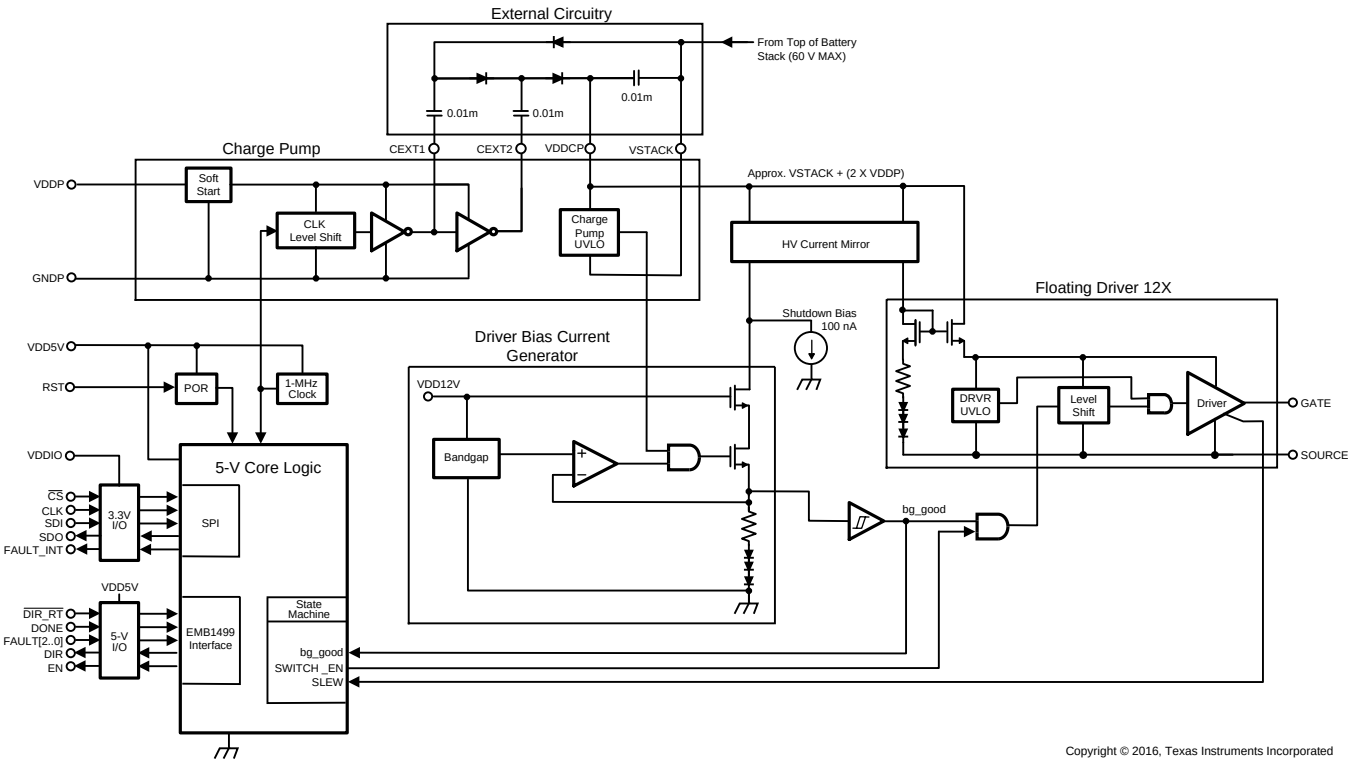

Figure 3. EMB1428Q Block Diagram

The EMB1428Q device features:

- Twelve floating gate drivers
- Serial peripheral interface (SPI) bus interface (for charge and discharge commands and fault reporting)
- Low-power sleep mode

The EMB1428Q switch-matrix gate driver integrated circuit (IC) has been designed to work in conjunction with the EMB1499Q DC-DC controller IC to support TI's switch matrix-based active cell-balancing scheme in a battery management system. The EMB1428 device provides the 12 floating MOSFET gate drivers necessary for balancing up to seven battery cells connected in a series stack. Multiple EMB1428 ICs can be used together to balance a stack of more than seven battery cells.

The EMB1428Q IC interfaces with the EMB1499Q DC-DC controller to control and enable charging and discharging modes. The EMB1428 device uses an SPI bus to accept commands from the main controller (CPU or MCU) as to which battery cell requires charging or discharging and reports any faults back to the main controller (CPU or MCU).

Refer to the EMB1428Q data sheet for more details [1].

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3.1.2 EMB1499Q Features

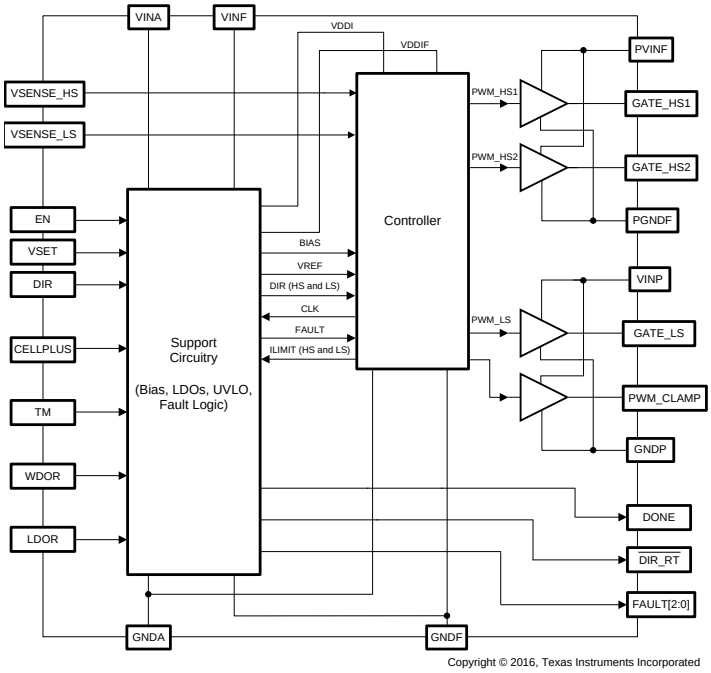

Figure 4. EMB1499Q Block Diagram

- Bidirectional balancing current
- Fully synchronous operation
- Active clamp signal
- 250-kHz switching frequency
- Fault detection includes:
  - Two separate undervoltage lockout (UVLO) cells (one for each external supply)
  - Primary and secondary side current limit
  - Overvoltage protection (OVP) sense and undervoltage protection (UVP) sense on cell being charged
  - Thermal shutdown
  - Watchdog timer
- Balancing current user-selectable through external voltage

The EMB1499Q bidirectional current DC-DC controller IC works in conjunction with the EMB1428 switch-matrix gate driver IC to support TI's switch matrix-based active cell-balancing scheme for a battery management system. The EMB1499Q provides three PWM MOSFET gate signals to a bidirectional forward converter so that its output current, either positive or negative, is regulated around a user-defined magnitude. The EMB1428 device channels this inductor current through the switch matrix to the cell that requires a charge or discharge. In a typical scheme, the EMB1499Q-based forward converter exchanges energy between a single cell and the battery stack to which it belongs, with a maximum stack voltage of up to 60 V. The switching frequency is fixed at 250 kHz. The EMB1499Q senses cell voltage, inductor current, and stack current and provides protection from abnormal conditions during balancing.

The EMB1499Q device also provides an active clamp timing signal to control an external FET driver for the primary-side active clamp FET. The EMB1428 enables and disables the EMB1499Q. Fault conditions detected by the EMB1499Q are communicated to the EMB1428 through the DONE and FAULT pins.

Refer to the EMB1499Q data sheet for more details [2].

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3.1.3 bq76PL455A-Q1 Features

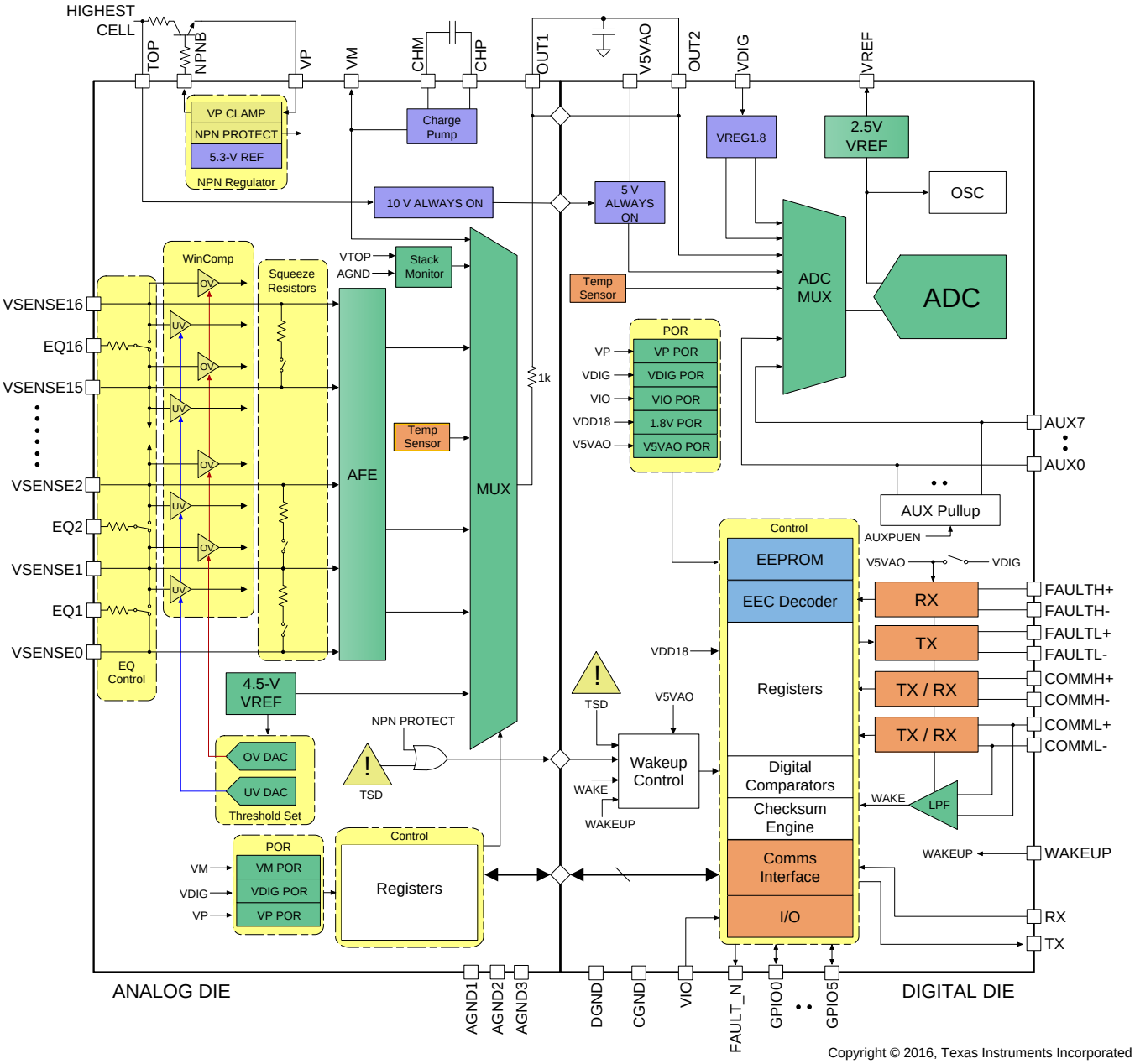

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Figure 5. bq76PL455A-Q1 Block Diagram

- Monitors 6 to 16 cells per device
- Highly accurate monitoring
  - High performance 14-bit analog-to-digital converter (ADC) with internal reference
  - All cells converted in 2.4 ms (nominal)
  - Eight AUX inputs for temperature and other sensors with input voltage of 0 V to 5 V
  - Internal precision reference
- Integrated protector with separate V_{REF} for overvoltage (OV) and undervoltage (UV) comparators and programmable VCELL set points

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- Engineered for high system robustness
  - Up to 1-Mb/s stackable, isolated differential universal asynchronous receiver/transmitter (UART)
  - Up to 16 ICs in daisy-chain with twisted pair
  - Passes bulk current injection (BCI) test
  - Designed for robust hot-plug performance
- Can help customers meet functional safety standard requirements (for example, ISO26262)
  - Built-in self-tests to validate defined internal functions
  - Support for open wire detection

The bq76PL455A-Q1 is an integrated 16-cell battery monitoring and protection device, designed for high-reliability automotive applications. The integrated high-speed, differential, capacitor-isolated communications interface allows up to sixteen bq76PL455A-Q1 devices to communicate with a host through a single, high-speed UART interface.

The bq76PL455A-Q1 device monitors and detects several different fault conditions, including: overvoltage, undervoltage, overtemperature, and communication faults. Six general purpose input/output (GPIO) ports as well as eight analog AUX ADC inputs have been included for additional monitoring and programmable functionality. A secondary thermal shutdown has also been included for further protection.

Refer to the bq76PL455A-Q1 data sheet for more details [3].

3.1.4 Other Devices

Table 2. Additional Major Devices

QUANTITY	DESCRIPTION	VENDOR	PART NUMBER
60	40-V NFETs (30 dual package or 60 single)	Texas Instruments	CSD18504Q5A
1	Transformer	Pulse Engineering	PA3856.005NLT
1	100-V NFET	Vishay	SI7846DP-T1-E3
2	40-V NFET	Texas Instruments	CSD17555Q5A
1	150-V PFET	Vishay	SI7439DP-T1-E3
1	3/1 isolator	Texas Instruments	ISO7342FCDWR
2	Gate driver	Texas Instruments	UCC27511DBVR
2	ESD protection	Texas Instruments	TPD4E05U06QDQARQ1
1	ESD protection	Texas Instruments	TPD2E001IDRLRQ1
2	5-V regulator	Texas Instruments	TPS70950DBVR
1	Buck regulator	Texas Instruments	LM5018MRE/NOPB
1	Comparator	Texas Instruments	TLV3011AIDCKR
1	Window comparator	Texas Instruments	TPS3700QDDCRQ1
1	8-bit DAC	Texas Instruments	DAC081S101CIMK/NOPB
1	SPI I/O expander	Texas Instruments	SN74AHC595QPWRQ1

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4 System Design Theory

The TI active cell balancing architecture has been built around the EMB1499Q bidirectional DC-DC controller, which provides accurate control of high balancing current, as well as the EMB1428Q device to enable one of many series cells as the secondary side of the DC-DC. For the implementation described in this TI Design, the primary side of the DC-DC has been connected to an external isolated 12-V supply, the power for which shares among up to 16 boards in a large battery pack. The cell charge is moved to or from the cell and the external isolated 12-V supply (battery).

4.1 Switch Matrix

View details of the operation and component selection criteria for the EMB1499Q converter circuit in the *Active Chipset Reference Design Guide* [4]. This design guide describes the differences to the fully-isolated implementation in more detail.

Figure 6 shows how the switch matrix FETs are connected and the control signals from the EMB1428Q device.

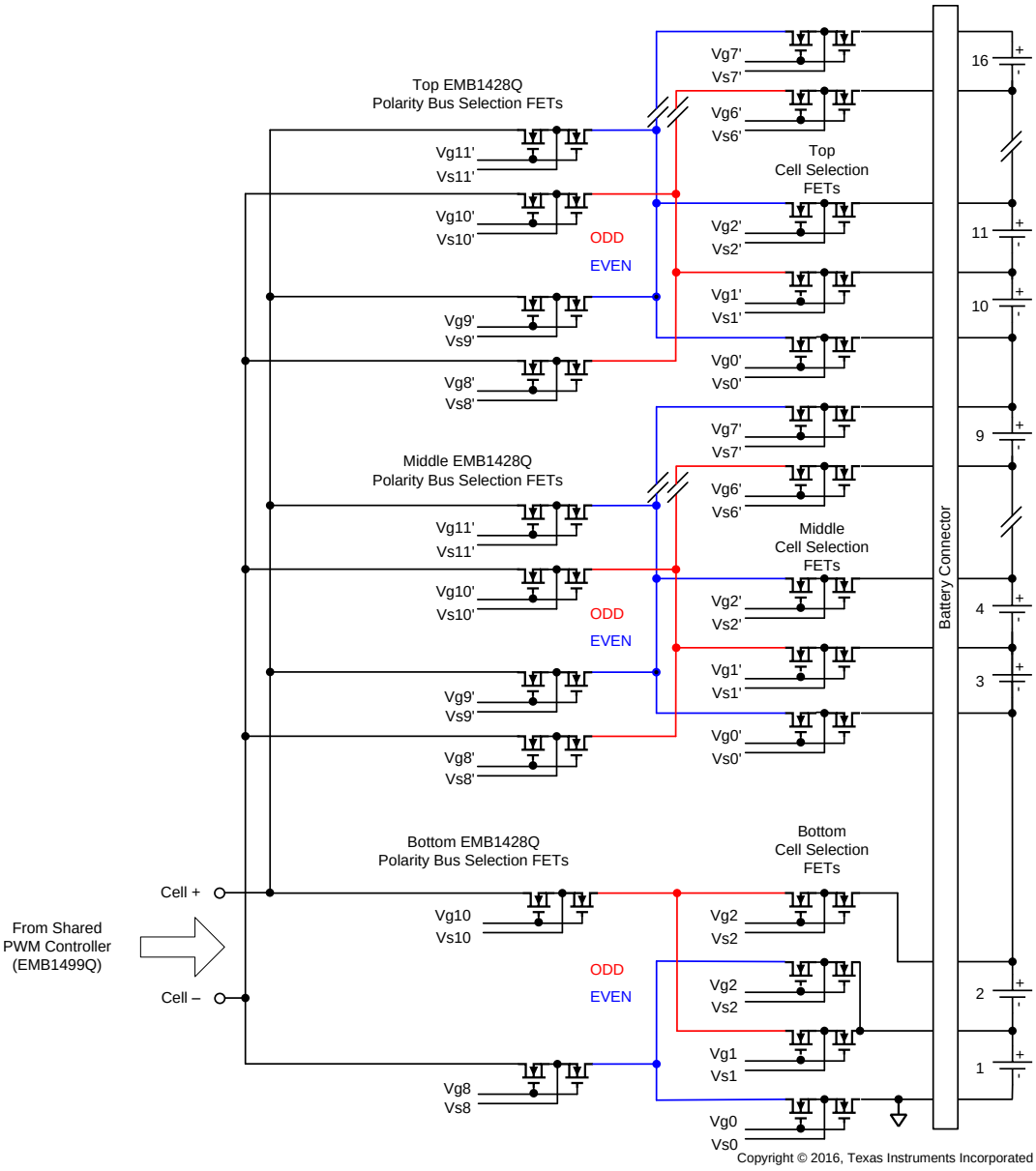

Figure 6. Secondary Switch Matrix

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The implementation of the active balance chipset components described in the *Active Chipset Reference Design Guide* [3] primarily focuses on having a dedicated EMB1499Q device per EMB1428Q device . While this configuration is certainly a viable solution, to implement a more cost-efficient and overall smaller solution, this design enables a single EMB1499Q to share with up to 16 cells. This alternative option means that only a single cell (of up to 16) can be balanced at a time; however, the overall solution can be much smaller.

To have multiple EMB1428Q polarity buses connected to a single EMB1499Q secondary circuit, an additional switch matrix must be placed back-to-back in the polarity selection circuit to extend the voltage rating of the FETs to full module voltage. Compared to Figure 7 from the data sheet [3], the designer can see that an additional FET has been placed back-to-back, which is controlled by Vg8, Vg9, Vg10, and Vg11 (as required) in each EMB1428Q switch-matrix circuit.

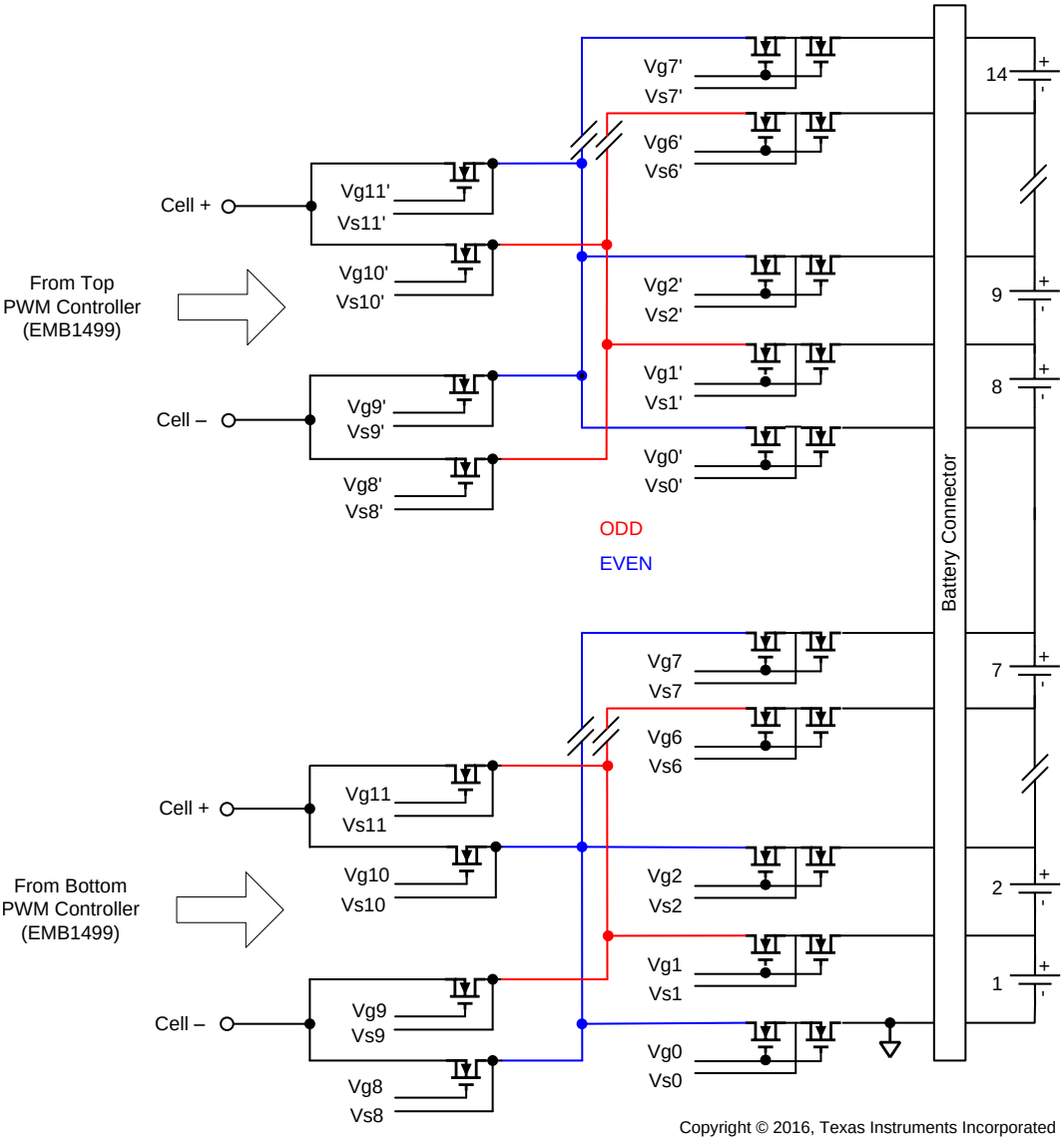

Figure 7. Cell Balancing Simplified Diagram

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4.2 Fully Isolated Bidirectional Converter

View further details of the operation and component selection criteria for the EMB1499Q converter circuit the in data sheet [3], which describes the differences to the fully isolated implementation in more detail.

The EMB1499Q device is isolated to 60 V (ABS max), but in this application, the ideal setup is to have the converter transfer to an external source shared by all boards. This requires a full, pack level isolation, so the isolation must be extended to ~2.5 kV.

Extending the isolation requires several additional components. Figure 8 shows a simplified diagram of the fully-isolated converter circuit. Because the primary switch FET and active clamp FET are in a different voltage domain (presumably referenced to chassis GND), the GATE_LS and PWM_CLAMP signals require isolation with a digital isolator in addition to a dual-channel gate driver.

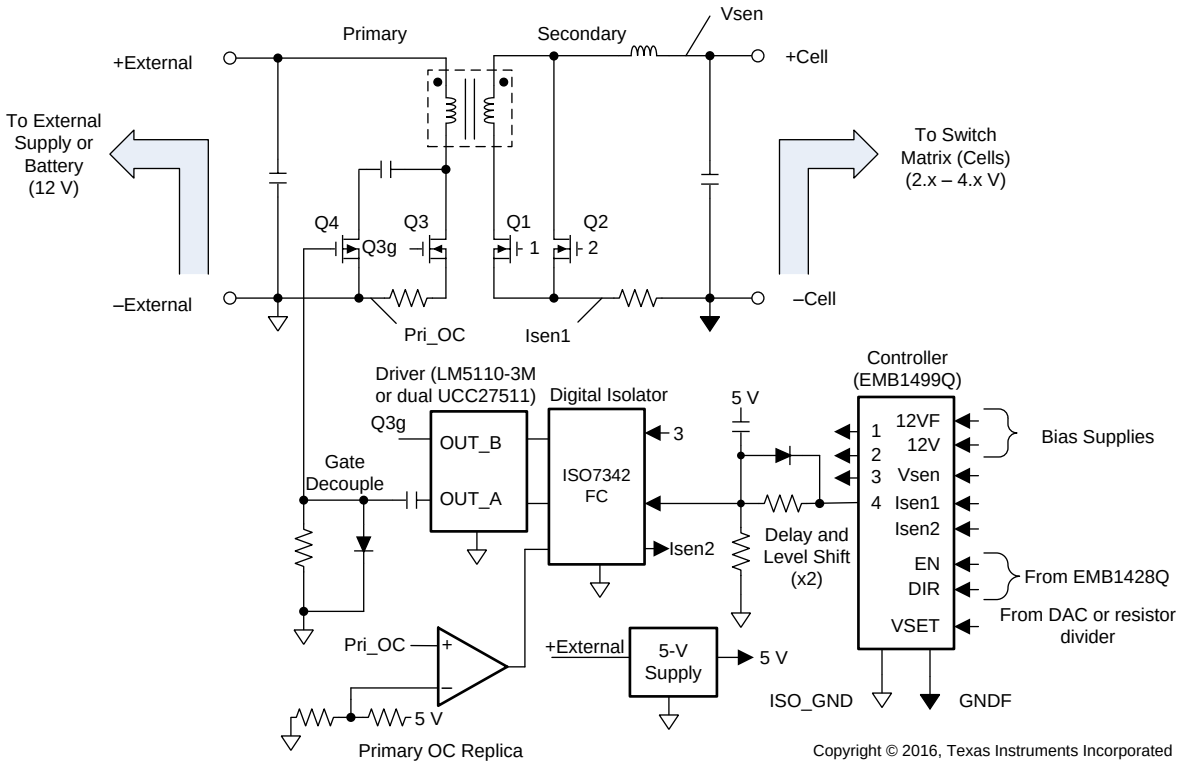

Figure 8. Fully Isolated Converter

If using the LM5110-3M driver (U7), connecting the driver with the PWM_CLAMP signal on the inverting channel (A) is important.

The digital isolator must also be a type that provides a default, low output condition. TI recommends selecting the ISO7342FCQDWQ1 low-power, quad-channel digital isolator; view more details in the following product folder ISO7342-Q1.

Two options are available to extend the isolation of the primary overcurrent (OC) sense (*Isen2* in the preceding ISO7342-Q1, which correlates to the *VSENSE_LS* input on EMB1499Q device):

1. Provide an isolated current sense transformer or sense amplifier
2. Replicate the OC sense threshold detection and simply pass the trigger signal across the digital isolator.

To avoid a complex circuit or development of a custom transformer, replication of the OC sense with an op-amp has been chosen for this design. A resistor divider has been configured to set the comparator threshold to approximately the same level as the EMB1499Q V_{CL_LS} max (170 mV).

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4.3 SPI

The three EMB1428Q and DAC081S101 devices on the board are controlled by receiving commands sent from a serial peripheral interface (SPI) master. The bq76PL455A-Q1 does not have enough GPIOs to provide the SPI and four $\overline{CS}$ signals, so a SN74AHC595 8-bit shift register with a three-state output is used to extend the number of IO pins.

The following Figure 9 shows the SN74AHC595 and DAC081S101 circuits (view the respective data sheets SCLS373 and SNAS323). The signals assigned to the bq76PL455A-Q1 GPIO that relate to the SPI are: SCLK, MOSI, MISO, SN74AHC595 Store, and SN74AHC595 OE.

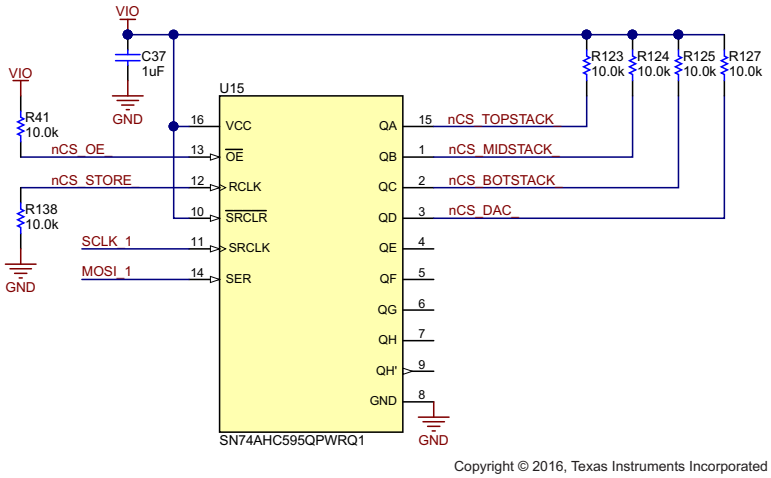

Figure 9. Chip Select and DAC Circuits

4.3.1 SPI Chip Select

The theory of operation is as follows:

1. The bq76PL455A-Q1 GPIO direction register (GPIO_DIR) is written with 0x0C to GPIO[3:2] as outputs.
2. The bq76PL455A-Q1 GPIO output register (GPIO_OUT) is written with bit 3 set to the bit value of bit 7 in the 8-bit value, which represents the desired outputs of the SN74AHC595. The SN74AHC595 output value is to be 0x01 for the top EMB1428Q, 0x02 for the middle EMB1428Q, 0x04 for the bottom EMB1428Q, and 0x08 for the DAC081S101.
3. The bq76PL455A-Q1 GPIO output register (GPIO_OUT) is written with bit 2 set to clock the MOSI bit value into the SN74AHC595.
4. The previous Step 3 is repeated, with the bit 2 cleared (lowering SCLK) and the desired SN74AHC595 output value shifted right one time so that bit 6 of the desired SN74AHC595 output value is output on bq76PL455A-Q1 GPIO pin 3.
5. The previous Step 3 and Step 4 are repeated for all 8 bits of the desired SN74AHC595 output bits.
6. The bq76PL455A-Q1 GPIO output register (GPIO_OUT) is written with bit 0 set to set the SN74AHC595 Store input, storing the 8-bit value to the output latch.
7. The bq76PL455A-Q1 GPIO output register (GPIO_OUT) is written with bit 1 set to set the SN74AHC595 OE input, enabling the 8-bit value to the be output from the SN74AHC595.
8. After this Step 7 completes, the $\overline{CS}$ is set for the following SPI command. Be careful to only set one $\overline{CS}$ at a time.

SPI commands are sent to the target EMB1428Q or DAC081S101 in the same manner, without toggling the SN74AHC595 Store or OE inputs. The SN74AHC595 OE input can be lowered as soon as the command has been clocked out and the SPI transaction completes.

4.3.2 SPI Commands

The sequence of commands is similar in the preceding Section 4.3.1, with the data byte clocked out being the command byte for the EMB1428Q or the DAC output for the DAC08S101.

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5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00817.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00817.

5.3 PCB Layout Recommendations

5.3.1 EMB1428Q

The decoupling caps on the EMB1428Q pins VSTACK, VDDP, VDD12V, and VDDIO must be placed as close as possible to the IC. The layout must keep every gate trace as close as possible to its companion source trace.

5.3.2 EMB1428Q

The EMB1499 is essentially a bidirectional, active-clamp, forward-switching converter, so the designer must simply follow the basic guidelines for the layout of a forward converter. These guidelines entail keeping the traces short and the loops small for discontinuous currents. A couple of unique considerations exist for this specific application or topology.

The designer must ensure that the decoupling cap from EMB1499Q PGNDF to GND is placed close to the EMB1499 converter and that the PCB trace loop is as small as possible. This capacitor is critical to providing an AC return path and must be kept as clean as possible.

The sense lines for the current sense resistor must also be set up as a Kelvin connection. Traces to both sides of the resistor must be close to the EMB1499Q converter to minimize offset errors and reduce the risk of noise coupling.

The layout must also meet the following basic criteria:

1. All decoupling capacitors must be placed as close as possible to the EMB1499Q converter.
2. Run the gate traces in parallel with their associated ground planes for as much of the total runs as possible.
3. Keep the current sensing traces away from high dv/dt nodes, such as the drain of power FETs.
4. Place enough copper underneath the power FETs to help cool down the same.
5. The ideal placement of the EMB1499Q converter is to place it within a couple inches of the power FETs so that the gates are tightly controlled.
6. Place ten or so 8-mil vias on the PCB pad beneath the EMB1499Q converter and connect them to the corresponding ground plane or ground planes on all layers to cool down the chip.

5.3.3 bq76PL455A-Q1

The decoupling caps on the EMB1428Q pins VSTACK, VDDP, VDD12V, and VDDIO must be placed as close as possible to the IC.

The layout must keep every gate trace as close as possible to its companion source trace.

5.3.3.1 Grounding

The bq76PL455A-Q1 device has three, analog ground pins: AGND1, AGND2, and AGND3. AGND1 is a general-purpose analog ground associated with the integrated linear regulator controller VP, while AGND2 and AGND3 are quiet analog grounds for the 2.5-V reference, ADC, AFE, and secondary protector (window comparator) circuitry. The bq76PL455A-Q1 device also has three DGND pins for the digital core and one CGND pin for the differential communications I/Os.

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The creation of a good ground plane in the layout is crucial to obtaining optimal performance from the part. A good ground plane on a dedicated layer improves measurement accuracy, reduces noise, and provides the necessary electrostatic discharge (ESD), electromagnetic interference (EMI), and electromagnetic compatibility (EMC) performance. TI strongly recommends having a minimum of four layers in the PCB, with one layer fully dedicated as an unbroken VSS plane (except thermal reliefs). Avoid placing tracks on this layer to maintain the unbroken integrity of the plane structure.

All seven device grounds must be able to connect to the ground plane with track sections as short as possible to minimize the effects of stray inductance on noise performance.

Although the plane has been employed as a solid GND reference with all the grounds connected to it, good layout practice still requires placing any decoupling capacitors as close as possible to the pin with which they associate. This placement reduces the inductance and keeps the loop area as small as possible, which in turn keeps the capacitors as effective as possible for noise reduction.

Review the *Layout Guidelines* section in the bq76PL455A-Q1 data sheet for the latest recommendations [3].

5.3.3.2 Differential Communications

The bq76PL455A-Q1 device uses two differential communications links to transmit signals between ICs in a stack. Employing differential links provides superior noise immunity. The base device then translates the differential signals back to a single-ended signal.

Maintaining the signal integrity of each differential pair is important to maximize the immunity to interfering signals from external sources.

1. Keep wires and PCB traces as short as possible. Do not exceed the data sheet recommendations.
2. For any single-signal pair between two nodes (ICs), individual wires and traces must have the same length.
3. Unshielded, twisted-pair wiring is required for any cable runs.
4. Run PCB traces in parallel, on the same layer, and without any other traces or planes in between. Long runs must either avoid noisy traces, be stitched at intervals similar to twisted-pair wire, or both.
5. Use high-quality capacitors for voltage isolation between ICs and place them in close physical proximity to each other as part of the parallel-track layout.

All seven device grounds must connect to the ground plane with as short as possible track sections to minimize the effects of stray inductance on noise performance.

Although the plane is employed as a solid GND reference with all grounds connected to it, good layout practice still requires locating any decoupling capacitors as close as possible to the pin with which they associate. This placement reduces the inductance and keeps the loop area as small as possible, which in turn keeps the capacitors as effective as possible in for noise reduction.

Review the *Layout Guidelines* section in the bq76PL455A-Q1 data sheet for the latest recommendations [3].

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5.3.3.3 Dimension Drawing

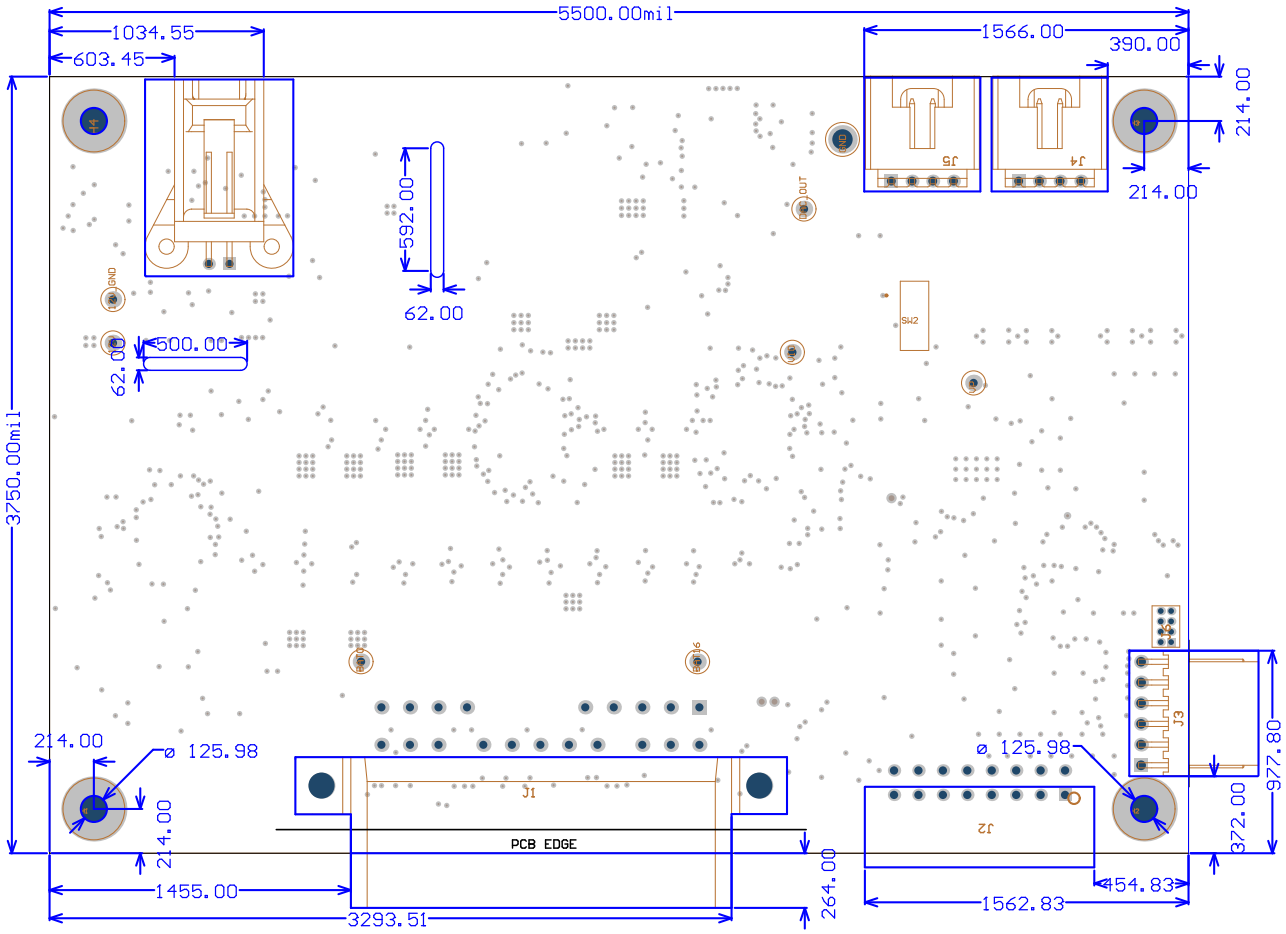

Figure 10. Dimension Drawing

5.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-00817.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00817.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00817.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00817.

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6 Software Files

To download the software files, see the design files at TIDCBZ0.

7 References

1. Texas Instruments, *EMB1428Q Switch Matrix Gate Driver*, EMB1428Q Data Sheet (SNVS812)
2. Texas Instruments, *EMB1499Q Bidirectional Current DC-DC Controller*, EMB1499Q Data Sheet (SNOSCV7)
3. Texas Instruments, *bq76PL455A-Q1 16-Cell EV/HEV Integrated Battery Monitor and Protector*, bq76PL455A-Q1 Data Sheet (SLUSC51)
4. Texas Instruments, *Active Chipset Reference Design Guide*, Reference Guide (SLUUAS6)

8 About the Author

STEPHEN HOLLAND is an applications engineer in the Monitor and Protector - Battery Management Solutions team at Texas Instruments, responsible for developing reference designs for large battery packs in automotive and industrial market applications.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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