PMP15006 Test Results

Test Data

PMP15006

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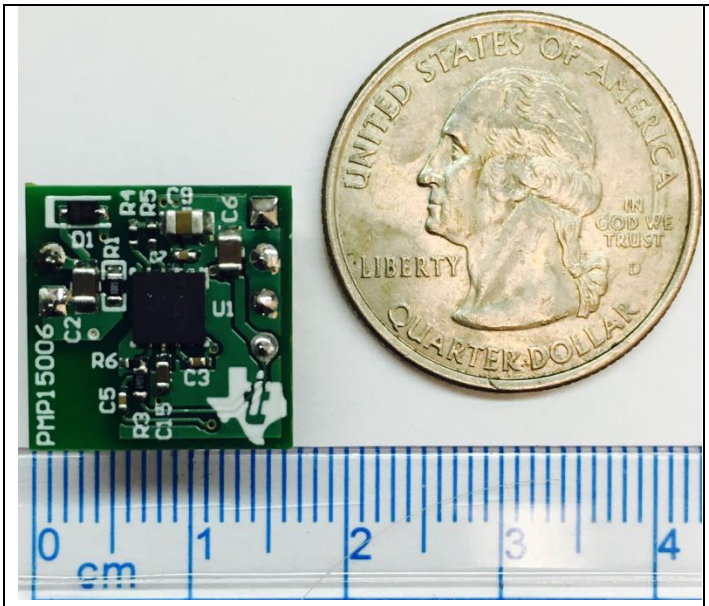
Circuit Description

PMP15006 is a miniature (15 mm X 15 mm) Fly-Buck™ reference design using the LM5017. The primary and secondary outputs are set +/-5V nominal. This ultra-compact design accommodates an input voltage range from 18V to 30V, and a nominal input voltage of 24V. The primary side is set at 5.3V using feedback resistors and the secondary isolated side will supply -5V. The transformer used is a 33uH, LPD8035V coupled inductor from Coilcraft, with a turns-ratio of 1:1, and the maximum operating current on both the primary and secondary rails is set at 250mA each. The switching frequency is set at 475 kHz.

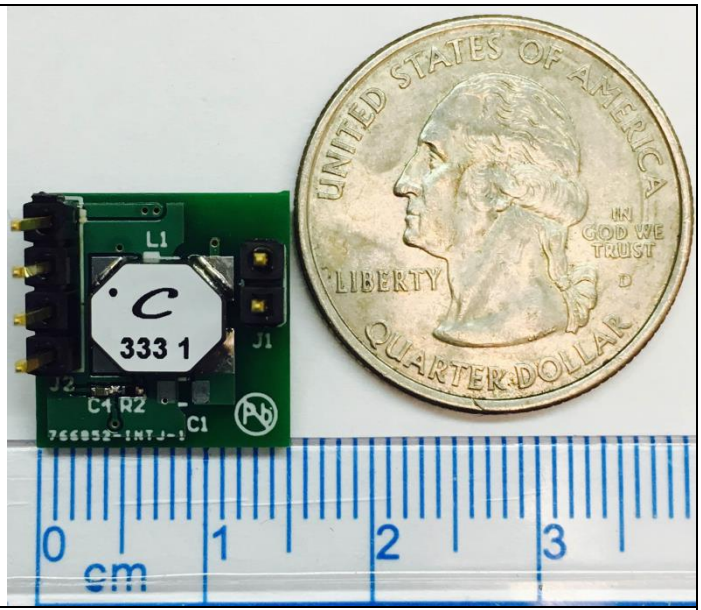
Power Specification

VIN Min.	**18-V**
VIN Max.	**30-V**
$V_{OUT,PRI}$	**~ 5-V (±1%)**
$V_{OUT,SEC}$	**− 5-V (±10%) (Unbalanced Loads)**
	− 5-V (±5%) (Balanced Loads)
$I_{OUT,PRI}$	**0-A-0.250-A**
$I_{OUT,SEC}$	**0-A-0.250-A**
Approximate Switching Frequency	**≈475 KHz**

Board Photo (with LM5017 WSON Package)

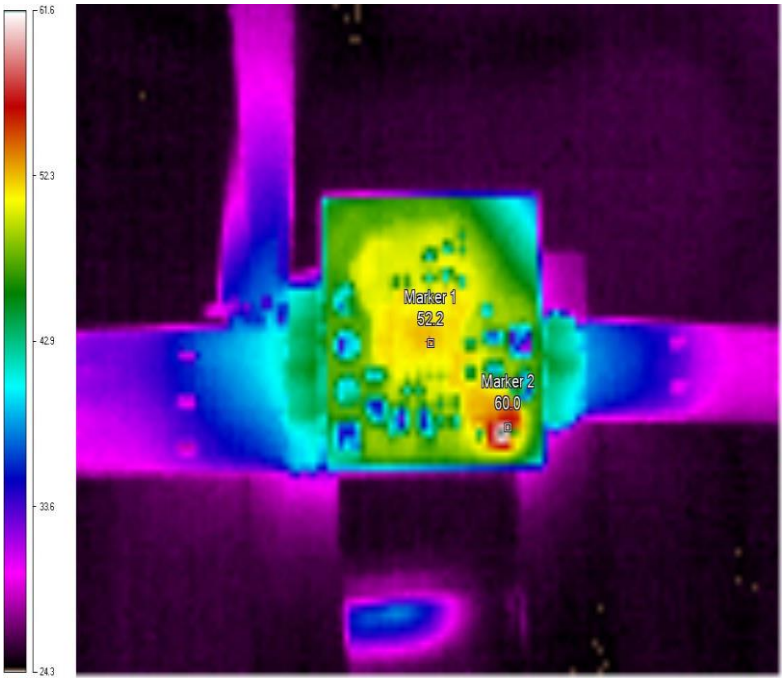


IC View

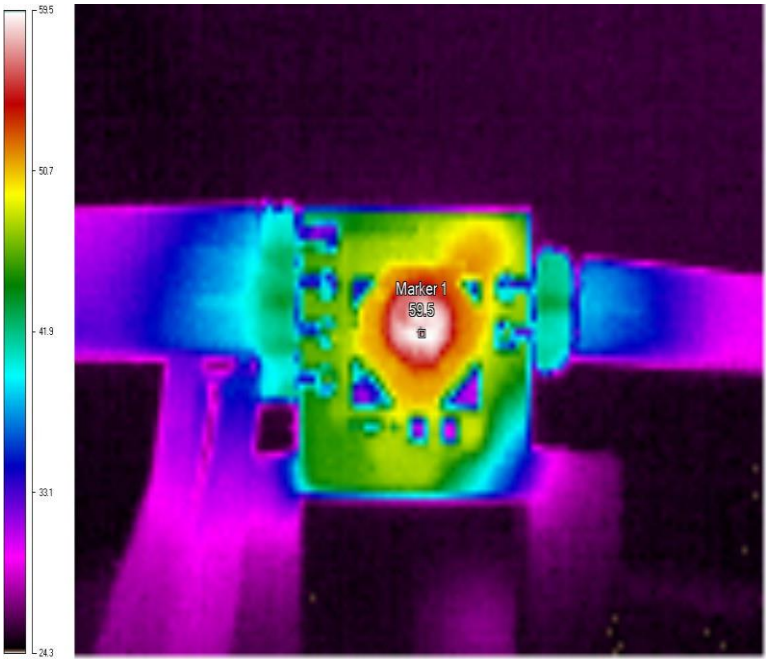


Coupled Inductor View

Thermal Image of the EVM at 18VIN &I_{PRI}=I_{SEC}=0.25A

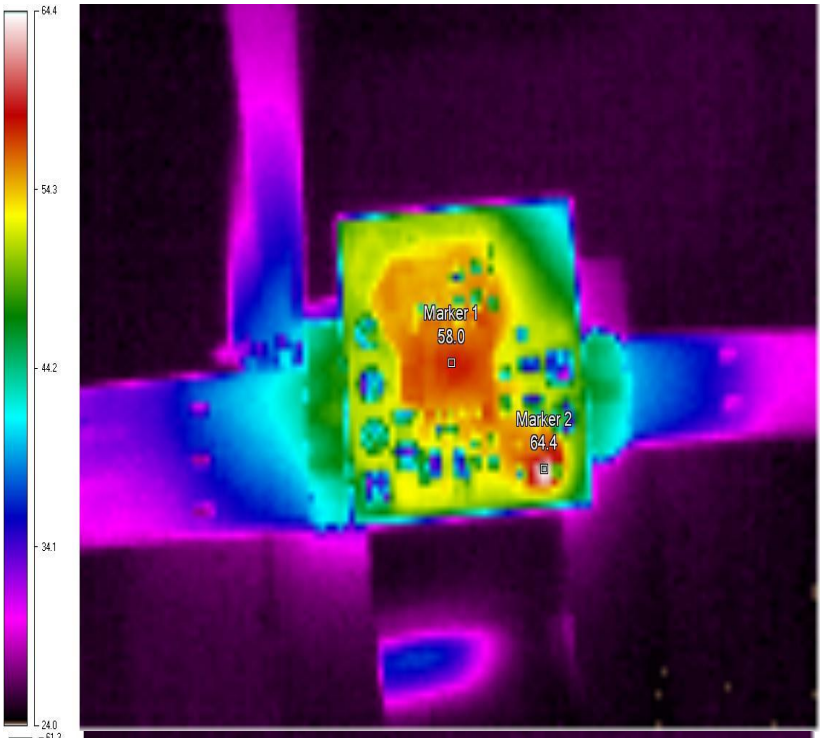


- IC view
- IC Top case temperature = 52.2 degC
- Secondary Rectifier Diode = 61.6 degC (Hottest Component)

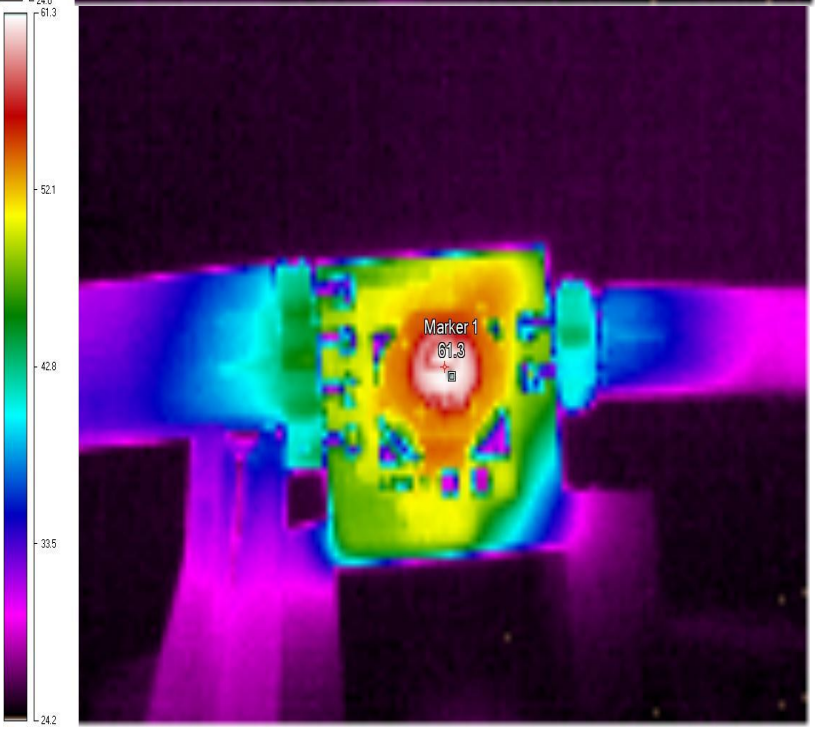


- Coupled Inductor View
- Coupled Inductor Case Temperature = 59.5 degC (Hottest Component)

Thermal Image of the EVM at 30VIN &I_{PRI}=I_{SEC}=0.25A



- IC View
- IC Top Case Temperature = 58 degC
- Secondary Rectifier Diode = 64.4 degC (Hottest Component)



- Coupled Inductor View
- Coupled Inductor Case Temperature = 61.3degC (Hottest component)

Efficiency Data

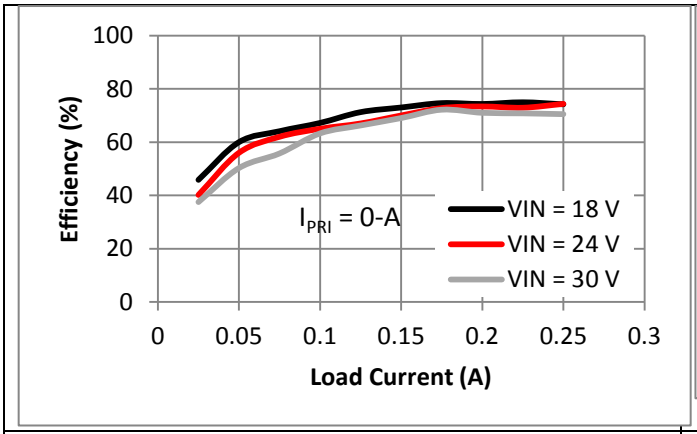


Figure 1. Efficiency with I_{PRI} set at 0A load and I_{SEC} increasing from 0.025A to 250mA

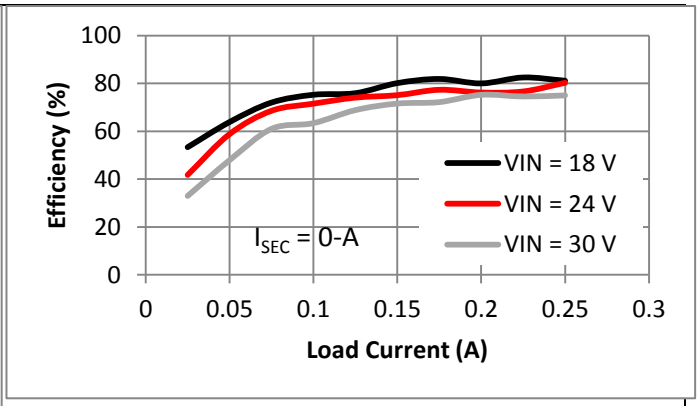


Figure 2. Efficiency with I_{SEC} set at 0A load and I_{PRI} increasing from 0.025A to 250mA

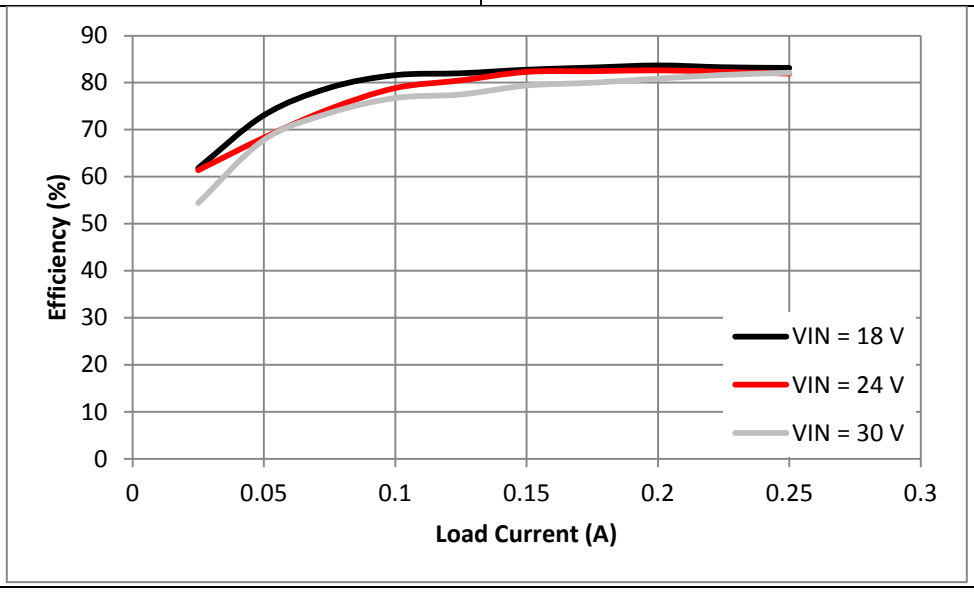


Figure 3. Efficiency with I_{PRI} = I_{SEC} = Load Current increased from 0.025A to 0.25A on each rail

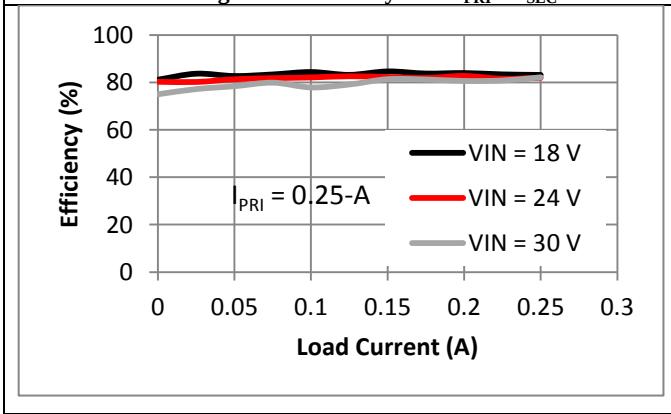


Figure 4. Efficiency with I_{PRI} set at 250mA load and I_{SEC} increasing from 0A to 250mA

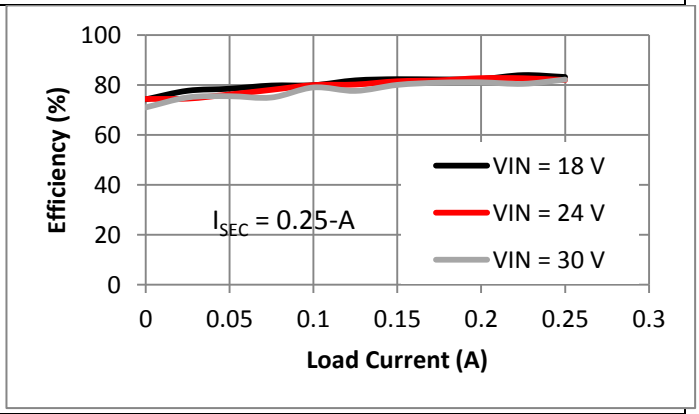


Figure 5. Efficiency with I_{SEC} set at 250mA load and I_{PRI} increasing from 0A to 250mA

Load Regulation Data

Dotted line plots (- - - -) show **V_{PRI}** and the solid line plots show **V_{SEC} (Magnitude) (unless specified otherwise).**

Legend: **Black: VIN = 18V** **Red: VIN = 24V** **Grey: VIN =30V**

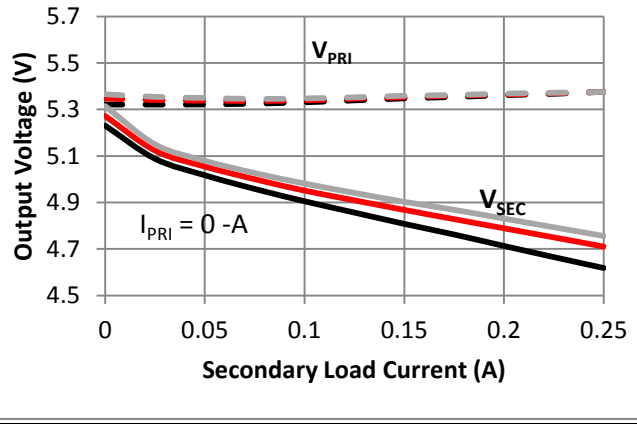


Figure 6. Load Regulation with I_{PRI} set at 0A and I_{SEC} increasing from 0A to 250mA

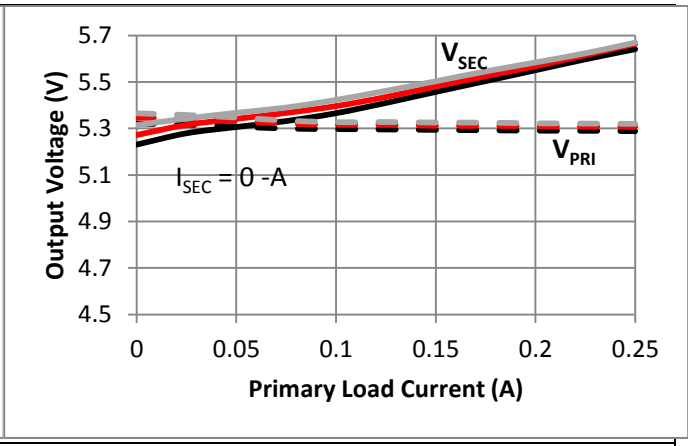


Figure 7. Load Regulation with I_{SEC} set at 0A and I_{PRI} increasing from 0A to 250mA

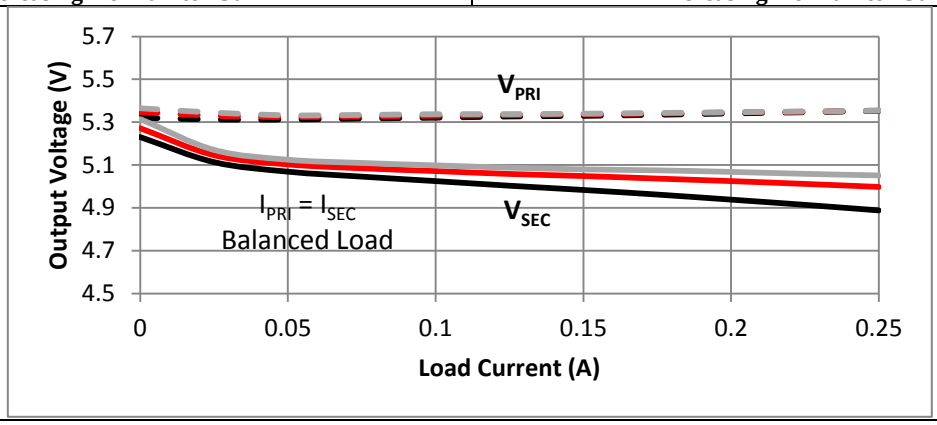


Figure 8. Load Regulation with I_{PRI} = I_{SEC} = Load Current increased from 0A to 0.25A on each rail

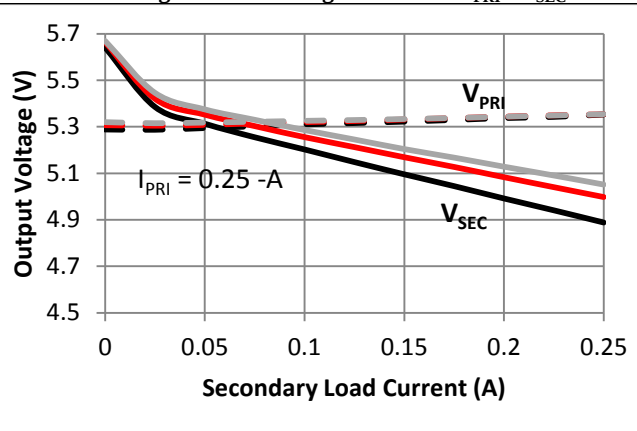


Figure 9. Load Regulation with I_{PRI} set at 250mA load and I_{SEC} increasing from 0A to 250mA

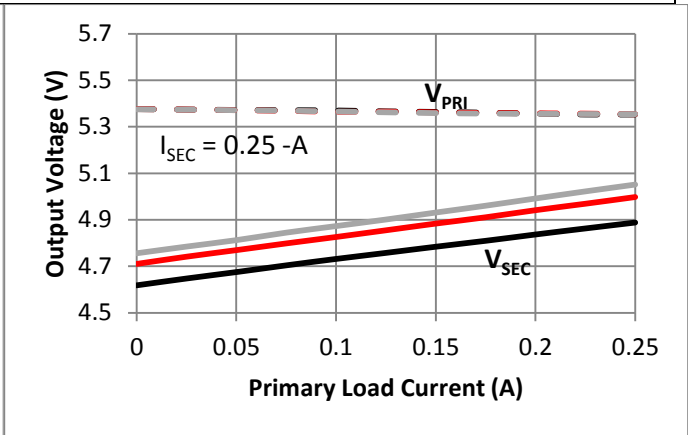


Figure 10. Load Regulation with I_{SEC} set at 250mA load and I_{PRI} increasing from 0A to 250mA

Line Regulation Data

Dotted line plots (- - - -) = **V_{PRI}** and the solid line plots = **V_{SEC} (Magnitude) (unless specified otherwise).**

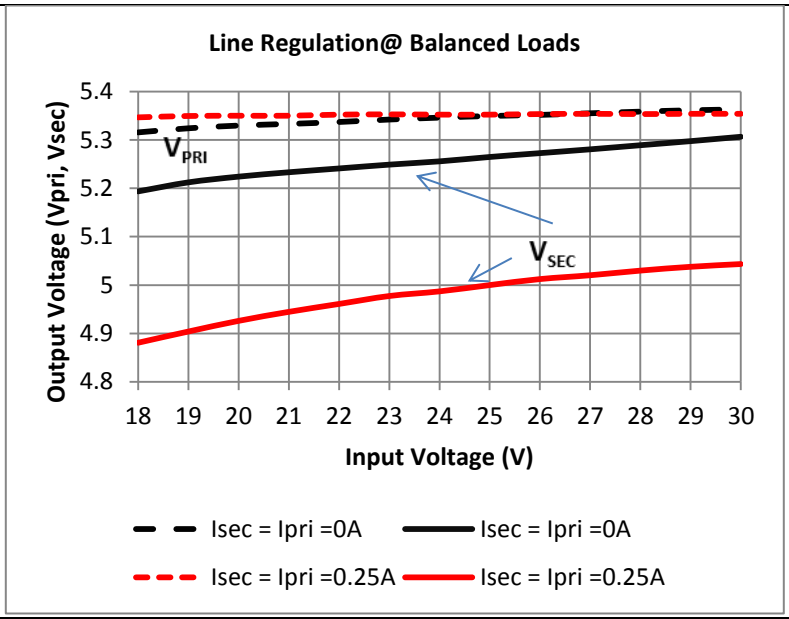


Figure 11. Line Regulation with $I_{SEC} = I_{PRI}$ (Balanced Loads)

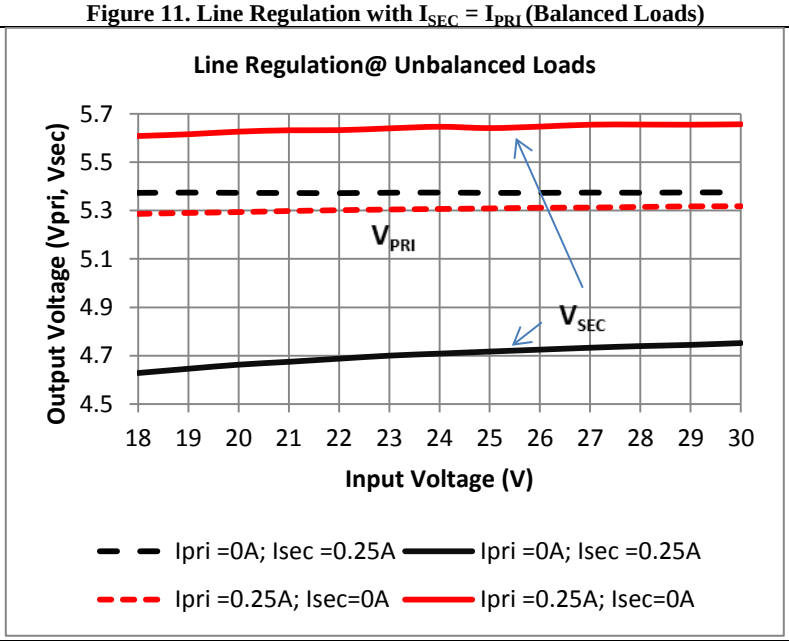


Figure 12. Line Regulation with $I_{SEC} \neq I_{PRI}$ (Unbalanced Loads; Unloaded one rail with maximum load on the other rail)

Start Up

Test condition: VIN = 24V, both outputs set at No load (0mA on Primary and Secondary).
C1 (Yellow) – VIN

C2 (Red) – I_{SEC}: Secondary DC Current

C3 (Blue) –V_{SEC} (-5.25V)

C4 (Green) –V_{PRI} (5.35V)

Figure 13. Startup at No load

Test condition: VIN = 24V, both outputs set at Full load (250mA (magnitude) on Primary and Secondary).
C1 (Yellow) – VIN

C2 (Red) – I_{SEC}: Secondary DC Current

C3 (Blue) –V_{SEC} (-5V)

C4 (Green) –V_{PRI} (5.35V)

Figure 14. Startup at Full load

Load Transients

V_{SEC} Load Step @ I_{PRI} =0-A

Test condition: VIN = 24V with I_{PRI} set to 0A**.**

CH2 (Red) - I_{SEC} = load step from 62.5mA to 187.5mA (magnitude) with slew rate set to 500mA/us

CH3 (Blue) - V_{SEC} (AC coupled); ΔV_{SEC} = 184mV peak to peak

CH4 (Green) - V_{PRI} (AC coupled); ΔV_{PRI} = 25mV peak to peak

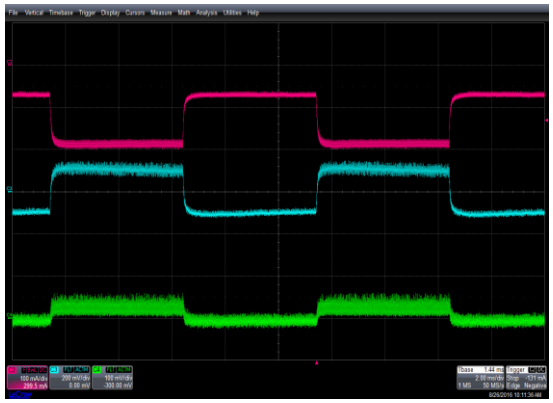


Figure 15. Secondary Side Load Transient at No load on Primary

V_{SEC} Load Step @ I_{PRI} =250-mA

Test condition: VIN = 24V with I_{PRI} set to 250mA (Maximum Load)**.**

CH2 (Red) - I_{SEC} = load step: 62.5mA to 187.5mA (magnitude) with slew rate set to 500mA/us

CH3 (Blue) - V_{SEC} (AC coupled); ΔV_{SEC} = 192mV peak to peak

CH4 (Green) - V_{PRI} (AC coupled); ΔV_{PRI} < 30mV peak to peak

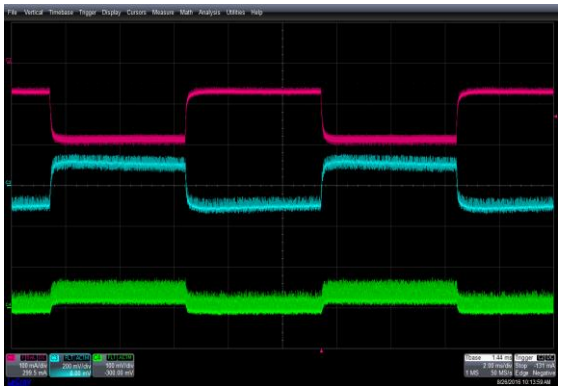


Figure 16. Secondary Side Load Transient at 250mA load on Primary

V_{PRI} Load Step @ I_{SEC} =0-A

Test condition: VIN = 24V with I_{SEC} set to 0A

CH2 (Red) - $I_{PRI:}$ load step: 62.5mA to 187.5mA with slew rate set to 500mA/us

CH3 (Blue) - V_{SEC} (AC coupled); ΔV_{SEC} = 170mV peak to peak

CH4 (Green) - V_{PRI} (AC coupled); ΔV_{PRI} = 10mV peak to peak

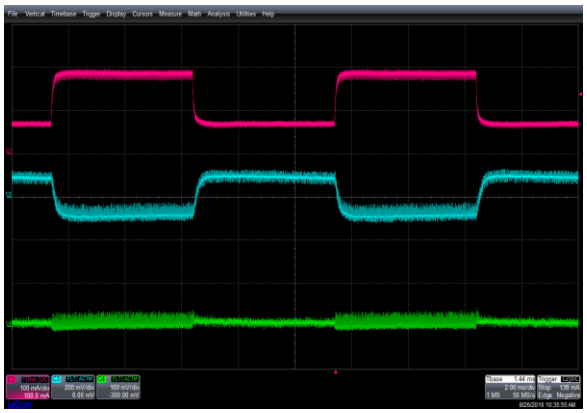


Figure 17. Primary Side Load Transient at no load on Secondary

V_{PRI} Load Step@ I_{SEC} =250-mA

Test condition: VIN = 24V with I_{SEC} set to 250mA (Maximum Load)

CH2 (Red) - I_{PRI}: load step: 62.5mA to 187.5mA with slew rate set to 500mA/us

CH3 (Blue) - V_{SEC} (AC coupled); ΔV_{SEC} = 120mV peak to peak

CH4 (Green) - V_{PRI} (AC coupled); ΔV_{PRI} < 15mV peak to peak

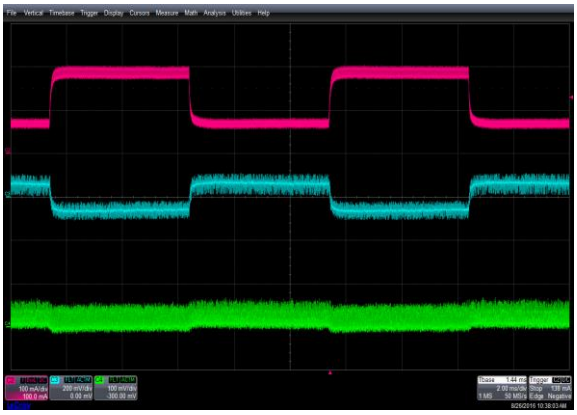


Figure 18. Primary Side Load Transient at 250mA load on Secondary

SW Node and Output Voltage Ripple Waveforms

Test condition: VIN = 24V, both outputs set to full load (250mA on Primary and on Secondary).

M1 (Yellow) - Switch node (475 kHz)

C2 (Red) - I_{SEC}: Secondary DC Current

C3 (Blue) - V_{SEC} (AC coupled): ΔV_{SEC} = 35mV peak to peak

C4 (Green) - V_{PRI} (AC coupled): ΔV_{PRI} = 50mV peak to peak

Figure 19. Steady State at Full Load

Short Circuit Test

Secondary Side Short Circuit Test

C1 (Yellow) – VIN

C2 (Red) – I_{SEC}: Secondary DC current

C3 (Blue) – V_{SEC}

C4 (Green) – V_{PRI}

Test condition: VIN = 24V, and both outputs were set to no load (0A on Primary and Secondary).

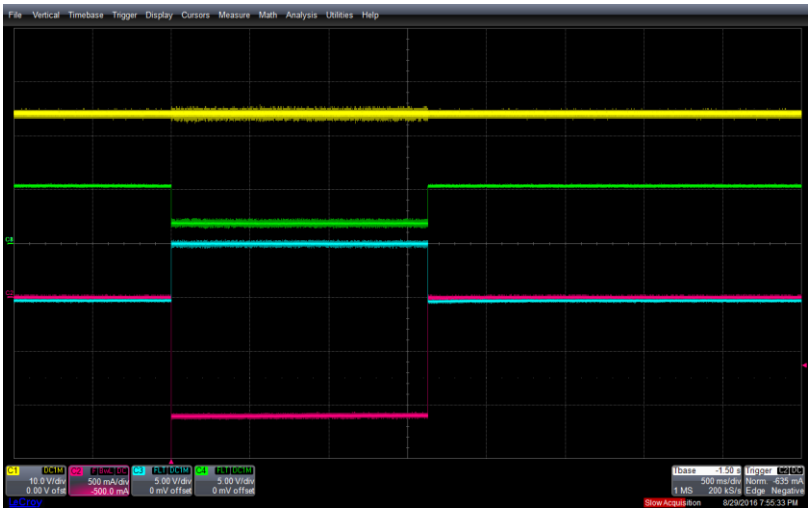


Figure 20. Secondary Short with both output rails unloaded

Test condition: VIN = 24V, with I_{SEC} = I_{PRI} set to 250mA (Maximum Load)

Figure 21. Secondary Short with both rails fully loaded

Primary Side Short Circuit Test

C1 (Yellow) – VIN

C2 (Red) – I_{PRI}: Primary DC current

C3 (Blue) – V_{SEC}

C4 (Green) – V_{PRI}

Test condition: VIN = 24V, and both outputs were set to no load (0A on Primary and Secondary).

Figure 22. Primary Short with both output rails unloaded

Test condition: VIN = 24V, with I_{SEC} = I_{PRI} set to 250mA (Maximum Load)

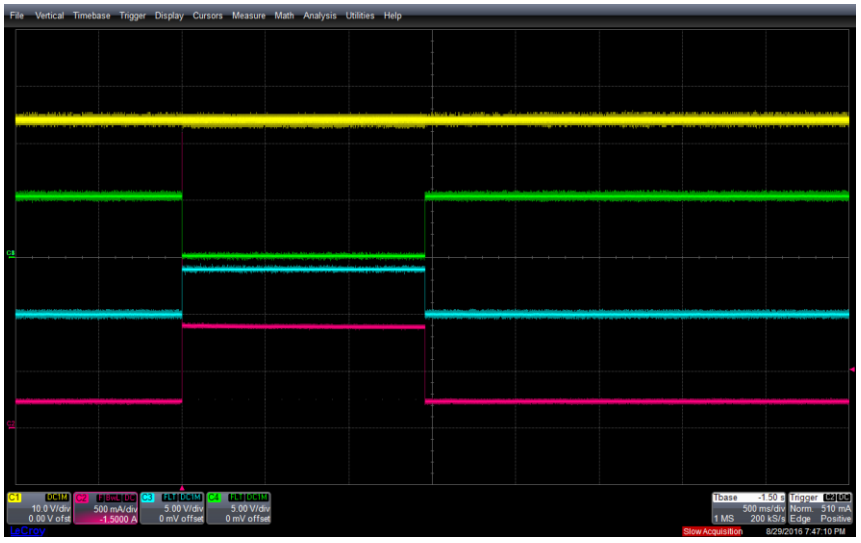


Figure 23. Primary Short with both output rails fully loaded

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