# ISO5451-Q1 具有有源安全特性的高 CMTI 2.5A/5A 隔离式 IGBT、MOSFET 栅极驱动器

## 1 特性

- 适用于汽车电子 应用
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 1 级：-40°C 至 125°C 的环境运行温度范围
  - 器件人体模型 (HBM) 分类等级 3A
  - 器件充电器件模型 (CDM) 分类等级 C6
- 在 $V_{CM}$ = 1500V 时，共模瞬态抗扰度 (CMTI) 的最小值为 50kV/µs，典型值为 100kV/µs
- 2.5A 峰值拉电流和 5A 峰值灌电流
- 短暂传播延迟：76ns（典型值），110ns（最大值）
- 2A 有源米勒钳位
- 输出短路钳位
- 在检测到去饱和故障时通过 $\overline{FLT}$ 发出故障报警，并通过 $\overline{RST}$ 复位
- 具有就绪 (RDY) 引脚指示的输入和输出欠压锁定 (UVLO)
- 有源输出下拉特性，在低电源或输入悬空的情况下默认输出低电平
- 3V 至 5.5V 输入电源电压
- 15V 至 30V 输出驱动器电源电压
- 互补金属氧化物半导体 (CMOS) 兼容输入
- 抑制短于 20ns 的输入脉冲和瞬态噪声
- 可承受的浪涌隔离电压达 10000$V_{PK}$
- 安全及管理认证：
  - 符合 DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 标准的 8000 $V_{PK}$ $V_{IOTM}$ 和 1420 $V_{PK}$ $V_{IORM}$ 增强型隔离
  - 符合 UL 1577 且长达 1 分钟的 5700$V_{RMS}$ 隔离
  - CSA 组件验收通知 5A、IEC 60950-1 和 IEC 60601-1 终端设备标准
  - 符合 EN 61010-1 和 EN 60950-1 标准的 TUV 认证
  - GB4943.1-2011 CQC 认证
  - 已通过 UL、VDE、CQC、TUV 认证并规划进行 CSA 认证

## 2 应用

- 隔离式绝缘栅双极型晶体管 (IGBT) 和金属氧化物半导体场效应晶体管 (MOSFET) 驱动器：
  - 混合动力汽车 (HEV) 和电动车 (EV) 电源模块
  - 工业电机控制驱动
  - 工业电源
  - 太阳能逆变器
  - 感应加热

## 3 说明

ISO5451-Q1 是一款用于 IGBT 和 MOSFET 的 5.7 $kV_{RMS}$ 增强型隔离栅极驱动器，具有 2.5A 的拉电流能力和 5A 的灌电流能力。输入端由 3V 至 5.5V 的单电源供电运行。输出端允许的电源范围为 15V 至 30V。两个互补 CMOS 输入控制栅极驱动器的输出状态。76ns 的短暂传播时间保证了对于输出级的精确控制。

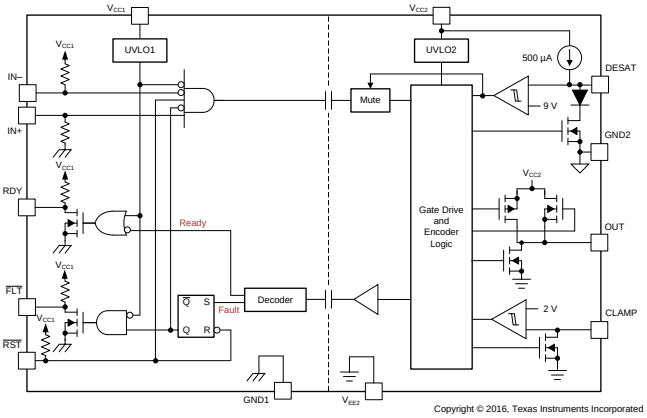
内置的去饱和 (DESAT) 故障检测功能可识别 IGBT 何时处于过载状态。当检测到 DESAT 时，栅极驱动器输出会被拉低为 $V_{EE2}$ 电势，从而将 IGBT 立即关断。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| ISO5451-Q1 | SOIC (16) | 10.30mm x 7.50mm |

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

功能方框图



# 目录



## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

| 日期 | 修订版本 | 注释 |
|---|---|---|
| 2016 年 9 月 | * | 最初发布版本 |

## 5 说明 （续）

当发生去饱和故障时，器件会通过隔离隔栅发送故障信号，以将输入端的 $\overline{\text{FLT}}$ 输出拉为低电平并阻断隔离器的输入。$\overline{\text{FLT}}$ 的输出状态将被锁存，可通过 $\overline{\text{RST}}$ 输入上的低电平有效脉冲复位。

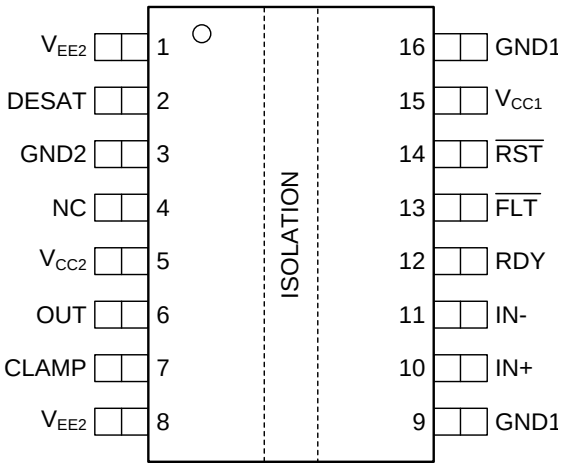
如果在由双极输出电源供电的正常运行期间关断 IGBT，输出电压会被硬钳位为 $V_{EE2}$。如果输出电源为单极，那么可采用有源米勒钳位，这种钳位会在一条低阻抗路径上灌入米勒电流，从而防止 IGBT 在高电压瞬态条件下发生动态导通。

栅极驱动器是否准备就绪待运行由两个欠压锁定电路控制，这两个电路会监视输入端和输出端的电源。如果任意一端电源不足，RDY 输出会变为低电平，否则该输出为高电平。

ISO5451-Q1 采用 16 引脚小外形尺寸集成电路 (SOIC) 封装。此器件的额定工作环境温度范围为 -40°C 至 125°C。

## 6 Pin Configuration and Function

**DW Package**
**16-Pin SOIC**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $V_{EE2}$ | 1, 8 | - | Output negative supply. Connect to GND2 for Unipolar supply application. |
| DESAT | 2 | I | Desaturation voltage input |
| GND2 | 3 | - | Gate drive common. Connect to IGBT emitter. |
| NC | 4 | - | Not connected |
| $V_{CC2}$ | 5 | - | Most positive output supply potential. |
| OUT | 6 | O | Gate drive voltage output |
| CLAMP | 7 | O | Miller clamp output |
| GND1 | 9, 16 | - | Input ground |
| IN+ | 10 | I | Non-inverting gate drive voltage control input |
| IN- | 11 | I | Inverting gate drive voltage control input |
| RDY | 12 | O | Power-good output, active high when both supplies are good. |
| $\overline{\text{FLT}}$ | 13 | O | Fault output, low-active during DESAT condition |
| $\overline{\text{RST}}$ | 14 | I | Reset input, apply a low pulse to reset fault latch. |
| $V_{CC1}$ | 15 | - | Positive input supply (3 V to 5.5 V) |

# 7 Specifications

## 7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC1}$ | Supply voltage input side | | GND1 - 0.3 | 6 | V |
| $V_{CC2}$ | Positive supply voltage output side | ($V_{CC2}$ – GND2) | –0.3 | 35 | V |
| $V_{EE2}$ | Negative supply voltage output side | ($V_{EE2}$ – GND2) | –17.5 | 0.3 | V |
| $V_{(SUP2)}$ | Total supply output voltage | ($V_{CC2}$ - $V_{EE2}$) | –0.3 | 35 | V |
| $V_{OUT}$ | Gate driver output voltage | | $V_{EE2}$ - 0.3 | $V_{CC2}$ + 0.3 | V |
| $I_{(OUTH)}$ | Gate driver high output current | Gate driver high output current (max pulse width = 10 μs, max duty cycle = 0.2%) | | 2.7 | A |
| $I_{(OUTL)}$ | Gate driver low output current | | | 5.5 | A |
| $V_{(LIP)}$ | Voltage at IN+, IN-, $\overline{FLT}$, RDY, $\overline{RST}$ | | GND1 - 0.3 | $V_{CC1}$ + 0.3 | V |
| $I_{(LOP)}$ | Output current of $\overline{FLT}$, RDY | | | 10 | mA |
| $V_{(DESAT)}$ | Voltage at DESAT | | GND2 - 0.3 | $V_{CC2}$ + 0.3 | V |
| $V_{(CLAMP)}$ | Clamp voltage | | $V_{EE2}$ - 0.3 | $V_{CC2}$ + 0.3 | V |
| $T_J$ | Junction temperature | | –40 | 150 | °C |
| $T_{STG}$ | Storage temperature | | -65 | 150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±4000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±1500 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC1}$ | Supply voltage input side | 3 | | 5.5 | V |
| $V_{CC2}$ | Positive supply voltage output side ($V_{CC2}$ – GND2) | 15 | | 30 | V |
| $V_{EE2}$ | Negative supply voltage output side ($V_{EE2}$ – GND2) | –15 | | 0 | V |
| $V_{(SUP2)}$ | Total supply voltage output side ($V_{CC2}$ – $V_{EE2}$) | 15 | | 30 | V |
| $V_{IH}$ | High-level input voltage (IN+, IN-, $\overline{RST}$) | 0.7 x $V_{CC1}$ | | $V_{CC1}$ | V |
| $V_{IL}$ | Low-level input voltage (IN+, IN-, $\overline{RST}$) | 0 | | 0.3 x $V_{CC1}$ | V |
| $t_{UI}$ | Pulse width at IN+, IN- for full output ($C_{LOAD}$ = 1nF) | 40 | | | ns |
| $t_{RST}$ | Pulse width at $\overline{RST}$ for resetting fault latch | 800 | | | ns |
| $T_A$ | Ambient temperature | -40 | 25 | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | DW (SOIC) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 99.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 48.5 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 56.5 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 29.2 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 56.5 | |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Power Rating

| | | VALUE | UNIT |
|---|---|---|---|
| $P_D$ | Maximum power dissipation(1) | 1255 | mW |
| $P_{ID}$ | Maximum input power dissipation | 175 | |
| $P_{OD}$ | Maximum output power dissipation | 1080 | |

(1) Full chip power dissipation is de-rated 10.04 mW/°C beyond 25°C ambient temperature. At 125°C ambient temperature, a maximum of 251 mW total power dissipation is allowed. Power dissipation can be optimized depending on ambient temperature and board design, while ensuring that Junction temperature does not exceed 150°C.

## 7.6 Insulation Characteristics

| PARAMETER | | TEST CONDITIONS | SPECIFICATION | UNIT |
|---|---|---|---|---|
| CLR | External clearance(1) | Shortest terminal-to-terminal distance through air | >8 | mm |
| CPG | External creepage(1) | Shortest terminal-to-terminal distance across the package surface | >8 | mm |
| DTI | Distance through the insulation | Minimum internal gap (internal clearance) | >21 | μm |
| CTI | Tracking resistance (comparative tracking index) | DIN EN 60112 (VDE 0303-11); IEC 60112; | >600 | V |
| | Material Group | According to IEC 60664-1; UL 746A | I | |
| | Overvoltage category (according to IEC 60664-1) | Rated Mains Voltage ≤ 300 $V_{RMS}$ | I-IV | |
| | | Rated Mains Voltage ≤ 600 $V_{RMS}$ | I-III | |
| | | Rated Mains Voltage ≤ 1000 $V_{RMS}$ | I-II | |
| **DIN V VDE V 0884-10 (VDE V 0884-10):2006-12**(2) | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | AC voltage (bipolar) | 1420 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum isolation working voltage | AC voltage. Time dependent dielectric breakdown (TDDB) Test, see Figure 1 | 1000 | $V_{RMS}$ |
| | | DC voltage | 1420 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum Transient isolation voltage | $V_{TEST} = V_{IOTM}$, t = 60 sec (qualification), t = 1 sec (100% production) | 8000 | $V_{PK}$ |
| $V_{IOSM}$ | Maximum surge isolation voltage(3) | Test method per IEC 60065, 1.2/50 μs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 10000\ V_{PK}$ (qualification)(3) | 6250 | |
| $q_{pd}$ | Apparent charge(4) | Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 1704\ V_{PK}$, $t_m$ = 10 s | ≤5 | pC |
| | | Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM} = 2272\ V_{PK}$, $t_m$ = 10 s | ≤5 | |
| | | Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IOTM}$, $t_{ini}$ = 60 s; $V_{pd(m)} = 1.875 \times V_{IORM} = 2663\ V_{PK}$, $t_m$ = 10 s | ≤5 | |
| $R_{IO}$ | Isolation resistance, input to output(5) | $V_{IO}$ = 500 V, $T_A$ = 25°C | > $10^{12}$ | Ω |
| | | $V_{IO}$ = 500 V, 100°C ≤ $T_A$ ≤ 125°C | > $10^{11}$ | Ω |
| | | $V_{IO}$ = 500 V at $T_S$ = 150°C | > $10^9$ | Ω |
| $C_{IO}$ | Barrier capacitance, input to output(5) | $V_{IO}$ = 0.4 x sin (2πft), f = 1 MHz | 1 | pF |
| | Pollution degree | | 2 | |
| **UL 1577** | | | | |
| $V_{ISO}$ | Withstanding Isolation voltage | $V_{TEST} = V_{ISO}$, t = 60 sec (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6840\ V_{RMS}$, t = 1 sec (100% production) | 5700 | $V_{RMS}$ |

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for basic electrical insulation only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device

## 7.7 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_S$ | Safety input, output or supply current | $\theta_{JA}$ = 99.6°C/W, $V_I$ = 3.6 V, $T_J$ = 150°C, $T_A$ = 25°C | | | 349 | mA |
| | | $\theta_{JA}$ = 99.6°C/W, $V_I$ = 5.5 V, $T_J$ = 150°C, $T_A$ = 25°C | | | 228 | |
| | | $\theta_{JA}$ = 99.6°C/W, $V_I$ = 15 V, $T_J$ = 150°C, $T_A$ = 25°C | | | 84 | |
| | | $\theta_{JA}$ = 99.6°C/W, $V_I$ = 30 V, $T_J$ = 150°C, $T_A$ = 25°C | | | 42 | |
| $P_S$ | Safety input, output, or total power | $\theta_{JA}$ = 99.6°C/W, $T_J$ = 150°C, $T_A$ = 25°C | | | 1255(1) | |
| $T_S$ | Maximum ambient safety temperature | | | | 150 | °C |

(1) Input, output, or the sum of input and output power should not exceed this value

## 7.8 Safety-Related Certifications

over operating free-air temperature range (unless otherwise noted)

| VDE | CSA | UL | CQC | TUV |
|---|---|---|---|---|
| Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 60950-1 (VDE 0805 Teil 1):2011-01 | Plan to certify under CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 60601-1 | Certified according to UL 1577 Component Recognition Program | Certified according to GB 4943.1-2011 | Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 |
| Reinforced Insulation Maximum Transient isolation voltage, 8000 $V_{PK}$; Maximum surge isolation voltage, 6250 $V_{PK}$, Maximum repetitive peak isolation voltage, 1420 $V_{PK}$ | Isolation Rating of 5700 $V_{RMS}$; Reinforced insulation per CSA 60950- 1- 07+A1+A2 and IEC 60950-1 (2nd Ed.), 800 $V_{RMS}$ max working voltage (pollution degree 2, material group I) ; 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 $V_{RMS}$ (354 $V_{PK}$) max working voltage | Single Protection, 5700 $V_{RMS}$ (1) | Reinforced Insulation, Altitude ≤ 5000m, Tropical climate, 400 $V_{RMS}$ maximum working voltage | 5700 $V_{RMS}$ Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 $V_{RMS}$ 5700 $V_{RMS}$ Reinforced insulation per EN 60950-1:2006/A11:2009/A1:2010/A12:2011/A2:2013 up to working voltage of 800 $V_{RMS}$ |
| Certification completed Certificate number: 40040142 | Certification planned | Certification completed File number: E181974 | Certification completed Certificate number: CQC16001141761 | Certification completed Client ID number: 77311 |

(1) Production tested ≥ 6840 $V_{RMS}$ for 1 second in accordance with UL 1577.

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed in the High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

## 7.9 Electrical Characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at $T_A$ = 25°C, $V_{CC1}$ = 5 V, $V_{CC2}$ – GND2 = 15 V, GND2 – $V_{EE2}$ = 8 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VOLTAGE SUPPLY** | | | | | | |
| $V_{IT+(UVLO1)}$ | Positive-going UVLO1 threshold voltage input side ($V_{CC1}$ – GND1) | | | | 2.25 | V |
| $V_{IT-(UVLO1)}$ | Negative-going UVLO1 threshold voltage input side ($V_{CC1}$ – GND1) | | 1.7 | | | V |
| $V_{HYS(UVLO1)}$ | UVLO1 Hysteresis voltage ($V_{IT+}$ – $V_{IT–}$) input side | | | 0.24 | | V |
| $V_{IT+(UVLO2)}$ | Positive-going UVLO2 threshold voltage output side ($V_{CC2}$ – GND2) | | | 12 | 13 | V |
| $V_{IT-(UVLO2)}$ | Negative-going UVLO2 threshold voltage output side ($V_{CC2}$ – GND2) | | 9.5 | 11 | | V |
| $V_{HYS(UVLO2)}$ | UVLO2 Hysteresis voltage ($V_{IT+}$ – $V_{IT–}$) output side | | | 1 | | V |
| $I_{Q1}$ | Input supply quiescent current | | | 2.8 | 4.5 | mA |
| $I_{Q2}$ | Output supply quiescent current | | | 3.6 | 6 | mA |
| **LOGIC I/O** | | | | | | |
| $V_{IT+(IN,\overline{RST})}$ | Positive-going input threshold voltage (IN+, IN-, $\overline{RST}$) | | | | 0.7 x $V_{CC1}$ | V |
| $V_{IT-(IN,\overline{RST})}$ | Negative-going input threshold voltage (IN+, IN-, $\overline{RST}$) | | 0.3 x $V_{CC1}$ | | | V |
| $V_{HYS(IN,\overline{RST})}$ | Input hysteresis voltage (IN+, IN-, $\overline{RST}$) | | | 0.15 x $V_{CC1}$ | | V |
| $I_{IH}$ | High-level input leakage at (IN+) (1) | IN+ = $V_{CC1}$ | | 100 | | µA |
| $I_{IL}$ | Low-level input leakage at (IN-, $\overline{RST}$) (2) | IN- = GND1, $\overline{RST}$ = GND1 | | -100 | | µA |
| $I_{PU}$ | Pull-up current of $\overline{FLT}$, RDY | $V_{(RDY)}$ = GND1, $V_{(FLT)}$ = GND1 | | 100 | | µA |
| $V_{OL}$ | Low-level output voltage at $\overline{FLT}$, RDY | $I_{(FLT)}$ = 5 mA | | | 0.2 | V |
| **GATE DRIVER STAGE** | | | | | | |
| $V_{(OUTPD)}$ | Active output pull-down voltage | $I_{OUT}$ = 200 mA, $V_{CC2}$ = open | | | 2 | V |
| $V_{(OUTH)}$ | High-level output voltage | $I_{OUT}$ = –20 mA | $V_{CC2}$ - 0.5 | $V_{CC2}$ - 0.24 | | V |
| $V_{(OUTL)}$ | Low-level output voltage | $I_{OUT}$ = 20 mA | | $V_{EE2}$ + 13 | $V_{EE2}$ + 50 | mV |
| $I_{(OUTH)}$ | High-level output peak current | IN+ = high, IN- = low, $V_{OUT}$ = $V_{CC2}$ - 15 V | 1.5 | 2.5 | | A |
| $I_{(OUTL)}$ | Low-level output peak current | IN+ = low, IN- = high, $V_{OUT}$ = $V_{EE2}$ + 15 V | 3.4 | 5 | | A |
| **ACTIVE MILLER CLAMP** | | | | | | |
| $V_{(CLP)}$ | Low-level clamp voltage | $I_{(CLP)}$ = 20 mA | | $V_{EE2}$ + 0.015 | $V_{EE2}$ + 0.08 | V |
| $I_{(CLP)}$ | Low-level clamp current | $V_{(CLAMP)}$ = $V_{EE2}$ + 2.5 V | 1.6 | 2.5 | | A |
| $V_{(CLTH)}$ | Clamp threshold voltage | | 1.6 | 2.1 | 2.5 | V |
| **SHORT CIRCUIT CLAMPING** | | | | | | |
| $V_{(CLP\_OUT)}$ | Clamping voltage ($V_{OUT}$ - $V_{CC2}$) | IN+ = high, IN- = low, $t_{CLP}$=10 µs, $I_{(OUTH)}$ = 500 mA | | 0.8 | 1.3 | V |
| $V_{(CLP\_CLAMP)}$ | Clamping voltage ($V_{CLP}$ - $V_{CC2}$) | IN+ = high, IN- = low, $t_{CLP}$=10 µs, $I_{(CLP)}$ = 500 mA | | 1.3 | | V |
| $V_{(CLP\_CLAMP)}$ | Clamping voltage at CLAMP | IN+ = High, IN- = Low, $I_{(CLP)}$ = 20 mA | | 0.7 | 1.1 | V |
| **DESAT PROTECTION** | | | | | | |
| $I_{(CHG)}$ | Blanking capacitor charge current | $V_{(DESAT)}$ - GND2 = 2 V | 0.42 | 0.5 | 0.58 | mA |
| $I_{(DCHG)}$ | Blanking capacitor discharge current | $V_{(DESAT)}$ - GND2 = 6 V | 9 | 14 | | mA |
| $V_{(DSTH)}$ | DESAT threshold voltage with respect to GND2 | | 8.3 | 9 | 9.5 | V |
| $V_{(DSL)}$ | DESAT voltage with respect to GND2, when OUT is driven low | | 0.4 | | 1 | V |

(1) $I_{IH}$ for IN-, RST pin is zero as they are pulled high internally.
(2) $I_{IL}$ for IN+ is zero, as it is pulled low internally.

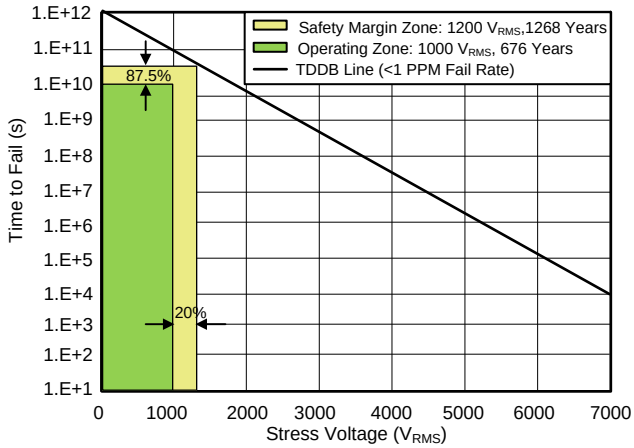
## 7.10 Switching Characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at $T_A$ = 25°C, $V_{CC1}$ = 5 V, $V_{CC2}$ – GND2 = 15 V, GND2 – $V_{EE2}$ = 8 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_r$ | Output signal rise time | $C_{LOAD}$ = 1 nF, see Figure 38, Figure 39 and Figure 40 | 12 | 20 | 35 | ns |
| $t_f$ | Output signal fall time | | 12 | 20 | 37 | ns |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay | | | 76 | 110 | ns |
| $t_{sk-p}$ | Pulse Skew $\lvert t_{PHL} - t_{PLH} \rvert$ | | | | 20 | ns |
| $t_{sk-pp}$ | Part-to-part skew | | | | 30 (1) | ns |
| $t_{GF}$ | Glitch filter on IN+, IN-, $\overline{RST}$ | | 20 | 30 | 40 | ns |
| $t_{DESAT\ (10\%)}$ | DESAT sense to 10% OUT delay | | 300 | 415 | 500 | ns |
| $t_{DESAT\ (GF)}$ | DESAT glitch filter delay | | | 330 | | ns |
| $t_{DESAT\ (\overline{FLT})}$ | DESAT sense to $\overline{FLT}$-low delay | see Figure 40 | | 2000 | 2420 | ns |
| $t_{LEB}$ | Leading edge blanking time | see Figure 38 and Figure 39 | 330 | 400 | 500 | ns |
| $t_{GF(RSTFLT)}$ | Glitch filter on $\overline{RST}$ for resetting $\overline{FLT}$ | | 300 | | 800 | ns |
| $C_I$ | Input capacitance (2) | $V_I = V_{CC1}/2 + 0.4 \times \sin(2\pi ft)$, f = 1 MHz, $V_{CC1}$ = 5 V | | 2 | | pF |
| CMTI | Common-mode transient immunity | $V_{CM}$ = 1500 V, see Figure 41 | 50 | 100 | | kV/µs |

(1) Measured at same supply voltage and temperature condition
(2) Measured from input pin to ground.

## 7.11 Safety and Insulation Characteristics Curves




$T_A$ upto 150°C Stress-voltage frequency = 60 Hz

**Figure 1. Reinforced High-Voltage Capacitor Life Time Projection**

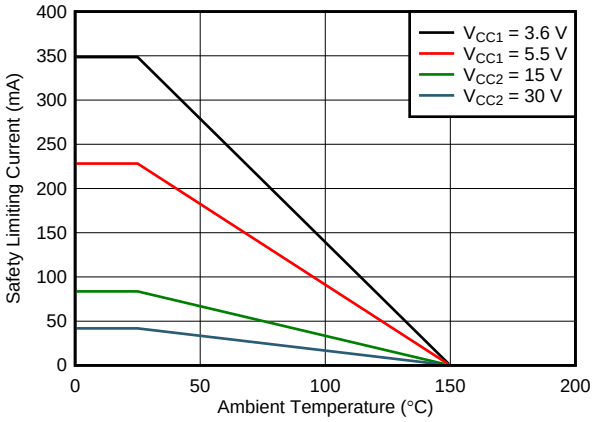



**Figure 2. Thermal Derating Curve for Safety Limiting Current per VDE**

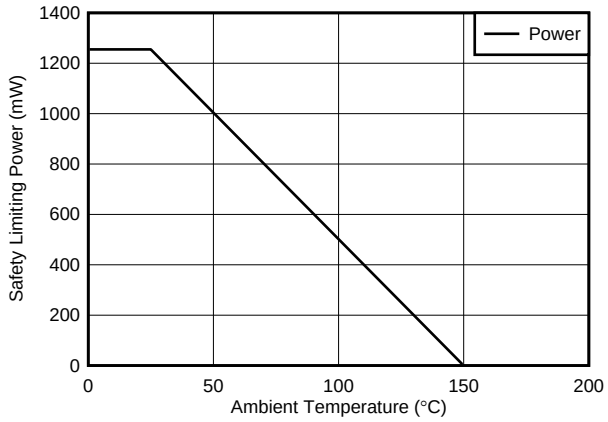
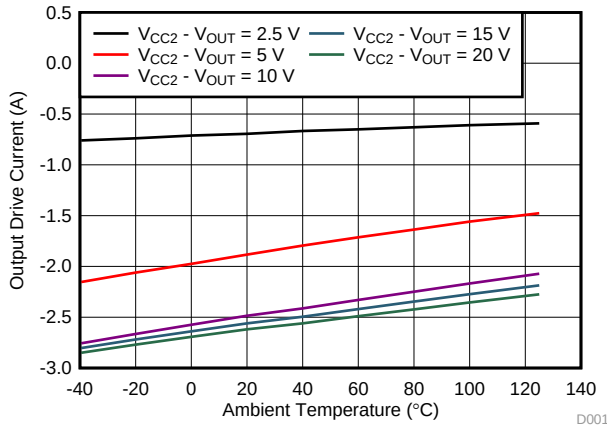


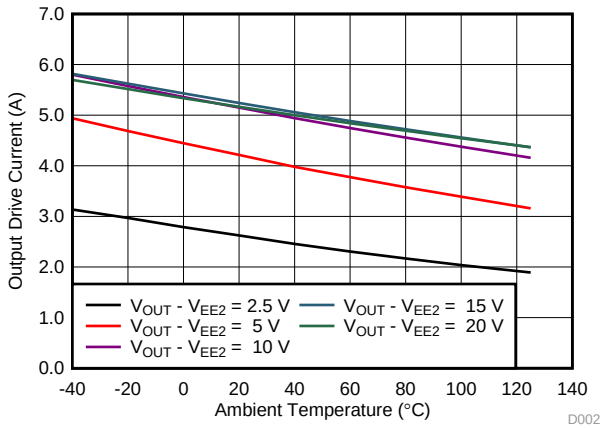

**Figure 3. Thermal Derating Curve for Safety Limiting Power per VDE**

## 7.12 Typical Characteristics




$V_{CC2}$ = 30 V

**Figure 4. Output High Drive Current vs Temperature**




$V_{CC2}$ = 30 V

**Figure 5. Output Low Drive Current vs Temperature**

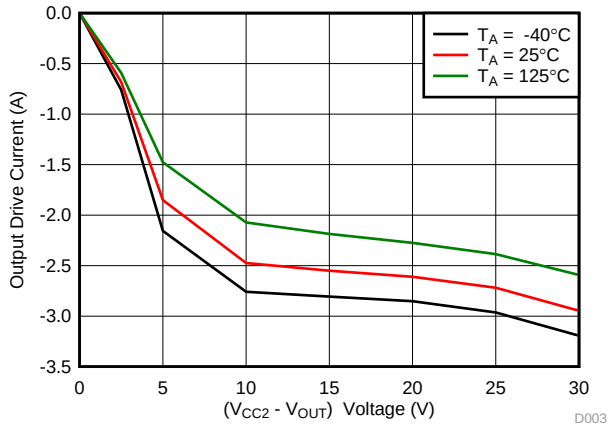



**Figure 6. Output High Drive Current vs Output Voltage**

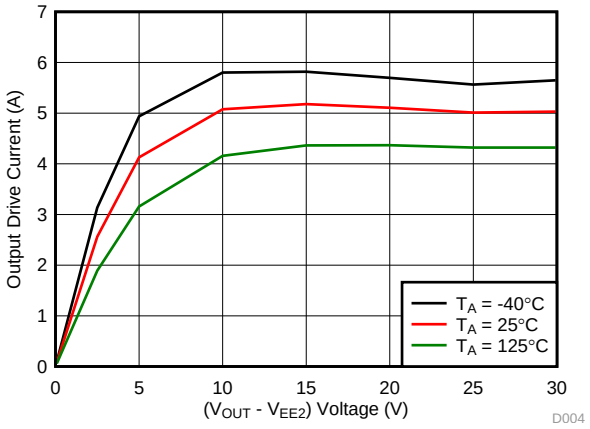
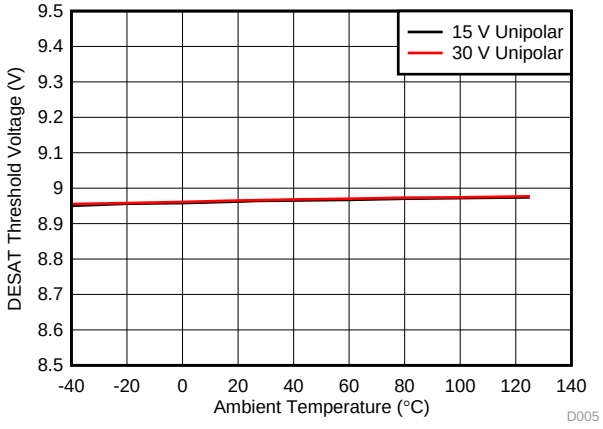


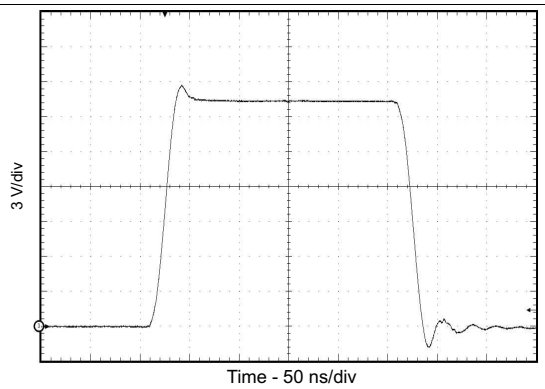

**Figure 7. Output Low Drive Current vs Output Voltage**




Unipolar: $V_{CC2}$ - $V_{EE2}$ = $V_{CC2}$ - GND2

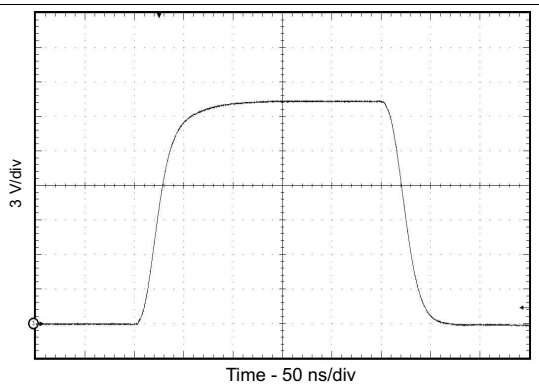
**Figure 8. DESAT Threshold Voltage vs Temperature**

## Typical Characteristics (continued)



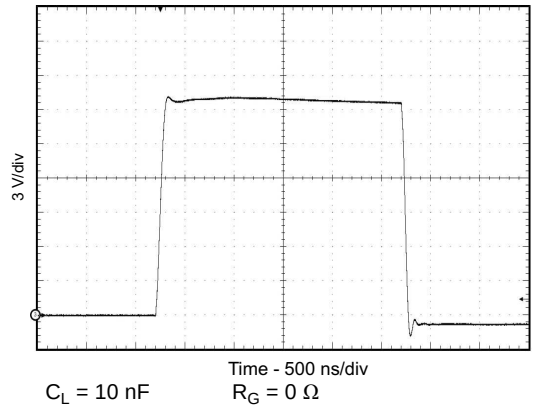

$C_L$ = 1 nF $R_G$ = 0 Ω
$V_{CC2}$ - $V_{EE2}$ = $V_{CC2}$ - GND2 = 20 V

**Figure 9. Output Transient Waveform**



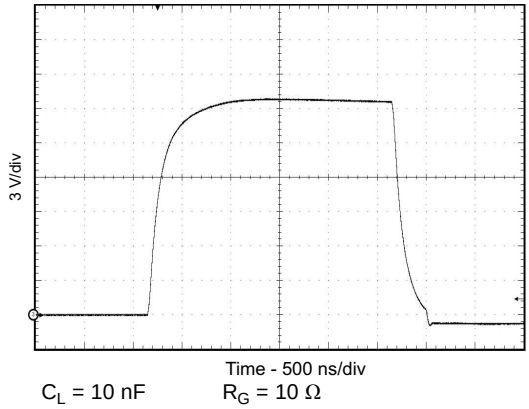

$C_L$ = 1 nF $R_G$ = 10 Ω
$V_{CC2}$ - $V_{EE2}$ = $V_{CC2}$ - GND2 = 20 V

**Figure 10. Output Transient Waveform**



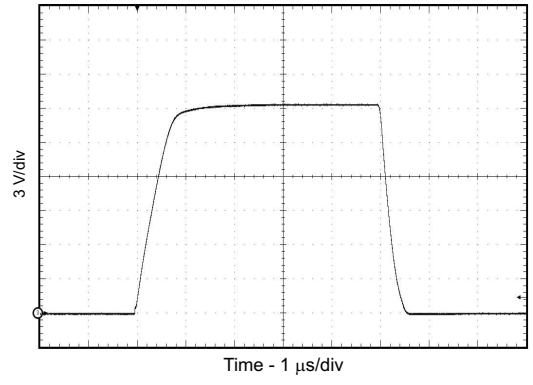

$C_L$ = 10 nF $R_G$ = 0 Ω
$V_{CC2}$ - $V_{EE2}$ = $V_{CC2}$ - GND2 = 20 V

**Figure 11. Output Transient Waveform**



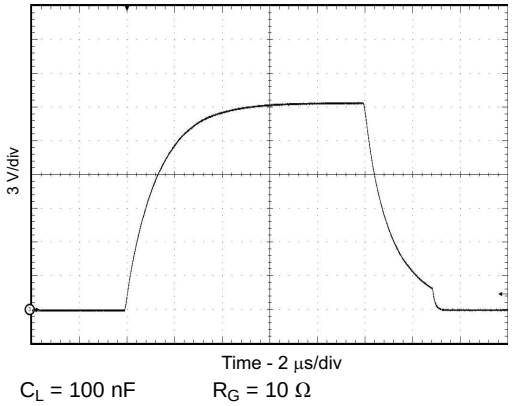

$C_L$ = 10 nF $R_G$ = 10 Ω
$V_{CC2}$ - $V_{EE2}$ = $V_{CC2}$ - GND2 = 20 V

**Figure 12. Output Transient Waveform**




$C_L$ = 100 nF $R_G$ = 0 Ω
$V_{CC2}$ - $V_{EE2}$ = $V_{CC2}$ - GND2 = 20 V

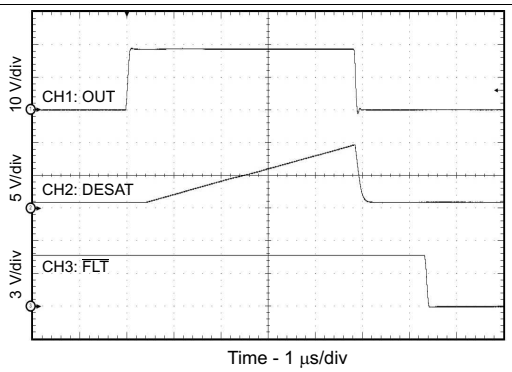
**Figure 13. Output Transient Waveform**




$C_L$ = 100 nF $R_G$ = 10 Ω
$V_{CC2}$ - $V_{EE2}$ = $V_{CC2}$ - GND2 = 20 V

**Figure 14. Output Transient Waveform**

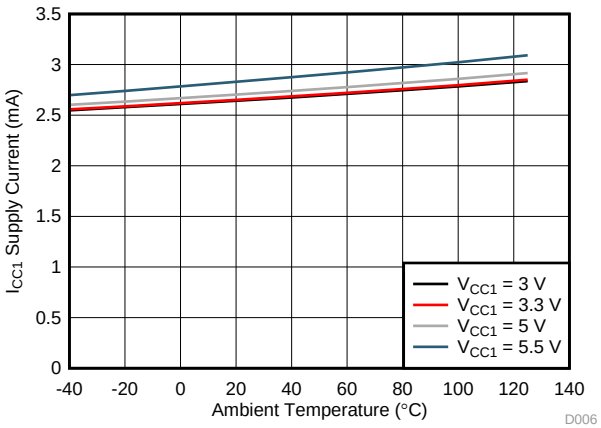
## Typical Characteristics (continued)




$C_L$ = 100 nF $R_G$ = 10 Ω

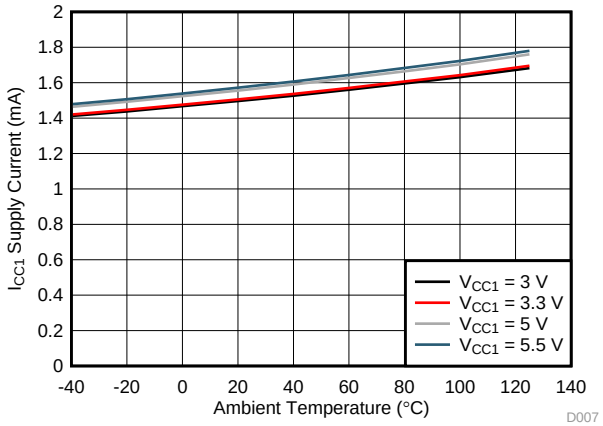
$V_{CC2}$ - $V_{EE2}$ = $V_{CC2}$ - GND2 = 20 V

**Figure 15. Output Transient Waveform DESAT and $\overline{FLT}$**



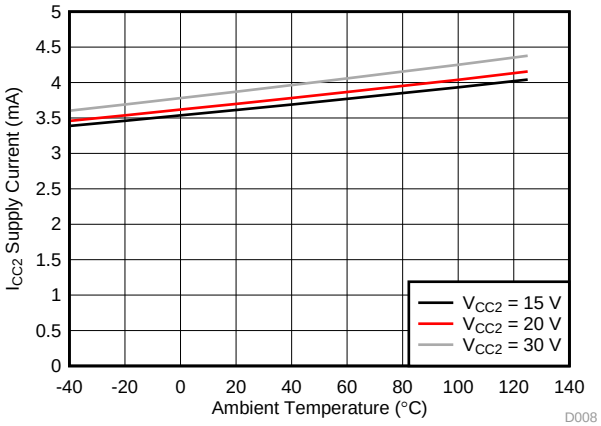

IN+ = High IN- = Low

**Figure 16. $I_{CC1}$ Supply Current vs Temperature**




IN+ = Low IN- = Low

**Figure 17. $I_{CC1}$ Supply Current vs Temperature**




Input Frequency = 1 kHz

**Figure 18. $I_{CC2}$ Supply Current vs Temperature**

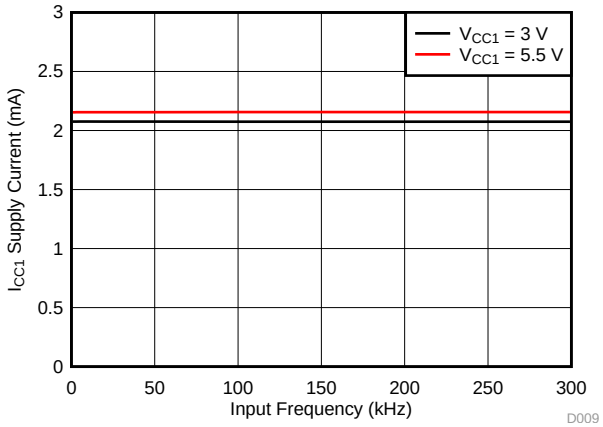
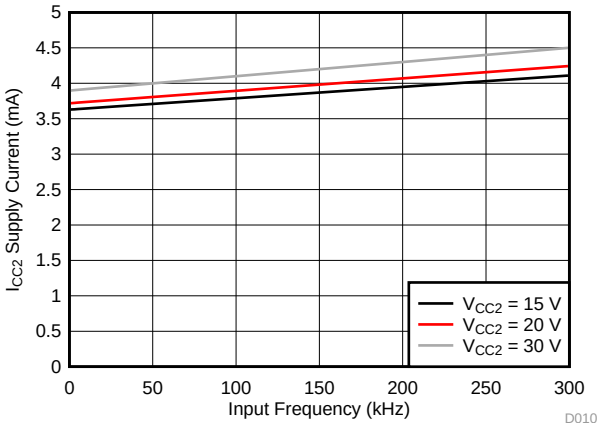


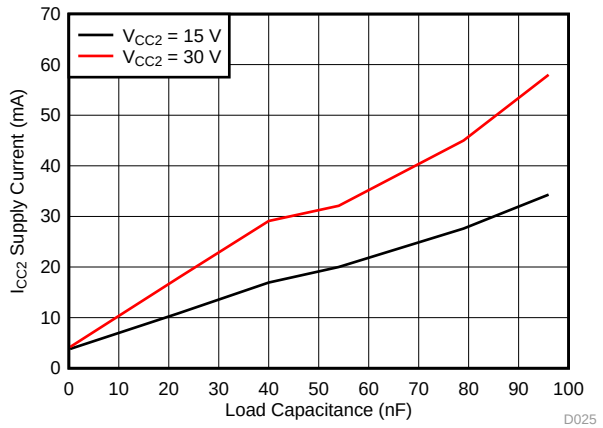

**Figure 19. $I_{CC1}$ Supply Current vs. Input Frequency**




No $C_L$

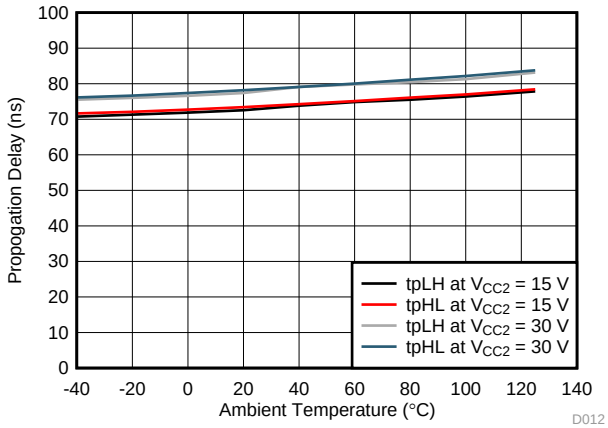
**Figure 20. $I_{CC2}$ Supply Current vs Input Frequency**

## Typical Characteristics (continued)



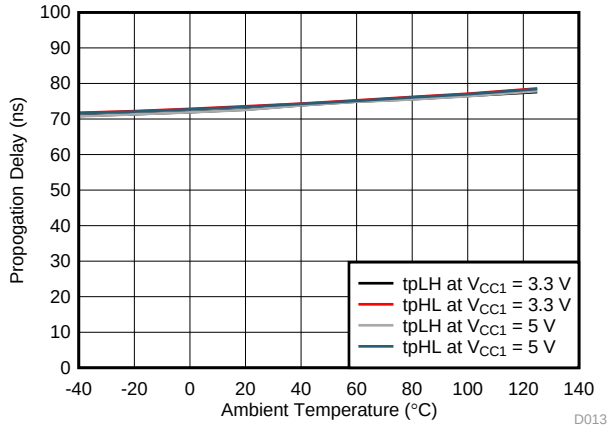

$R_G$ = 10 Ω, 20kHz

**Figure 21. $I_{CC2}$ Supply Current vs Load Capacitance**



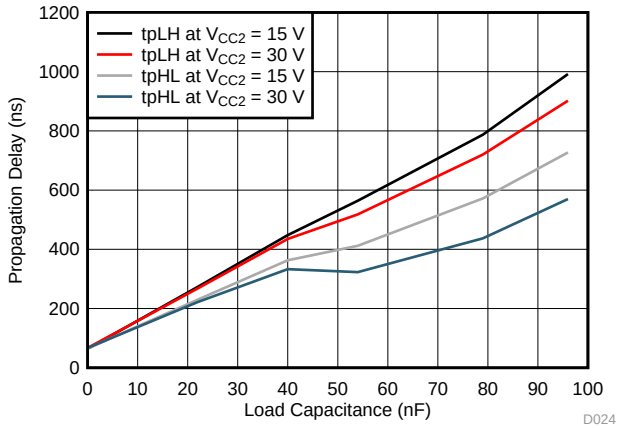

$C_L$ = 1nF $R_G$ = 0 Ω $V_{CC1}$ = 5 V

**Figure 22. $V_{CC1}$ Propagation Delay vs Temperature**



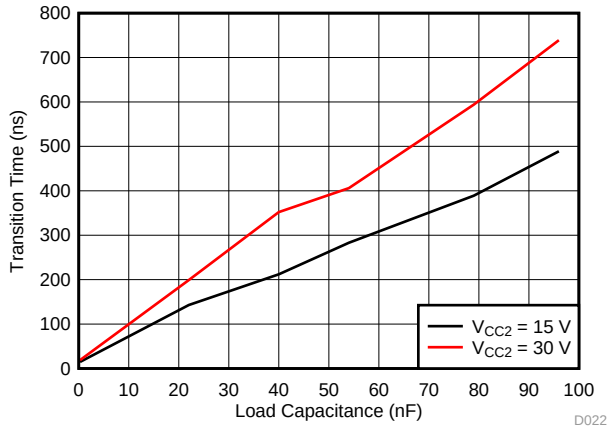

$C_L$ = 1nF $R_G$ = 0 Ω $V_{CC2}$ = 15 V

**Figure 23. $V_{CC2}$ Propagation Delay vs Temperature**



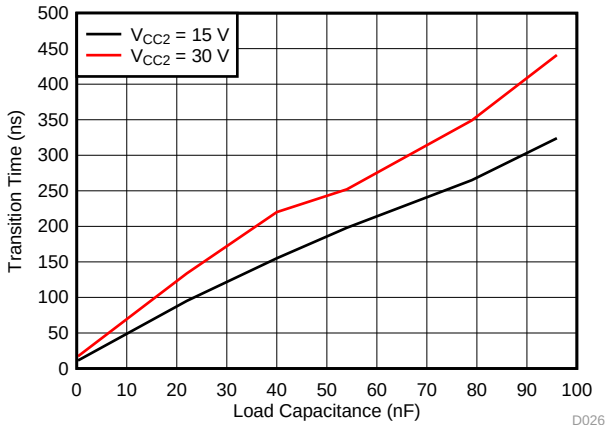

$R_G$ = 10 Ω $V_{CC1}$ = 5 V

**Figure 24. Propagation Delay vs Load Capacitance**




$R_G$ = 0 Ω $V_{CC1}$ = 5 V

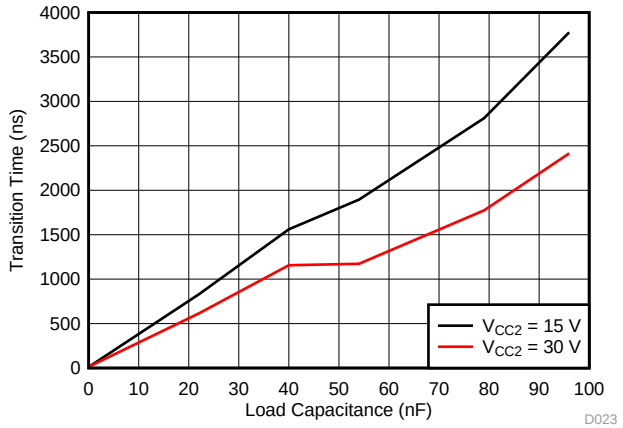
**Figure 25. $t_r$ Rise Time vs Load Capacitance**




$R_G$ = 0 Ω $V_{CC1}$ = 5 V

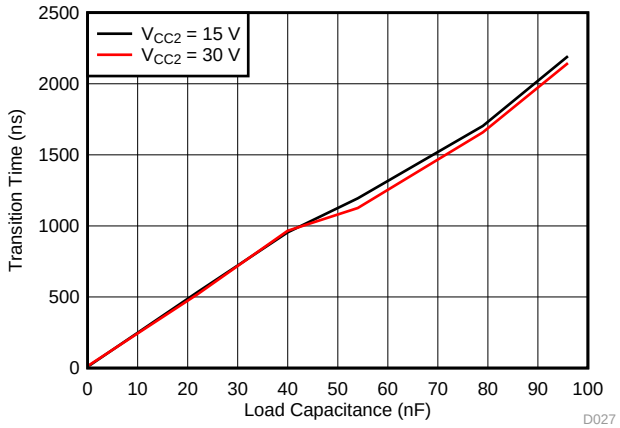
**Figure 26. $t_f$ Fall Time v. Load Capacitance**

## Typical Characteristics (continued)




$R_G$ = 10 Ω $V_{CC1}$ = 5 V

**Figure 27. $t_r$ Rise Time vs Load Capacitance**




$R_G$ = 10 Ω $V_{CC1}$ = 5 V

**Figure 28. $t_f$ Fall Time vs Load Capacitance**

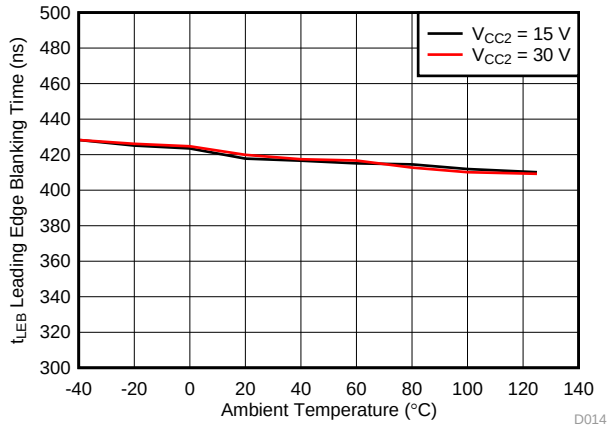
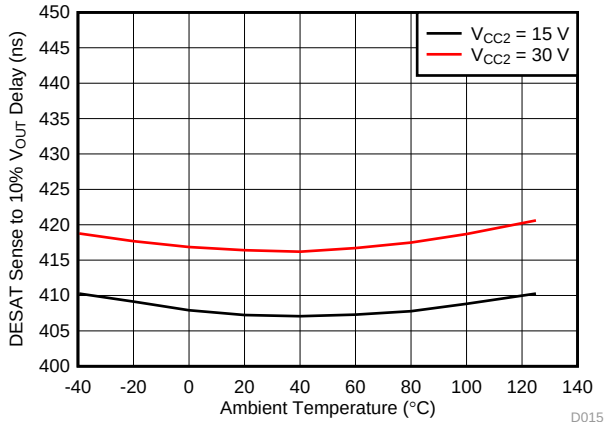
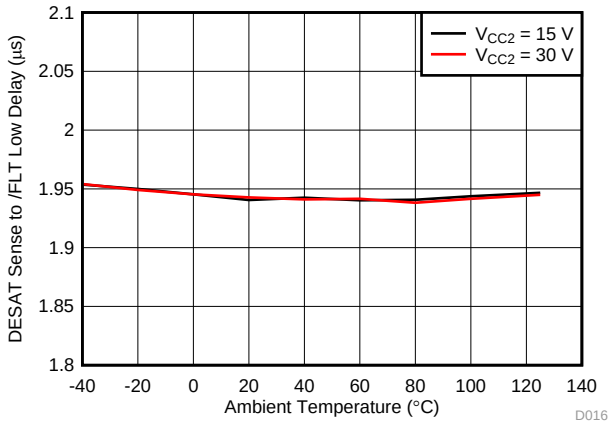



**Figure 29. Leading Edge Blanking Time With Temperature**




$C_L$ = 10 nF

**Figure 30. DESAT Sense to $V_{OUT}$ 10% Delay vs Temperature**




$C_L$ = 1 nF

**Figure 31. DESAT Sense to $\overline{FLT}$ Low Delay vs Temperature**

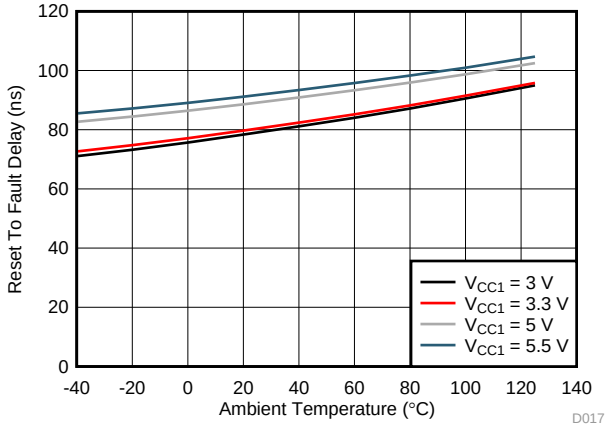



**Figure 32. Reset to Fault Delay Across Temperature**

## Typical Characteristics (continued)

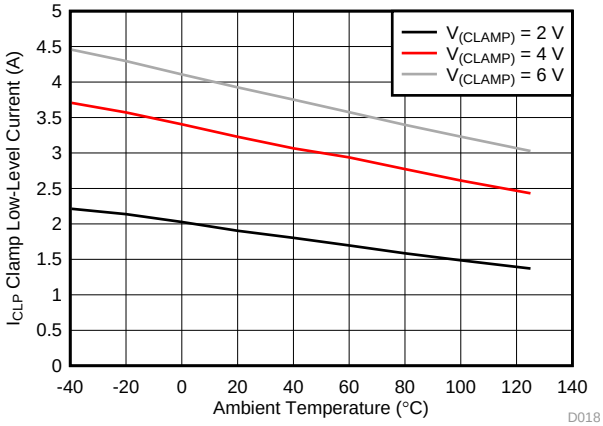



**Figure 33. Miller Clamp Current vs Temperature**

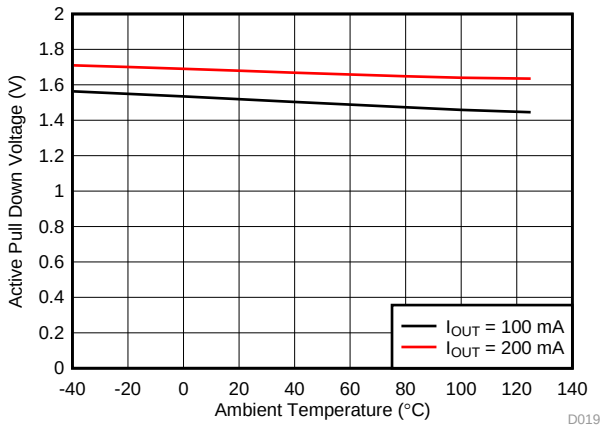



**Figure 34. Active Pull Down Voltage vs Temperature**

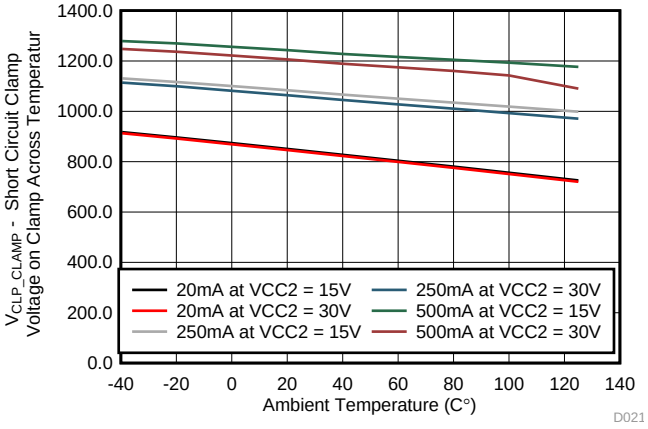



**Figure 35. $V_{CLP\_CLAMP}$ - Short Circuit Clamp Voltage on Clamp Across Temperature**

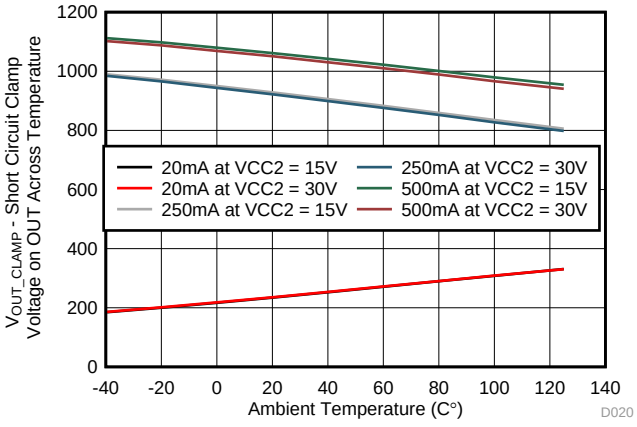
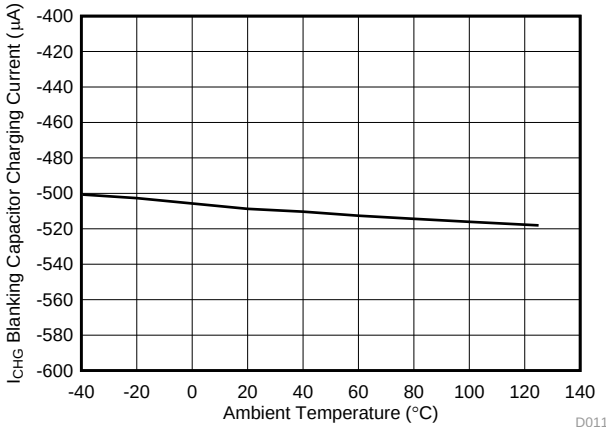



**Figure 36. $V_{OUT\_CLAMP}$ - Short Circuit Clamp Voltage on OUT Across Temperature**




$V_{CC2}$ = 15 V DESAT = 6 V

**Figure 37. Blanking Capacitor Charging Current vs Temperature**

# 8 Parameter Measurement Information

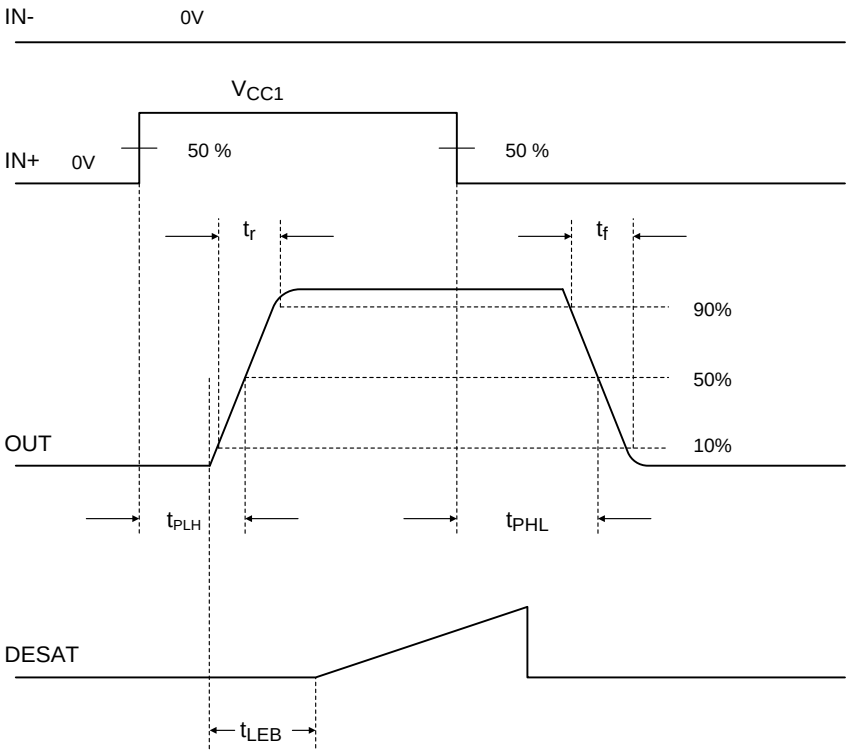



**Figure 38. OUT Propagation Delay, Non-Inverting Configuration**

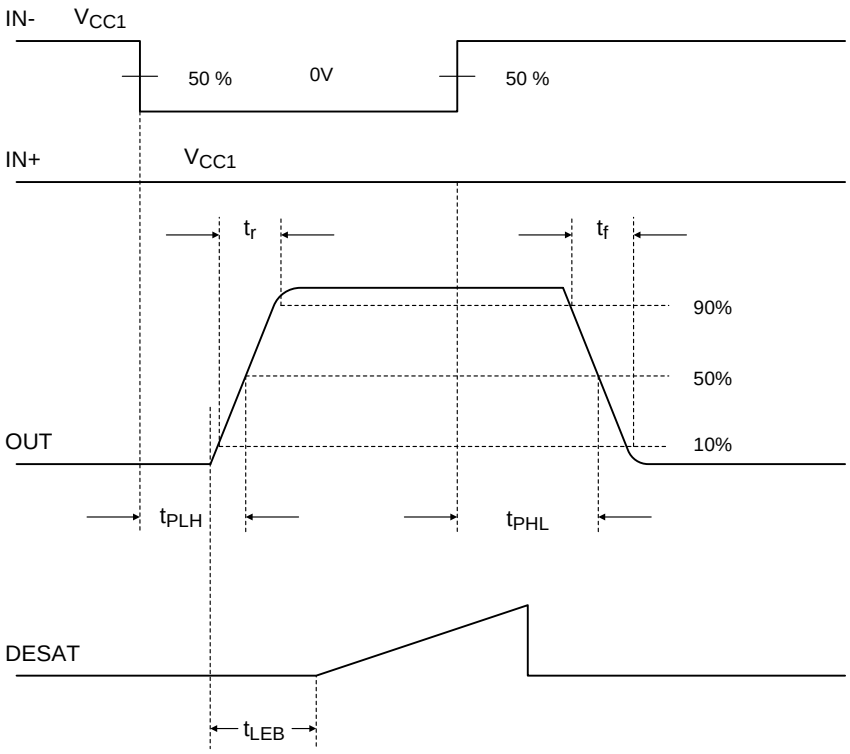



**Figure 39. OUT Propagation Delay, Inverting Configuration**

## Parameter Measurement Information (continued)

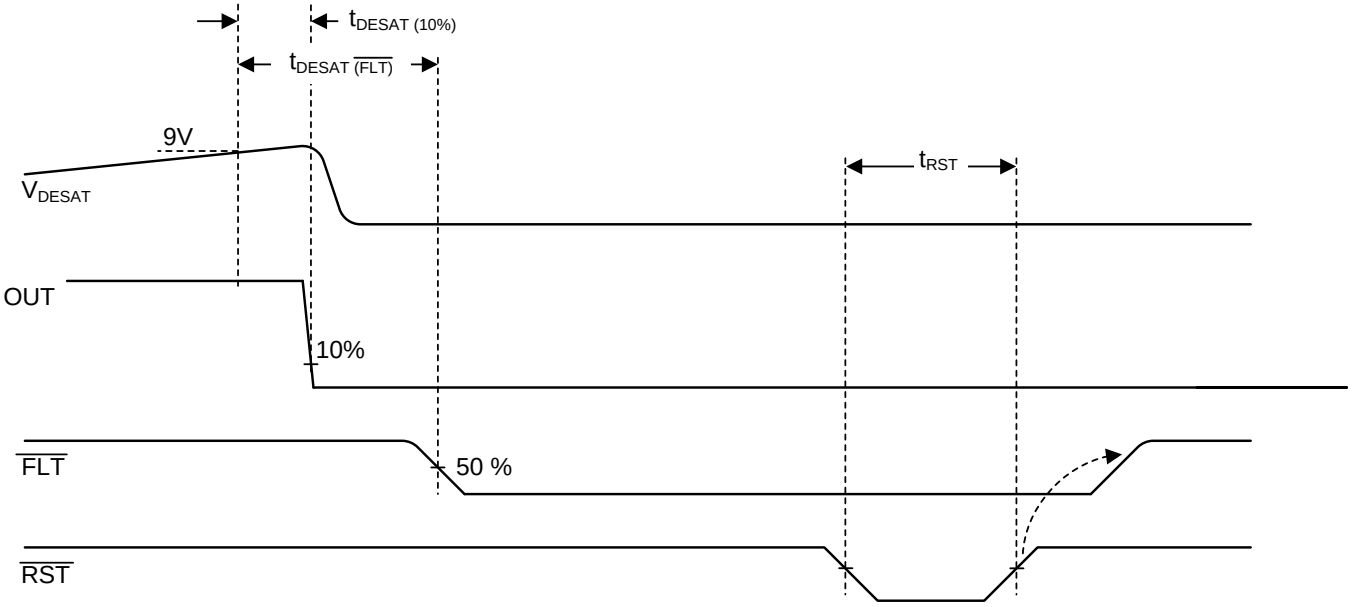



**Figure 40. DESAT, OUT, $\overline{FLT}$, $\overline{RST}$ Delay**

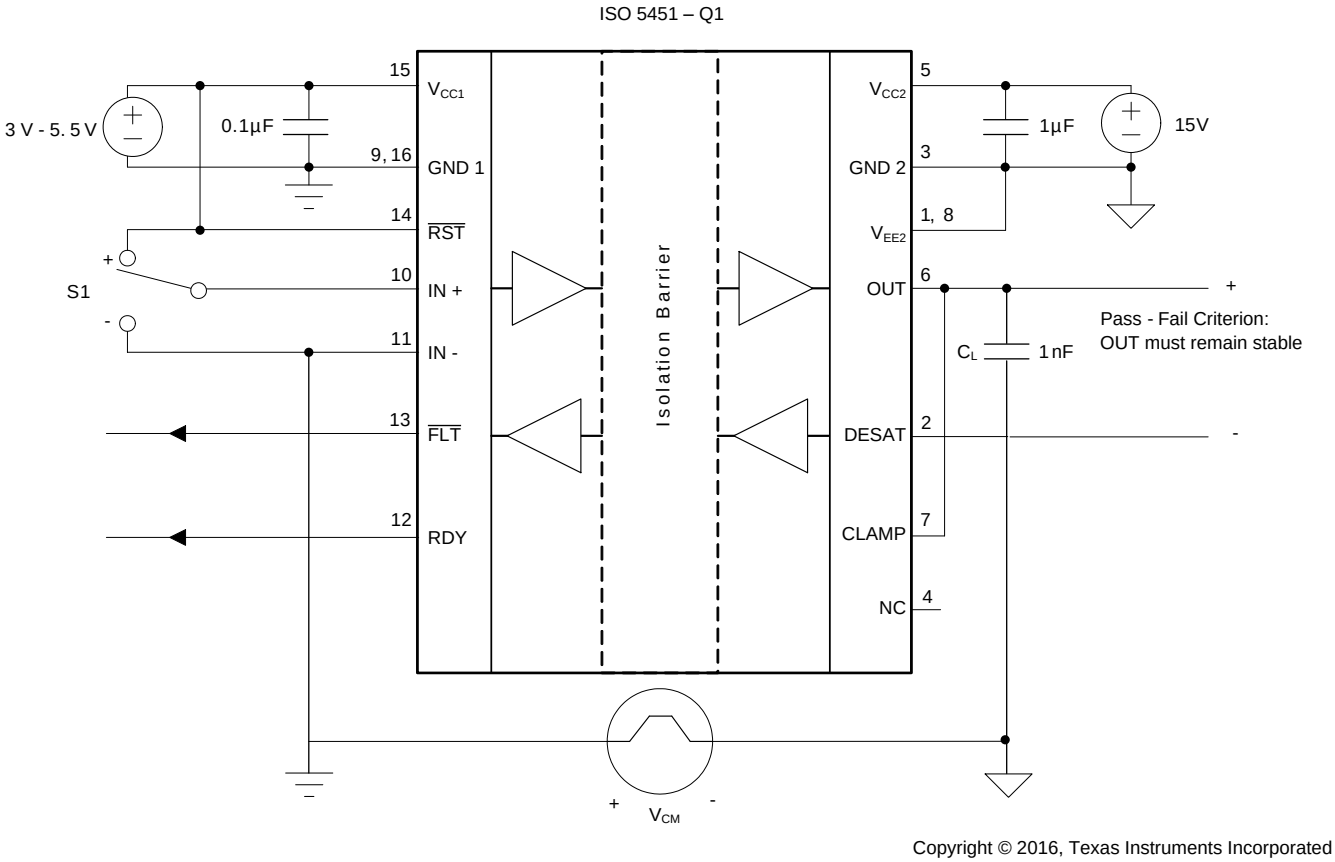



**Figure 41. Common-Mode Transient Immunity Test Circuit**

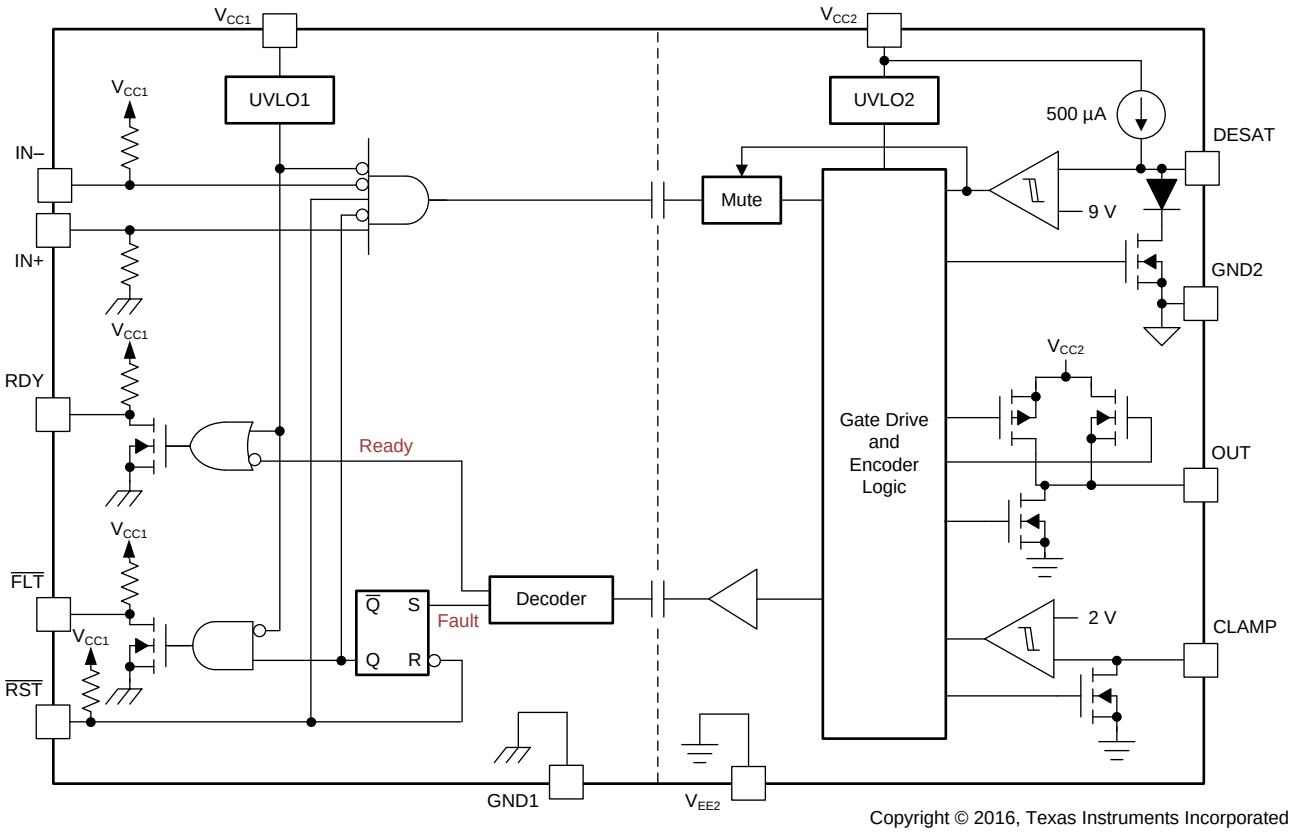
# 9 Detailed Description

## 9.1 Overview

The ISO5451-Q1 is an isolated gate driver for IGBTs and MOSFETs. Input CMOS logic and output power stage are separated by a capacitive, silicon dioxide ($SiO_2$), isolation barrier.

The IO circuitry on the input side interfaces with a micro controller and consists of gate drive control and RESET ($\overline{RST}$) inputs, READY (RDY) and FAULT ($\overline{FLT}$) alarm outputs. The power stage consists of power transistors to supply 2.5-A pull-up and 5-A pull-down currents to drive the capacitive load of the external power transistors, as well as DESAT detection circuitry to monitor IGBT collector-emitter overvoltage under short circuit events. The capacitive isolation core consists of transmit circuitry to couple signals across the capacitive isolation barrier, and receive circuitry to convert the resulting low-swing signals into CMOS levels. The ISO5451-Q1 also contains under voltage lockout circuitry to prevent insufficient gate drive to the external IGBT, and active output pull-down feature which ensures that the gate-driver output is held low, if the output supply voltage is absent. The ISO5451-Q1 also has an active Miller clamp function which can be used to prevent parasitic turn-on of the external power transistor, due to Miller effect, for unipolar supply operation.

## 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Supply and active Miller clamp

The ISO5451-Q1 supports both bipolar and unipolar power supply with active Miller clamp.

For operation with bipolar supplies, the IGBT is turned off with a negative voltage on its gate with respect to its emitter. This prevents the IGBT from unintentionally turning on because of current induced from its collector to its gate due to Miller effect. In this condition it is not necessary to connect CLAMP output of the gate driver to the IGBT gate, but connecting CLAMP output of the gate driver to the IGBT gate is also not an issue. Typical values of $V_{CC2}$ and $V_{EE2}$ for bipolar operation are 15 V and -8 V with respect to GND2.

For operation with unipolar supply, typically, $V_{CC2}$ is connected to 15 V with respect to GND2, and $V_{EE2}$ is connected to GND2. In this use case, the IGBT can turn-on due to additional charge from IGBT Miller capacitance caused by a high voltage slew rate transition on the IGBT collector. To prevent IGBT to turn on, the CLAMP pin is connected to IGBT gate and Miller current is sinked through a low impedance CLAMP transistor.

Miller CLAMP is designed for miller current up to 2 A. When the IGBT is turned-off and the gate voltage transitions below 2 V the CLAMP current output is activated.

### 9.3.2 Active Output Pull-down

The Active output pull-down feature ensures that the IGBT gate OUT is clamped to $V_{EE2}$ to ensure safe IGBT off-state when the output side is not connected to the power supply.

### 9.3.3 Undervoltage Lockout (UVLO) with Ready (RDY) Pin Indication Output

Undervoltage Lockout (UVLO) ensures correct switching of IGBT. The IGBT is turned-off, if the supply $V_{CC1}$ drops below $V_{IT-(UVLO1)}$, irrespective of IN+, IN- and RST input till $V_{CC1}$ goes above $V_{IT+(UVLO1)}$.

In similar manner, the IGBT is turned-off, if the supply $V_{CC2}$ drops below $V_{IT-(UVLO2)}$, irrespective of IN+, IN- and RST input till $V_{CC2}$ goes above $V_{IT+(UVLO2)}$.

Ready (RDY) pin indicates status of input and output side Under Voltage Lock-Out (UVLO) internal protection feature. If either side of device have insufficient supply ($V_{CC1}$ or $V_{CC2}$), the RDY pin output goes low; otherwise, RDY pin also serves as an indication to the micro-controller that the device is ready for operation.

### 9.3.4 Fault ($\overline{\text{FLT}}$) and Reset ($\overline{\text{RST}}$)

During IGBT overload condition, to report desaturation error $\overline{\text{FLT}}$ goes low. If $\overline{\text{RST}}$ is held low for the specified duration, $\overline{\text{FLT}}$ is cleared at rising edge of $\overline{\text{RST}}$. $\overline{\text{RST}}$ has an internal filter to reject noise and glitches. By asserting $\overline{\text{RST}}$ for at-least the specified minimum duration, device input logic can be enabled or disabled.

### 9.3.5 Short Circuit Clamp

Under short circuit events it is possible that currents are induced back into the gate-driver OUT and CLAMP pins due to parasitic Miller capacitance between the IGBT collector and gate terminals. Internal protection diodes on OUT and CLAMP help to sink these currents while clamping the voltages on these pins to values slightly higher than the output side supply.

## 9.4 Device Functional Modes

In ISO5451-Q1 OUT to follow IN+ in normal functional mode, $\overline{RST}$ and RDY needs to be in high state.

**Table 1. Function Table(1)**

| $V_{CC1}$ | $V_{CC2}$ | IN+ | IN- | $\overline{RST}$ | RDY | OUT |
|---|---|---|---|---|---|---|
| PU | PD | X | X | X | Low | Low |
| PD | PU | X | X | X | Low | Low |
| PU | PU | X | X | Low | High | Low |
| PU | Open | X | X | X | Low | Low |
| PU | PU | Low | X | X | High | Low |
| PU | PU | X | High | X | High | Low |
| PU | PU | High | Low | High | High | High |

(1) PU: Power Up ($V_{CC1}$ ≥ 2.25-V, $V_{CC2}$ ≥ 13-V), PD: Power Down ($V_{CC1}$ ≤ 1.7-V, $V_{CC2}$ ≤ 9.5-V), X: Irrelevant

# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The ISO5451-Q1 is an isolated gate driver for power semiconductor devices such as IGBTs and MOSFETs. It is intended for use in applications such as motor control, industrial inverters and switched mode power supplies. In these applications, sophisticated PWM control signals are required to turn the power devices on and off, which at the system level eventually may determine, for example, the speed, position, and torque of the motor or the output voltage, frequency and phase of the inverter. These control signals are usually the outputs of a micro controller, and are at low voltage levels such as 3.3-V or 5-V. The gate controls required by the MOSFETs and IGBTs, on the other hand, are in the range of 30-V (using Unipolar Output Supply) to 15-V (using Bipolar Output Supply), and need high current capability to be able to drive the large capacitive loads offered by those power transistors. Not only that, the gate drive needs to be applied with reference to the Emitter of the IGBT (Source for MOSFET), and by construction, the Emitter node in a gate drive system may swing between 0 to the DC bus voltage, that can be several 100s of volts in magnitude.

The ISO5451-Q1 is thus used to level shift the incoming 3.3-V and 5-V control signals from the microcontroller to the 30-V (using Unipolar Output Supply) to 15-V (using Bipolar Output Supply) drive required by the power transistors while ensuring high-voltage isolation between the driver side and the microcontroller side.

## 10.2 Typical Applications

Figure 42 shows the typical application of a three-phase inverter using six ISO5451-Q1 isolated gate drivers. Three-phase inverters are used for variable-frequency drives to control the operating speed and torque of AC motors and for high power applications such as High-Voltage DC (HVDC) power transmission.

The basic three-phase inverter consists of six power switches, and each switch is driven by one ISO5451-Q1. The switches are driven on and off at high switching frequency with specific patterns that to converter dc bus voltage to three-phase AC voltages.

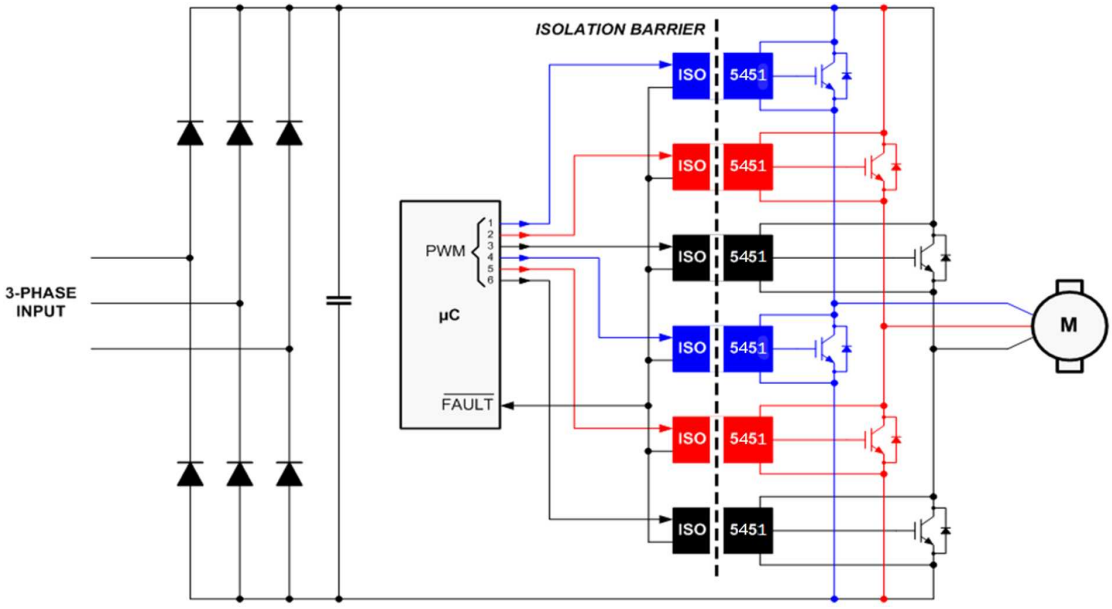



**Figure 42. Typical Motor Drive Application**

## Typical Applications (continued)

### 10.2.1 Design Requirements

Unlike optocoupler based gate drivers which need external current drivers and biasing circuitry to provide the input control signals, the input control to the ISO5451-Q1 is CMOS and can be directly driven by the microcontroller. Other design requirements include decoupling capacitors on the input and output supplies, a pullup resistor on the common drain $\overline{FLT}$ output signal and $\overline{RST}$ input signal, and a high-voltage protection diode between the IGBT collector and the DESAT input. Further details are explained in the subsequent sections. Table 2 shows the allowed range for Input and Output supply voltage, and the typical current output available from the gate-driver.

**Table 2. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| Input supply voltage | 3-V to 5.5-V |
| Unipolar output supply voltage ($V_{CC2}$ - GND2 = $V_{CC2}$ - $V_{EE2}$) | 15-V to 30-V |
| Bipolar output supply voltage ($V_{CC2}$ - $V_{EE2}$) | 15-V to 30-V |
| Bipolar output supply voltage (GND2 - $V_{EE2}$) | 0-V to 15-V |
| Output current | 2.5-A |

### 10.2.2 Detailed Design Procedure

#### *10.2.2.1 Recommended ISO5451-Q1 Application Circuit*

The ISO5451-Q1 has both, inverting and non-inverting gate control inputs, an active low reset input, and an open drain fault output suitable for wired-OR applications. The recommended application circuit in Figure 43 illustrates a typical gate driver implementation with Unipolar Output Supply and Figure 44 illustrates a typical gate driver implementation with Bipolar Output Supply using the ISO5451-Q1.

A 0.1-µF bypass capacitor, recommended at input supply pin $V_{CC1}$ and 1-µF bypass capacitor, recommended at output supply pin $V_{CC2}$, provide the large transient currents necessary during a switching transition to ensure reliable operation. The 220 pF blanking capacitor disables DESAT detection during the off-to-on transition of the power device. The DESAT diode ($D_{DST}$) and its 1-kΩ series resistor are external protection components. The $R_G$ gate resistor limits the gate charge current and indirectly controls the IGBT collector voltage rise and fall times. The open-drain $\overline{FLT}$ output and RDY output has a passive 10-kΩ pull-up resistor. In this application, the IGBT gate driver is disabled when a fault is detected and will not resume switching until the micro-controller applies a reset signal.

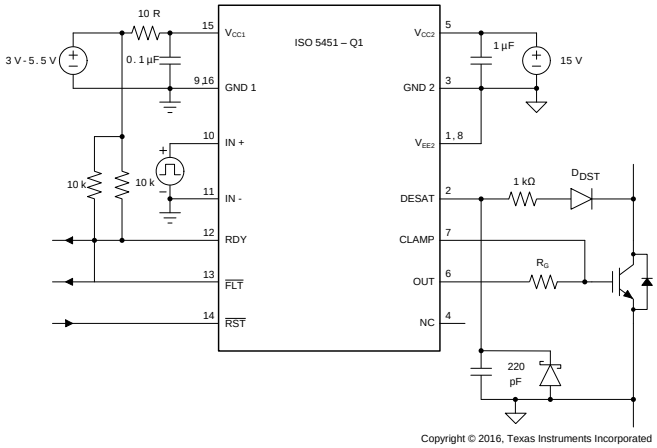



**Figure 43. Unipolar Output Supply**

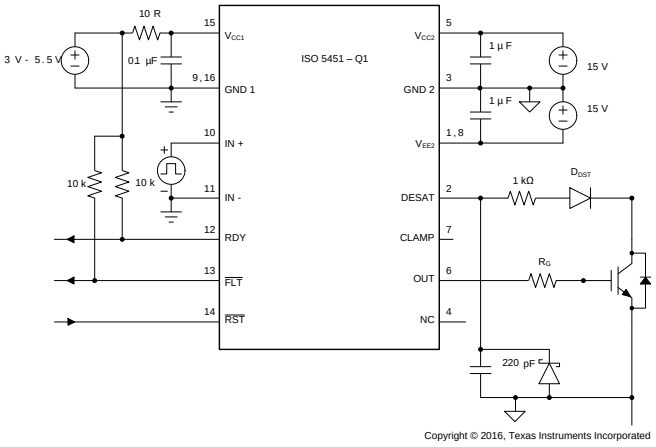



**Figure 44. Bipolar Output Supply**

#### 10.2.2.2 $\overline{FLT}$ and RDY Pin Circuitry

There is 50k pull-up resistor internally on $\overline{FLT}$ and RDY pins. The $\overline{FLT}$ and RDY pin is an open-drain output. A 10-kΩ pull-up resistor can be used to make it faster rise and to provide logic high when $\overline{FLT}$ and RDY is inactive, as shown in Figure 45.

Fast common mode transients can inject noise and glitches on $\overline{FLT}$ and RDY pins due to parasitic coupling. This is dependent on board layout. If required, additional capacitance (100 pF to 300 pF) can be included on the $\overline{FLT}$ and RDY pins.

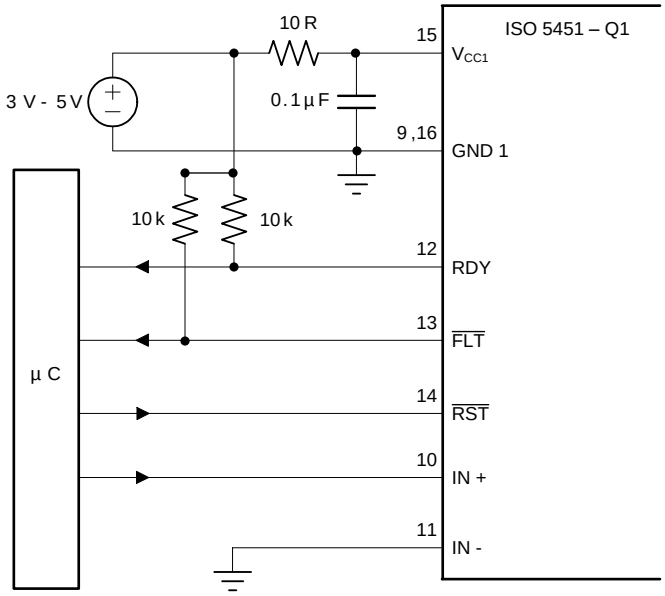




**Figure 45. $\overline{FLT}$ and RDY Pin Circuitry for High CMTI**

#### 10.2.2.3 Driving the Control Inputs

The amount of common-mode transient immunity (CMTI) can be curtailed by the capacitive coupling from the high-voltage output circuit to the low-voltage input side of the ISO5451-Q1. For maximum CMTI performance, the digital control inputs, IN+ and IN-, must be actively driven by standard CMOS, push-pull drive circuits. This type of low-impedance signal source provides active drive signals that prevent unwanted switching of the ISO5451-Q1 output under extreme common-mode transient conditions. Passive drive circuits, such as open-drain configurations using pull-up resistors, must be avoided. There is a 20 ns glitch filter which can filter a glitch up to 20 ns on IN+ or IN-.

### 10.2.2.4 Local Shutdown and Reset

In applications with local shutdown and reset, the $\overline{FLT}$ output of each gate driver is polled separately, and the individual reset lines are asserted low independently to reset the motor controller after a fault condition.

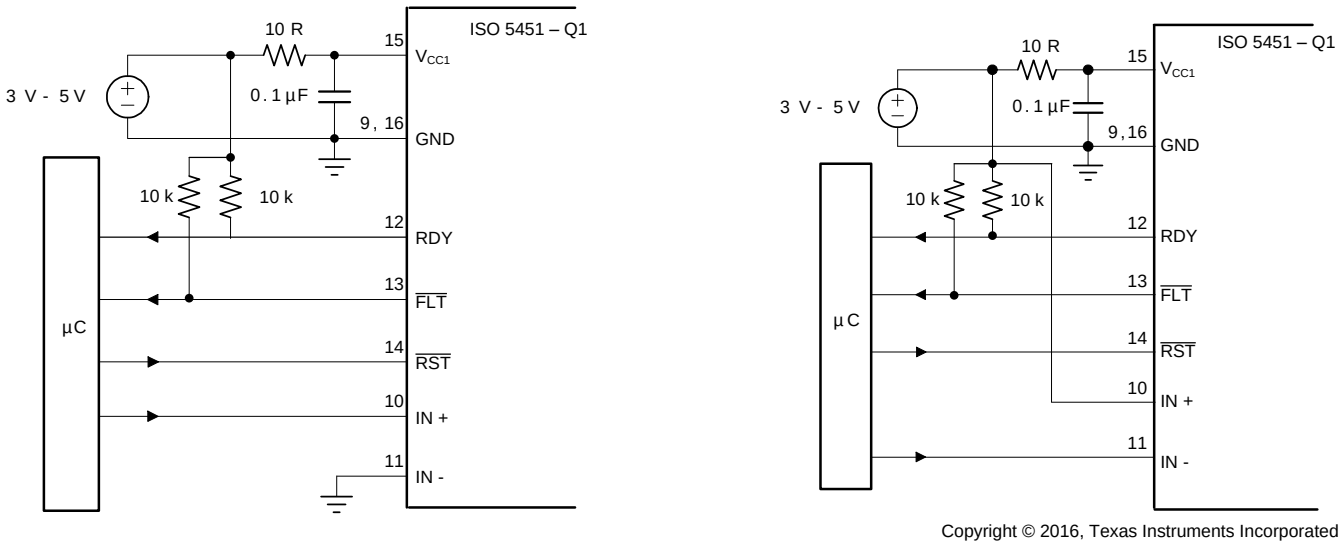





**Figure 46. Local Shutdown and Reset for Noninverting (left) and Inverting Input Configuration (right)**

### 10.2.2.5 Global-Shutdown and Reset

When configured for inverting operation, the ISO5451-Q1 can be configured to shutdown automatically in the event of a fault condition by tying the $\overline{FLT}$ output to IN+. For high reliability drives, the open drain $\overline{FLT}$ outputs of multiple ISO5451-Q1 devices can be wired together forming a single, common fault bus for interfacing directly to the micro-controller. When any of the six gate drivers of a three-phase inverter detects a fault, the active low $\overline{FLT}$ output disables all six gate drivers simultaneously.

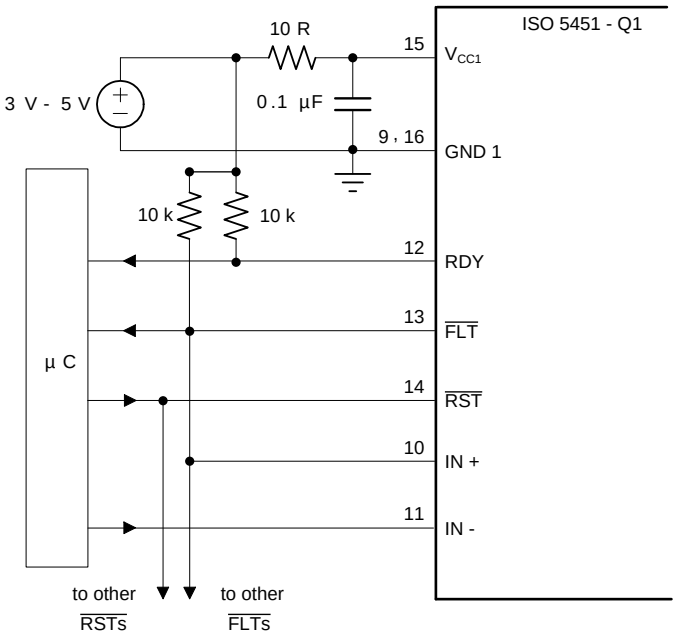





**Figure 47. Global Shutdown with Inverting Input Configuration**

#### *10.2.2.6 Auto-Reset*

In this case, the gate control signal at IN+ is also applied to the $\overline{RST}$ input to reset the fault latch every switching cycle. Incorrect $\overline{RST}$ makes output go low. A fault condition, however, the gate driver remains in the latched fault state until the gate control signal changes to the 'gate low' state and resets the fault latch.

If the gate control signal is a continuous PWM signal, the fault latch will always be reset before IN+ goes high again. This configuration protects the IGBT on a cycle by cycle basis and automatically resets before the next 'on' cycle.

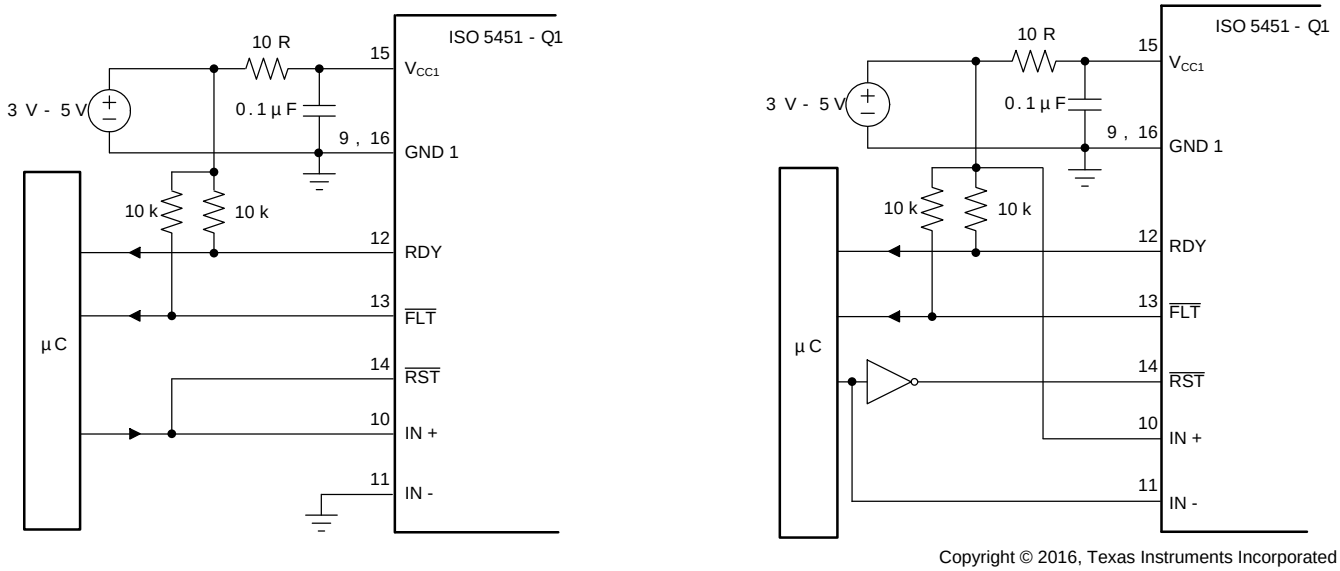





**Figure 48. Auto Reset for Non-inverting and Inverting Input Configuration**

### 10.2.2.7 DESAT Pin Protection

Switching inductive loads causes large instantaneous forward voltage transients across the freewheeling diodes of IGBTs. These transients result in large negative voltage spikes on the DESAT pin which draw substantial current out of the device. To limit this current below damaging levels, a 100-Ω to 1-kΩ resistor is connected in series with the DESAT diode.

Further protection is possible through an optional Schottky diode, whose low forward voltage assures clamping of the DESAT input to GND2 potential at low voltage levels.

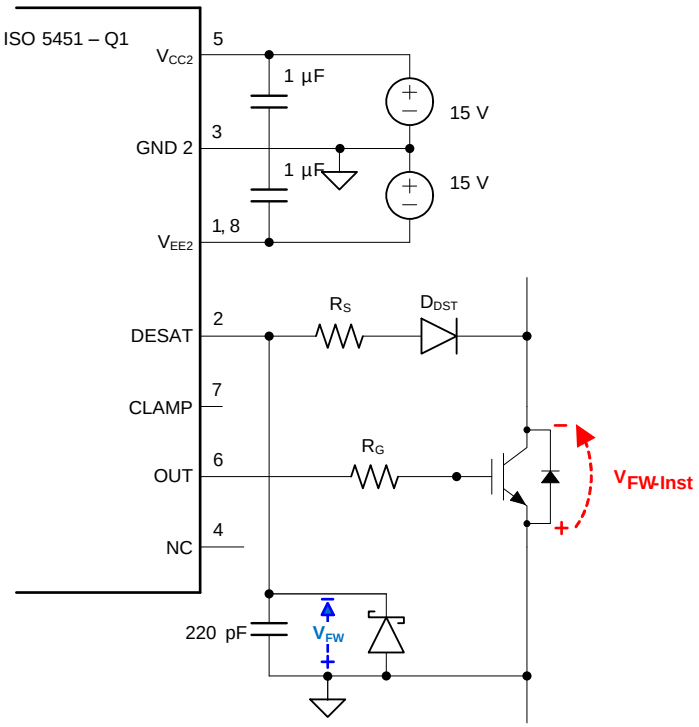



**Figure 49. DESAT Pin Protection with Series Resistor and Schottky Diode**

### 10.2.2.8 DESAT Diode and DESAT Threshold

The DESAT diode's function is to conduct forward current, allowing sensing of the IGBT's saturated collector-to-emitter voltage, $V_{(CESAT)}$, (when the IGBT is "on") and to block high voltages (when the IGBT is "off"). During the short transition time when the IGBT is switching, there is commonly a high $dV_{CE}/dt$ voltage ramp rate across the IGBT. This results in a charging current $I_{(CHARGE)} = C_{(D\text{-}DESAT)} \times d_{VCE}/dt$, charging the blanking capacitor. $C_{(D\text{-}DESAT)}$ is the diode capacitance at DESAT.

To minimize this current and avoid false DESAT triggering, fast switching diodes with low capacitance are recommended. As the diode capacitance builds a voltage divider with the blanking capacitor, large collector voltage transients appear at DESAT attenuated by the ratio of $1+ C_{(BLANK)} / C_{(D\text{-}DESAT)}$.

Because the sum of the DESAT diode forward-voltage and the IGBT collector-emitter voltage make up the voltage at the DESAT-pin, $V_F + V_{CE} = V_{(DESAT)}$, the $V_{CE}$ level, which triggers a fault condition, can be modified by adding multiple DESAT diodes in series: $V_{CE\text{-}FAULT(TH)} = 9\ V – n \times VF$ (where n is the number of DESAT diodes).

When using two diodes instead of one, diodes with half the required maximum reverse-voltage rating may be chosen.

#### 10.2.2.9 Determining the Maximum Available, Dynamic Output Power, $P_{OD\text{-}max}$

The ISO5451-Q1 maximum allowed total power consumption of $P_D$ = 251 mW consists of the total input power, $P_{ID}$, the total output power, $P_{OD}$, and the output power under load, $P_{OL}$:

$$P_D = P_{ID} + P_{OD} + P_{OL} \quad (1)$$

With:

$$P_{ID} = V_{CC1\text{-}max} \times I_{CC1\text{-}max} = 5.5\ V \times 4.5\ mA = 24.75\ mW \quad (2)$$

and:

$$P_{OD} = (V_{CC2} - V_{EE2}) \times I_{CC2\text{-}max} = (15V - (-8V)) \times 6\ mA = 138\ mW \quad (3)$$

then:

$$P_{OL} = P_D - P_{ID} - P_{OD} = 251\ mW - 24.75\ mW - 138\ mW = 88.25\ mW \quad (4)$$

In comparison to $P_{OL}$, the actual dynamic output power under worst case condition, $P_{OL\text{-}WC}$, depends on a variety of parameters:

$$P_{OL\text{-}WC} = 0.5 \times f_{INP} \times Q_G \times (V_{CC2} - V_{EE2}) \times \left( \frac{r_{on\text{-}max}}{r_{on\text{-}max} + R_G} + \frac{r_{off\text{-}max}}{r_{off\text{-}max} + R_G} \right) \quad (5)$$

where

- $f_{INP}$ = signal frequency at the control input IN+
- $Q_G$ = power device gate charge
- $V_{CC2}$ = positive output supply with respect to GND2
- $V_{EE2}$ = negative output supply with respect to GND2
- $r_{on\text{-}max}$ = worst case output resistance in the on-state: 4Ω
- $r_{off\text{-}max}$ = worst case output resistance in the off-state: 2.5Ω
- $R_G$ = gate resistor

Once $R_G$ is determined, Equation 5 is to be used to verify whether $P_{OL\text{-}WC} < P_{OL}$. Figure 50 shows a simplified output stage model for calculating $P_{OL\text{-}WC}$.

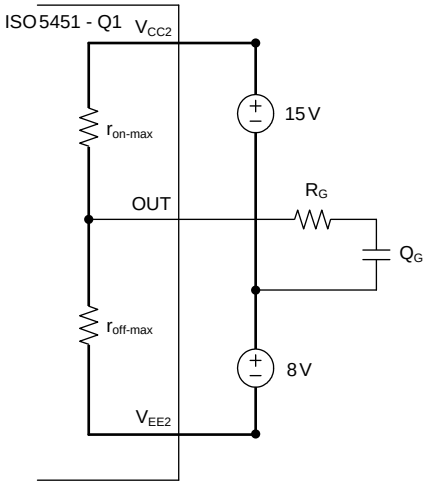





**Figure 50. Simplified Output Model for Calculating $P_{OL\text{-}WC}$**

#### 10.2.2.10 Example

This examples considers an IGBT drive with the following parameters:

$I_{ON-PK}$ = 2 A, $Q_G$ = 650 nC, $f_{INP}$ = 20 kHz, $V_{CC2}$ = 15V, $V_{EE2}$ = –8 V (6)

Apply the value of the gate resistor $R_G$ = 10 Ω.

Then, calculating the worst-case output power consumption as a function of $R_G$, using Equation 5 $r_{on-max}$ = worst case output resistance in the on-state: 4Ω, $r_{off-max}$ = worst case output resistance in the off-state: 2.5Ω, $R_G$ = gate resistor yields

$$P_{OL-WC} = 0.5 \times 20\ kHz \times 650\ nC \times (15\ V - (-8\ V)) \times \left( \frac{4\ \Omega}{4\ \Omega + 10\ \Omega} + \frac{2.5\ \Omega}{2.5\ \Omega + 10\ \Omega} \right) = 72.61\ mW \quad (7)$$

Because $P_{OL-WC}$ = 72.61 mW is below the calculated maximum of $P_{OL}$ = 88.25 mW, the resistor value of $R_G$ = 10 Ω is suitable for this application.

#### 10.2.2.11 Higher Output Current Using an External Current Buffer

To increase the IGBT gate drive current, a non-inverting current buffer (such as the npn/pnp buffer shown in Figure 51) may be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for currents up to 8 A, the D44VH10/ D45VH10 pair for up to 15 A maximum.

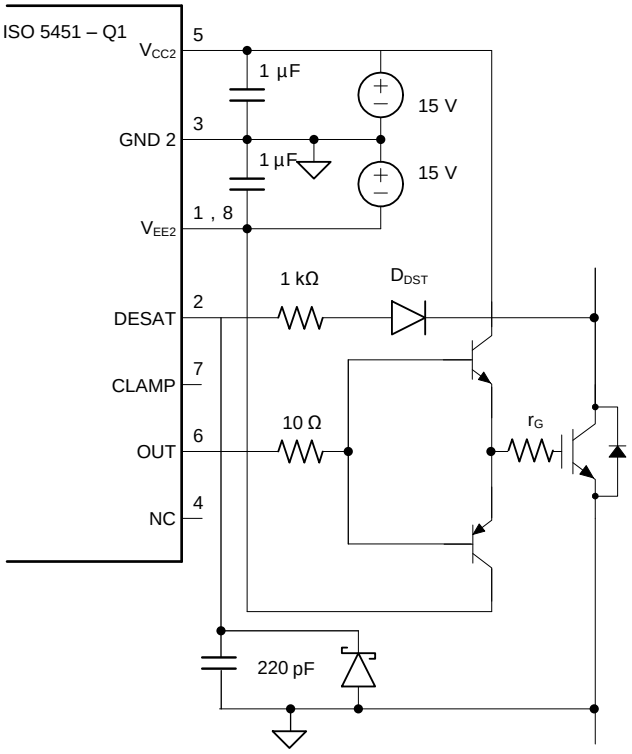
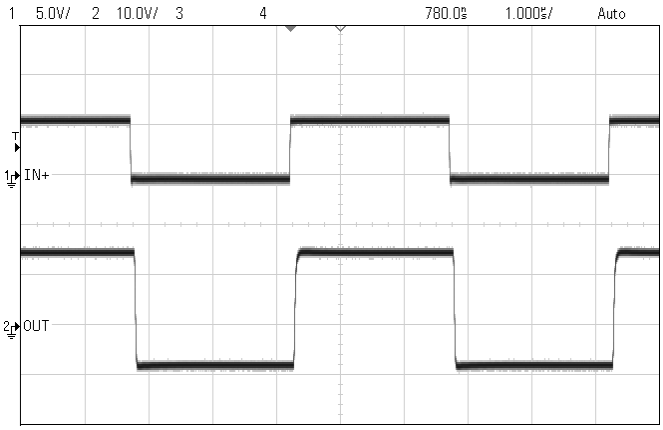




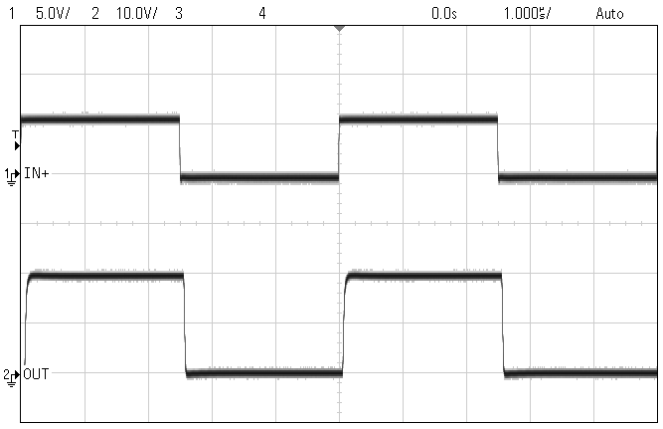

**Figure 51. Current Buffer for Increased Drive Current**

### 10.2.3 Application Curve




$C_L$ = 1 nF $R_G$ = 10 Ω
$V_{CC2}$ - GND2 = 15 V GND2 - $V_{EE2}$ = 8 V
($V_{CC2}$ - $V_{EE2}$ = 23 V)

**Figure 52. Normal Operation - Bipolar Supply**




$C_L$ = 1 nF $R_G$ = 10 Ω
$V_{CC2}$ - $V_{EE2}$ = $V_{CC2}$ - GND2 = 20 V

**Figure 53. Normal Operation - Unipolar Supply**

# 11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1-μF bypass capacitor is recommended at input supply pin $V_{CC1}$ and 1-μF bypass capacitor is recommended at output supply pin $V_{CC2}$. The capacitors should be placed as close to the supply pins as possible. Recommended placement of capacitors needs to be 2-mm maximum from input and output power supply pin ($V_{CC1}$ and $V_{CC2}$).

# 12 Layout

## 12.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 54). Layer stacking should be in the following order (top-to-bottom): high-current or sensitive signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-current or sensitive traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the gate driver and the microcontroller and power transistors. Gate driver control input, Gate driver output OUT and DESAT should be routed in the top layer.
- Placing a solid ground plane next to the sensitive signal layer provides an excellent low-inductance path for the return current flow. On the driver side, use GND2 as the ground plane.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch$^2$. On the gate-driver $V_{EE2}$ and $V_{CC2}$ can be used as power planes. They can share the same layer on the PCB as long as they are not connected together.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

For more detailed layout recommendations, including placement of capacitors, impact of vias, reference planes, routing etc. see Application Note SLLA284, *Digital Isolator Design Guide*.

## 12.2 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

## 12.3 Layout Example

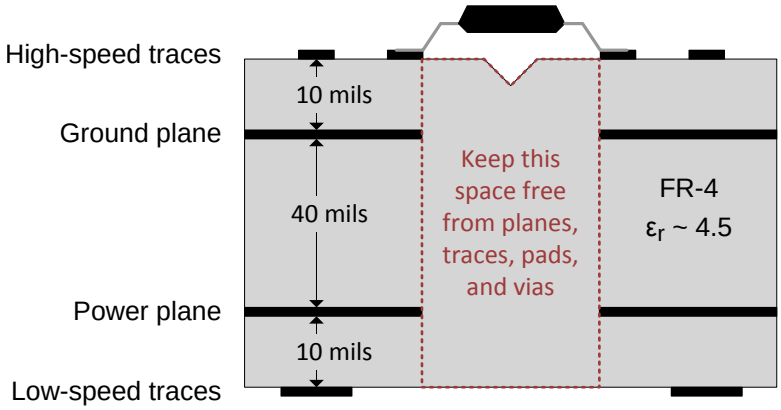



**Figure 54. Recommended Layer Stack**

# 13 器件和文档支持

## 13.1 文档支持

### 13.1.1 相关文档

相关文档如下：

- *《ISO5851 评估模块 (EVM) 用户指南》*，SLLU218
- *《数字隔离器设计指南》*，SLLA284
- *《隔离相关术语》*，SLLA353

## 13.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

## 13.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 13.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 13.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 14 机械、封装和可订购信息

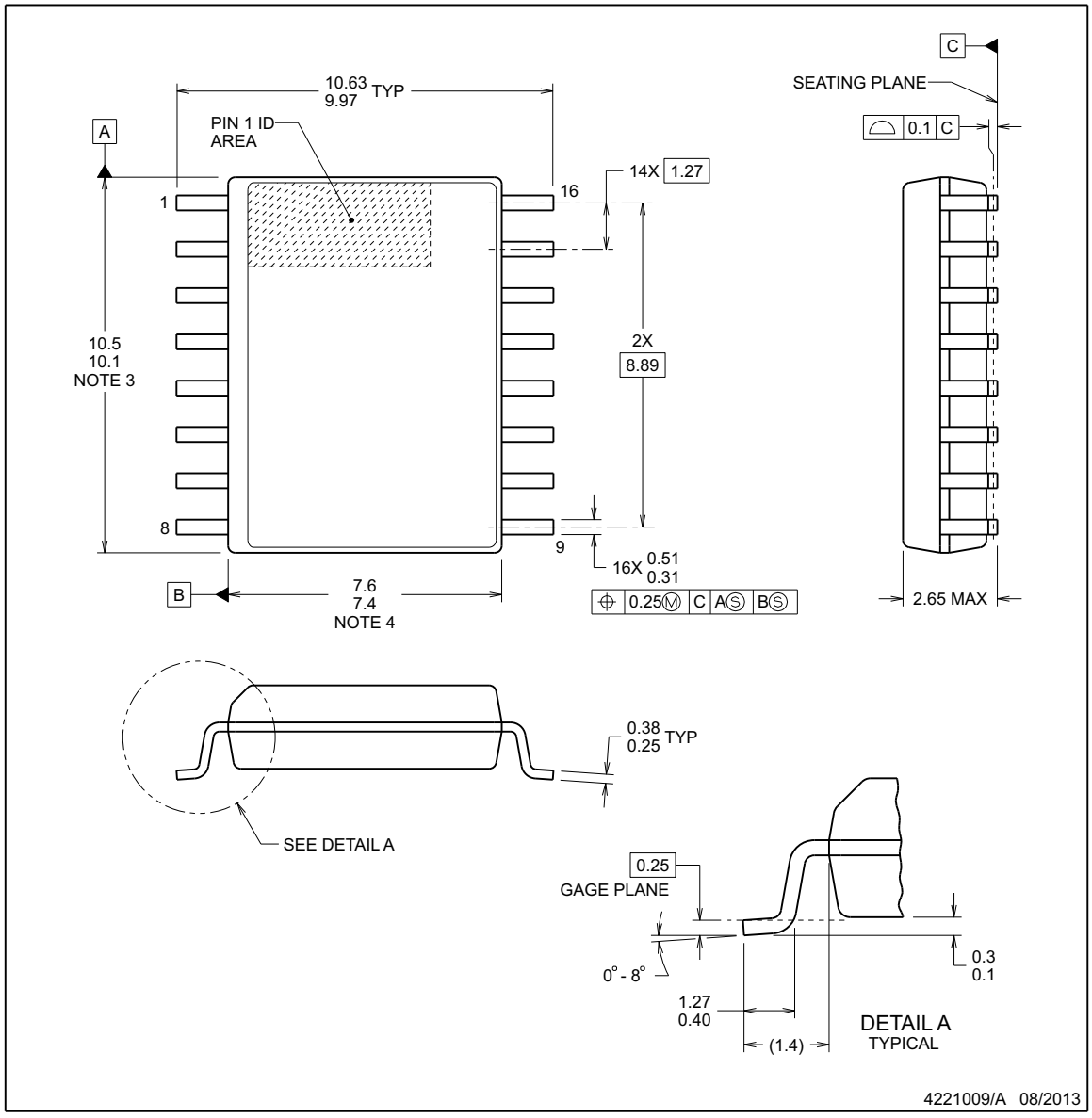
以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

# PACKAGE OUTLINE

## DW0016B

SOIC - 2.65 mm max height

SOIC




NOTES:

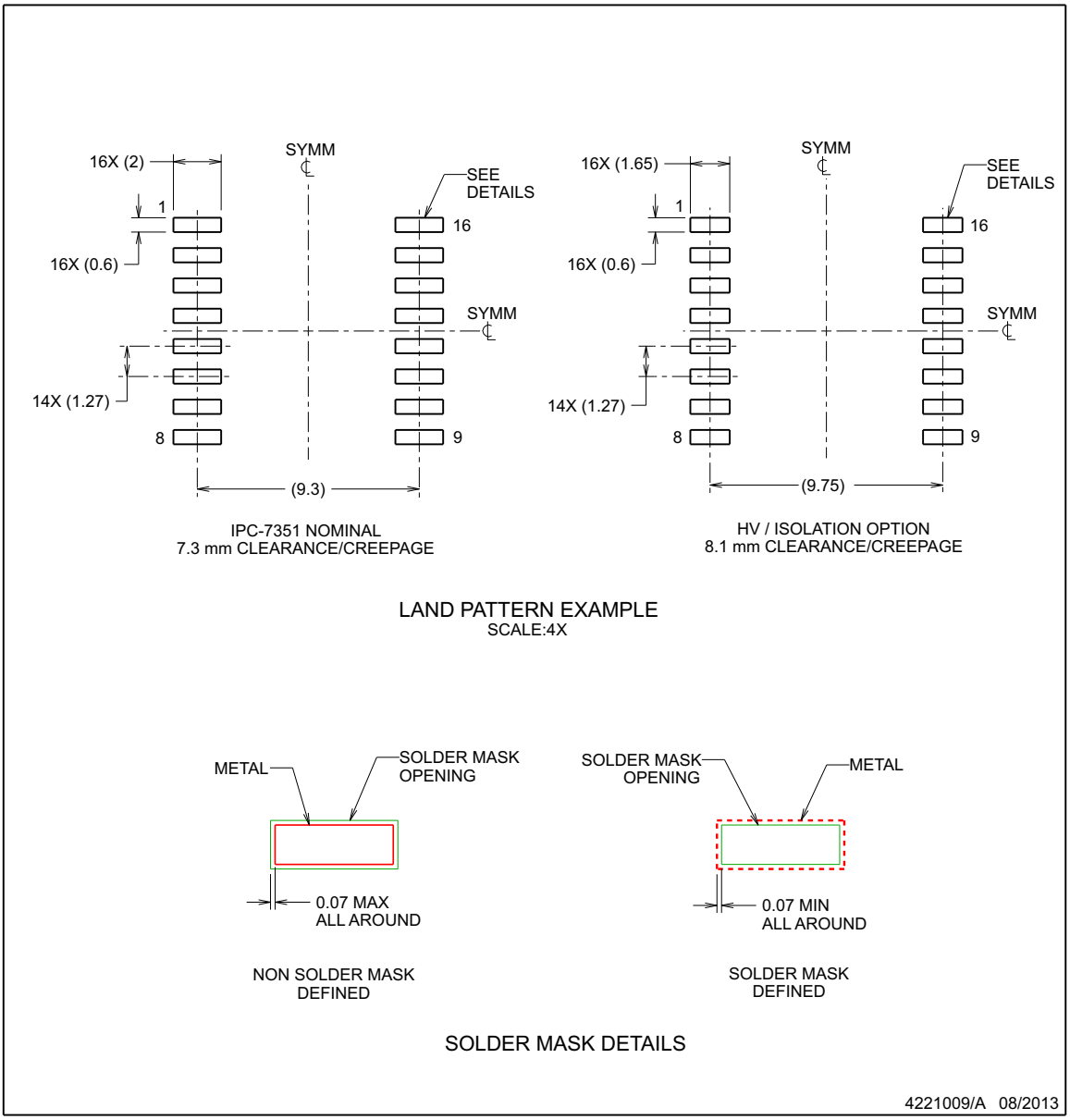
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-013, variation AA.

# EXAMPLE BOARD LAYOUT

## DW0016B

SOIC - 2.65 mm max height

SOIC




NOTES: (continued)

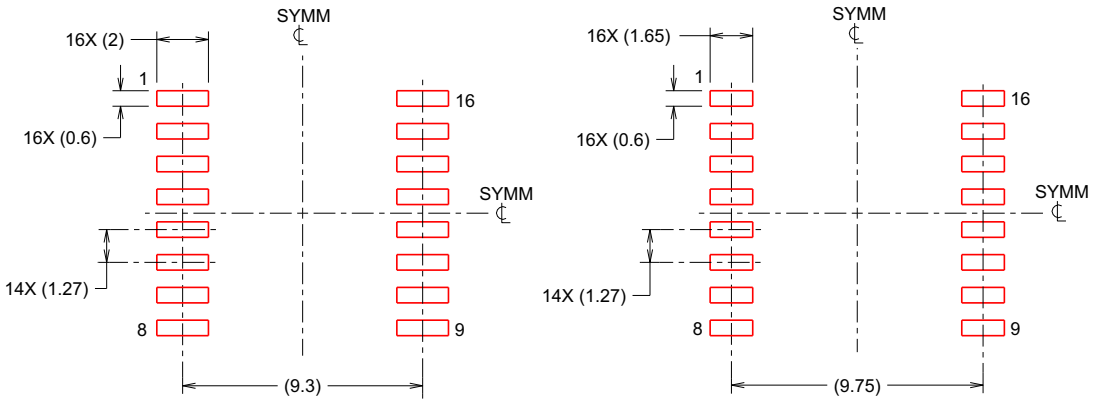
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DW0016B

SOIC - 2.65 mm max height

SOIC




IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/A 08/2013

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO5451QDWQ1 | LIFEBUY | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO5451Q | |
| ISO5451QDWRQ1 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO5451Q | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF ISO5451-Q1 :**

- Catalog : ISO5451

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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