具有相位同步功能且支持 JESD204B 的 LMX2615-SP 航空级 40MHz 至 15GHz 宽带合成器

1 特性

- 辐射规范
  - 单粒子闩锁 > 120MeV-cm^2/mg
  - 电离辐射总剂量达 100 krad(Si)
- 40MHz 至 15GHz 输出频率
- 在 100KHz 偏频和 15GHz 载波的情况下具有 -110dBc/Hz 的相位噪声
- 45在 8 GHz 时，具有 45fs RMS 抖动（100Hz 至 100MHz）
- 可编程输出功率
- PLL 主要规格
  - 品质因数：–236dBc/Hz
  - 标称 1/f 噪声：–129dBc/Hz
  - 相位检测器频率高达 200MHz
- 跨多个设备实现输出相位同步
- 支持具有 9ps 分辨率可编程延迟的 SYSREF
- 3.3V 单电源运行
- 71 种预选引脚模式
- 11 x 11 mm² 64 引线 CQFP 陶瓷封装
- 工作温度范围为 -55°C 至 +125°C
- 由 PLLatinum Sim 设计工具提供支持

2 应用

- 航空通信
- 天基雷达系统
- 相控阵天线和波束形成
- 高速数据转换器时钟（支持 JESD204B）

3 说明

LMX2615-SP 是一款集成有电压控制振荡器 (VCO) 和稳压器的高性能宽带锁相环 (PLL)，在无倍频器的情况，可输出 40MHz 至 15GHz 范围内的任意频率，从而无需使用 ½ 谐波滤波器。此器件上的 VCO 涵盖了整个倍频区间，因而频率覆盖度可完全低至 40MHz。品质因数为 -236dBc/Hz 的高性能 PLL 和高相位检测器频率可实现非常低的带内噪声和集成抖动。

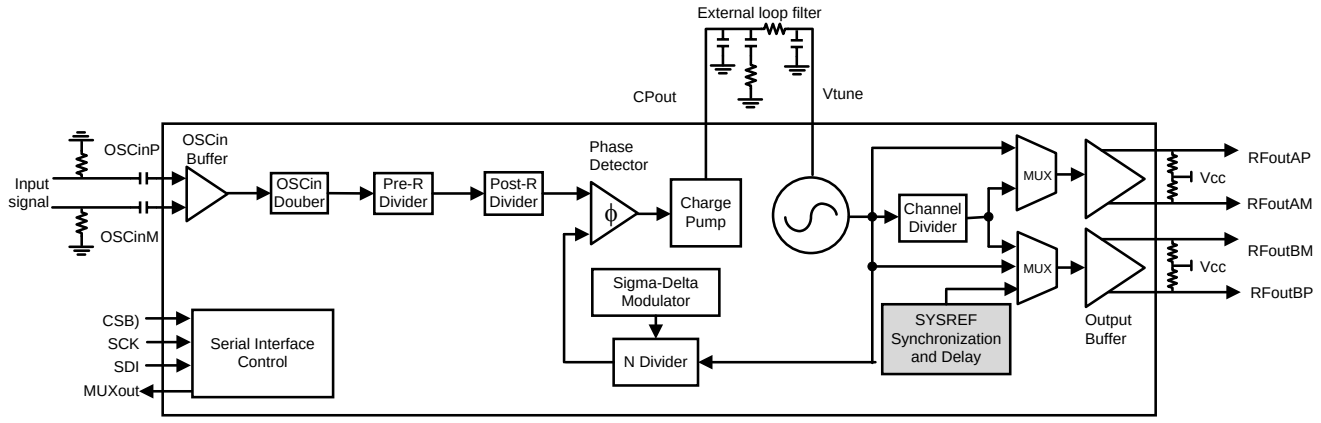
LMX2615-SP 允许用户同步多个器件实例的输出。这意味着我们可从任意应用情形下的器件中获得确定性相位，包括采用分数引擎或启用输出分频器的情形。该器件还可支持生成或重复 SYSREF（符合 JESD204B 标准），使其成为高速数据转换器的理想低噪声时钟源。

该器件采用德州仪器 (TI) 先进的 BiCMOS 工艺制造，可提供 64 引线 CQFP 陶瓷封装。

器件信息

器件编号	等级	封装
LMX2615W-MPR	非飞行用工程样片	64 引线 CQFP
LMX2615W-MLS	飞行用生产器件	64 引线 CQFP

简化原理图



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注：之前版本的页码可能与当前版本有所不同。

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- 已更改 output power, VCO Calibration time, and harmonics. ... 7
- 已添加 Typical Performance Characteristics ... 12
- 已更改 Updated Max Frequencies for higher divides to be based on 11.5 GHz, not 15.2 GHz ... 24
- 已添加 FS7 Pin description ... 34
- 已添加 Typical Application ... 60
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- 已添加 Layout Example ... 63

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- Changed Typical VCO Gain ... 9
- 已更改 readback timing diagram and added tCD. ... 11
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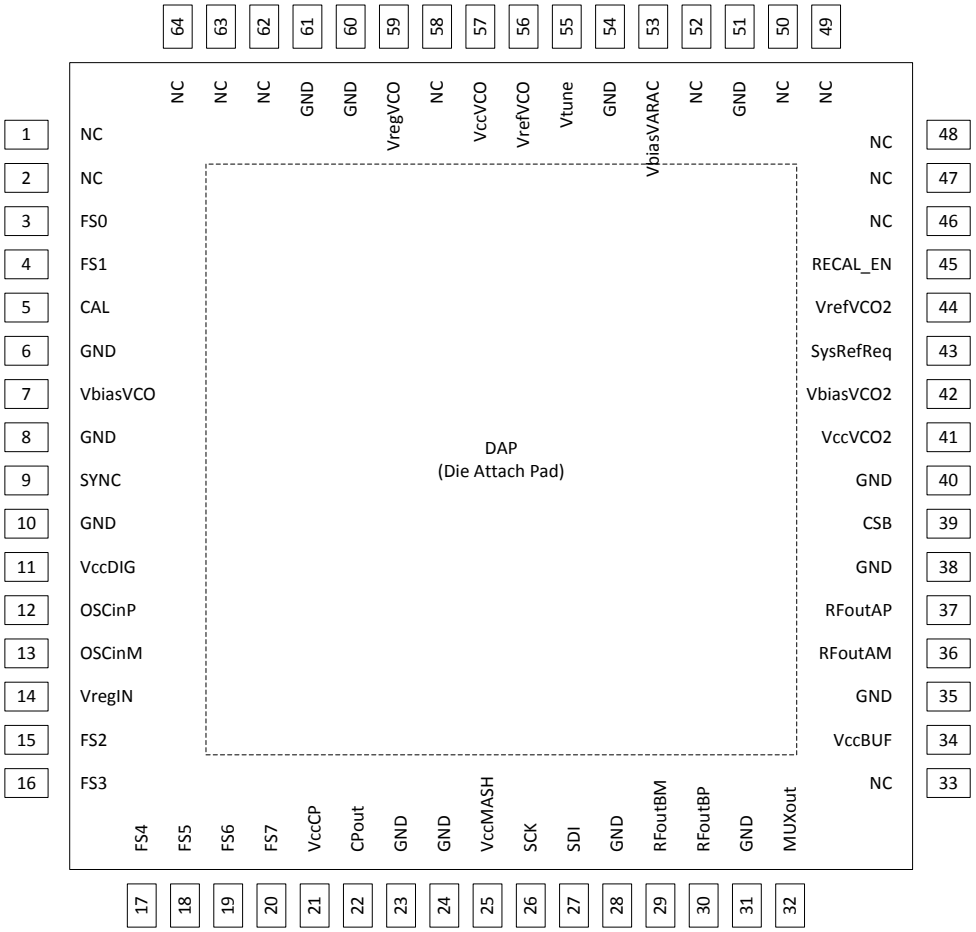
5 Pin Configuration and Functions

64-Pin CQFP
Top View



Pin Functions

CQFP Package (QFN) Pin Functions

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	NC	—	—	No connection. Pin may be grounded or left unconnected.
2	NC	—	—	No connection. Pin may be grounded or left unconnected.
3	FS0	I	—	Parallel pin control. This is the LSB.
4	FS1	I	—	Parallel pin control
5	CAL	I	—	Chip enable. In Pin Mode (not SPI Mode), rising edges presented to this pin activate the VCO calibration.
6	GND	—	—	Ground
7	VbiasVCO	—	—	VCO bias. Requires connecting 10uF capacitor to ground. Place close to pin.
8	GND	—	—	Ground
9	SYNC	I	—	Phase synchronization input pin.
10	GND	—	—	Ground
11	VccDIG	—	—	Digital supply. Recommend connecting 0.1uF capacitor to ground.
12	OSCinP	I	—	Complimentary Reference input clock pins. High input impedance. Requires connecting series capacitor (0.1 uF recommended).
13	OSCinM	I	—	Complimentary pin to OSCinP.
14	VregIN	—	—	Input reference path regulator decoupling. Requires connecting 1uF capacitor to ground. Place close to pin.
15	FS2	I	—	Parallel pin control
16	FS3	I	—	Parallel pin control
17	FS4	I	—	Parallel pin control
18	FS5	I	—	Parallel pin control
19	FS6	I	—	Parallel pin control
20	FS7	I	—	Parallel pin control. This is the MSB. Controls output state in pin mode. When this pin is low, only RFoutA is active, otherwise both outputs are active.
21	VccCP	—	—	Charge pump supply. Recommend connecting 0.1uF capacitor to ground.
22	CPout	O	—	Charge pump output. Recommend connecting C1 of loop filter close to charge pump pin.
23	GND	—	Ground	Ground
24	GND	—	Ground	Ground
25	VccMASH	—	—	Digital supply. Recommend connecting 0.1uF and 10uF capacitor to ground.
26	SCK	I	—	SPI input clock. High impedance CMOS input. 1.8 – 3.3V logic.
27	SDI	I	—	SPI input data. High impedance CMOS input. 1.8 – 3.3V logic.
28	GND	—	Ground	Ground
29	RFoutBM	O	—	Complementary pin for RFoutBP
30	RFoutBP	O	—	Differential output B Pair. Requires connecting a 50-Ω resistor pull-up to Vcc as close as possible to pin. Can be used as a synthesizer output or SYSREF output.
31	GND	—	Ground	Ground
32	MUXout	O	—	Multiplexed output pin. Can output: lock detect, SPI readback and diagnostics.
33	NC	—	—	No connection. Leave Unconnected
34	VccBUF	—	—	Output buffer supply. Requires connecting 0.1uF capacitor to ground.
35	GND	—	Ground	Ground
36	RFoutAM	O	—	Complementary pin for RFoutAP
37	RFoutAP	O	—	Differential output B Pair. Requires connecting a 50-Ω resistor pull-up to Vcc as close as possible to pin.
38	GND	—	Ground	Ground
39	CSB	I	—	SPI chip select bar. High impedance CMOS input. 1.8 – 3.3V logic.
40	GND	—	Ground	Ground

CQFP Package (QFN) Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
41	VccVCO2	—	—	VCO supply. Recommend connecting 0.1uF and 10uF capacitor to ground.
42	VbiasVCO2	—	—	VCO bias. Requires connecting 1uF capacitor to ground.
43	SysRefReq	I	—	SYSREF request input for JESD204B support.
44	VrefVCO2	—	—	VCO supply reference. Requires connecting 10uF capacitor to ground.
45	RECAL_EN	I	—	Enables the automatic recalibration feature.
46	NC	—	—	No connection. Pin may be grounded or left unconnected.
47	NC	—	—	No connection. Pin may be grounded or left unconnected.
48	NC	—	—	No connection. Pin may be grounded or left unconnected.
49	NC	—	—	No connection. Pin may be grounded or left unconnected.
50	NC	—	—	No connection. Pin may be grounded or left unconnected.
51	GND	—	Ground	Ground
52	NC	—	—	No connection. Pin may be grounded or left unconnected.
53	VbiasVARAC	—	—	VCO Varactor bias. Requires connecting 10uF capacitor to ground.
54	GND	—	Ground	Ground
55	Vtune	I	—	VCO tuning voltage input.
56	VrefVCO	—	—	VCO supply reference. Requires connecting 10uF capacitor to ground.
57	VccVCO	—	—	VCO supply. Recommend connecting 0.1uF and 10uF capacitor to ground.
58	NC	—	—	No connection. Leave Unconnected
59	VregVCO	—	—	VCO regulator node. Requires connecting 1uF capacitor to ground.
60	GND	—	Ground	Ground
61	GND	—	Ground	Ground
62	NC	—	—	No connection. Pin may be grounded or left unconnected.
63	NC	—	—	No connection. Pin may be grounded or left unconnected.
64	NC	—	—	No connection. Pin may be grounded or left unconnected.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Power supply voltage(1)	–0.3	3.6	V
V_{DIG}	Digital pin voltage (FS0-FS7,SYNC, SysRefReq,RECAL_EN,CAL)	-0.3	V_{CC}+0.3	V
$\|V_{OSCin}\|$	Differential AC voltage between OSCinP and OSCinN		2.1	Vpp
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V

(1) JEDEC document JEP155 states that 500 V HBM allows safemanufacturing with a standard ESD control process. Manufacturing with less than 500 V HBM ispossible with the necessary precautions. Pins listed as ±XXX V may actually have higherperformance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Power supply voltage	3.2	3.3	3.45	V
T_c	Case temperature	–55	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		CQFP 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (2)	7.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and ICPackage Thermal Metrics* application report.
(2) DAP

6.5 Electrical Characteristics

3.2 V ≤ V_{CC} ≤ 3.45 V, –55°C ≤ T_C ≤+125°C. Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{CC}	Supply voltage			3.2	3.3	3.45	V
I_{CC}	Supply current	OUTA_PD = 0, OUTB_PD = 1 OUTA_MUX = OUTB_MUX = 1 OUTA_PWR = 31, CPG=7 f_{OSC}= f_{PD} = 100 MHz, f_{VCO} = f_{OUT} = 14.5 GHz			360		mA
	Power on reset current	RESET=1			289		
	Power down current	POWERDOWN=1			6		
OUTPUT CHARACTERISTICS							
p_{OUT}	Single-ended output power(1) (2)	50-Ω resistor pullup OUTx_PWR = 31	f_{OUT} = 8 GHz		6		dBm
			f_{OUT} = 15 GHz		4		
INPUT SIGNAL PATH							
f_{OSCin}	Reference input frequency	OSC_2X = 0		5		1000	MHz
		OSC_2X = 1		5		200	
v_{OSCin}	Reference input voltage	Single-ended AC coupled sine wave input with complementary side AC coupled to ground with 50 Ω resistor	f_{OSCin}≥ 20 MHz	0.4		2	Vpp
			10 MHz ≤ f_{OSCin} <20 MHz	0.8		2	
			5 MHz ≤ f_{OSCin} <10 MHz	1.6		2	
PHASE DETECTOR AND CHARGE PUMP							
f_{PD}	Phase detector frequency(3)	MASH_ORDER=0		0.125		250	MHz
		MASH_ORDER>0		5		200	
I_{CPout}	Charge-pump leakage current	CPG = 0				15	nA
	Effective charge pump current. This is the sum of the up and down currents	CPG = 4			3		mA
		CPG = 1			6		
		CPG = 5			9		
		CPG = 3			12		
		CPG = 7			15		
$PN_{PLL\_1/f}$	Normalized PLL 1/f noise	f_{PD} = 100 MHz, f_{VCO} = 12 GHz(4)			–129		dBc/Hz
PN_{PLL_FOM}	Normalized PLL noise floor				–236		dBc/Hz

(1) Single ended output power obtained after de-embeddingmicrostrip trace losses and matching with a manual tuner. Unused port terminated to 50-Ωload.
(2) Output power, spurs, and harmonics can vary based on boardlayout and components.
(3) For lower VCO frequencies, the N divider minimum value canlimit the phase-detector frequency.
(4) The PLL noise contribution is measured using a clean referenceand a wide loop bandwidth and is composed into flicker and flat components. PLL_flat = PLL_FOM + 20× log(Fvco/Fpd) + 10 × log(Fpd / 1Hz). PLL_flicker (offset) = PLL_1/f + 20 × log(Fvco / 1GHz) – 10× log(offset / 10kHz). Once these two components are found, the total PLL noise can be calculatedas PLL_Noise = 10 × log(10 $^{PLL\_Flat / 10}$ + 10 $^{PLL\_flicker /10}$)

Electrical Characteristics (continued)

3.2 V ≤ V_{CC} ≤ 3.45 V, –55°C ≤ T_C ≤+125°C. Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VCO CHARACTERISTICS							
PN_{VCO}	VCO phase noise	VCO1 f_{VCO} = 8.1 GHz	100 kHz		-105		dBc/Hz
			1 MHz		-127		
			10 MHz		-148		
			100 MHz		-155		
		VCO2 f_{VCO} = 9.3 GHz	100 kHz		-103		
			1 MHz		-125		
			10 MHz		-146		
			100 MHz		-153		
		VCO3 f_{VCO} = 10.4 GHz	100 kHz		-103		
			1 MHz		-125		
			10 MHz		-147		
			100 MHz		-158		
		VCO4 f_{VCO} = 11.4 GHz	100 kHz		-101		
			1 MHz		-124		
			10 MHz		-146		
			100 MHz		-158		
		VCO5 f_{VCO} = 12.5 GHz	100 kHz		-102		
			1 MHz		-126		
			10 MHz		-147		
			100 MHz		-156		
		VCO6 f_{VCO} = 13.6 GHz	100 kHz		-101		
			1 MHz		-124		
			10 MHz		-146		
			100 MHz		-160		
		VCO7 f_{VCO} = 14.7 GHz	100 kHz		-101		
			1 MHz		-124		
			10 MHz		-146		
			100 MHz		-157		
t_{VCOCAL}	VCO calibration speed, switch across the entire frequency band, f_{OSC} = 100 MHz, f_{PD} = 100 MHz, f_{VCO} = 7.9 GHz,VCO_SEL=7	Partial assist			650		µs
K_{VCO}	VCO Gain	8.1 GHz			94		MHz/V
		9.3 GHz			106		
		10.4 GHz			122		
		11.4 GHz			148		
		12.5 GHz			185		
		13.6 GHz			202		
		14.7 GHz			233		
$\lvert\Delta T_{CL}\rvert$	Allowable temperature drift when VCO is not re-calibrated				125		°C
H2	VCO second harmonic	f_{VCO} = 8 GHz, divider disabled			–30		dBc
H3	VCO third haromonic	f_{VCO} = 8 GHz, divider disabled			-25		
DIGITAL INTERFACE **Applies to SCLK, SDI, CSB, CAL, RECAL_EN, MUXout, SYNC, SysRefReq**							
V_{IH}	High-level input voltage					1.6	V

Electrical Characteristics (continued)

3.2 V ≤ V_{CC} ≤ 3.45 V, –55°C ≤ T_C ≤+125°C. Typical values are at V_{CC} = 3.3 V, 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage			0.4			V
I_{IH}	High-level input current			–100		100	µA
I_{IL}	Low-level input current			–100		100	µA
V_{OH}	High-level output voltage	MUXout pin	Load current = –5 mA	V_{CC} – 0.6			V
V_{OL}	High-level output current		Load current = 5 mA			0.6	V

6.6 Timing Requirements

(3.2 V ≤ V_{CC} ≤ 3.45 V, –55°C ≤ T_A ≤+125°C, except as specified. Nominal values are at V_{CC} = 3.3 V,T_A = 25°C)

			MIN	NOM	MAX	UNIT
DIGITAL INTERFACE WRITE SPECIFICATIONS						
f_{SPI}Write	SPI write speed				2	MHz
t_{CE}	Clock to enable low time	See 图 1	50			ns
t_{CS}	Data to clock setup time		50			ns
t_{CH}	Data to clock hold time		50			ns
t_{CWH}	Clock pulse width high		200			ns
t_{CWL}	Clock pulse width low		200			ns
t_{CES}	Enable to clock setup time		100			ns
t_{EWH}	Enable pulse width high		100			ns

Timing Requirements (continued)

(3.2 V ≤ V_{CC} ≤ 3.45 V, –55°C ≤ T_A ≤+125°C, except as specified. Nominal values are at V_{CC} = 3.3 V,T_A = 25°C)

			MIN	NOM	MAX	UNIT
DIGITAL INTERFACE READBACK SPECIFICATIONS						
$f_{SPIReadback}$	SPI readback speed	See 图 2			2	MHz
t_{CE}	Clock to enable low time	See 图 2	50			ns
t_{CS}	Clock to data wait time	See 图 2	50			ns
t_{CWH}	Clock pulse width high	See 图 2	200			ns
t_{CWL}	Clock pulse width low	See 图 2	200			ns
t_{CES}	Enable to clock setup time	See 图 2	50			ns
t_{EWH}	Enable pulse width high	See 图 2	100			ns
t_{CD}	Falling clock edge to data wait time	See 图 2	200			ns

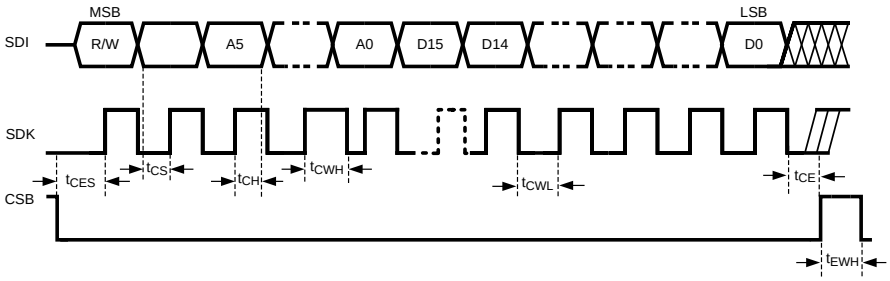


图 1. Serial Data Input Timing Diagram

There are several other considerations for writing on the SPI:

- The R/W bit must be set to 0.
- The data on SDI pin is clocked into a shift register on each rising edge on the SCK pin.
- The CSB must be held low for data to be clocked. Device will ignore clock pulses if CSB is held high.
- The CSB transition from high to low must occur when SCK is low.
- When SCK and SDI lines are shared between devices, TI recommends hold the CSB line high on the device that is not to be clocked.

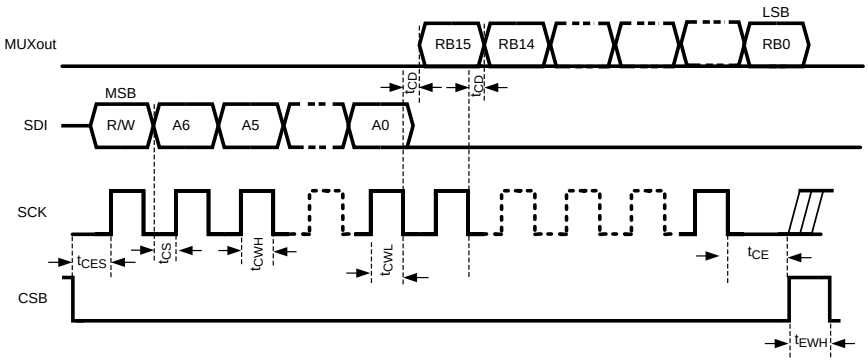
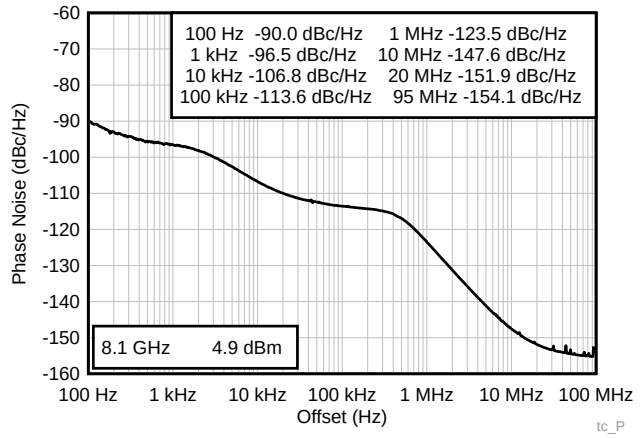


图 2. Serial Data Readback Timing Diagram

There are several other considerations for SPI readback:

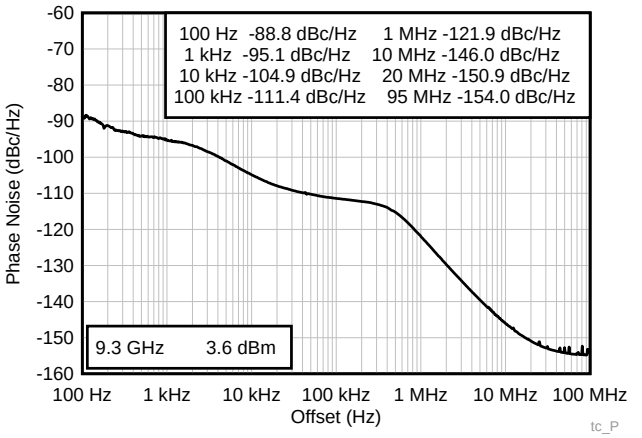
- The R/W bit must be set to 1.
- The MUXout pin will always be low for the address portion of the transaction.
- The data on MUXout becomes available momentarily after the falling edge of SCK and therefore should be read back on the rising edge of SCK.
- The data portion of the transition on the SDI line is always ignored.

6.7 Typical Characteristics



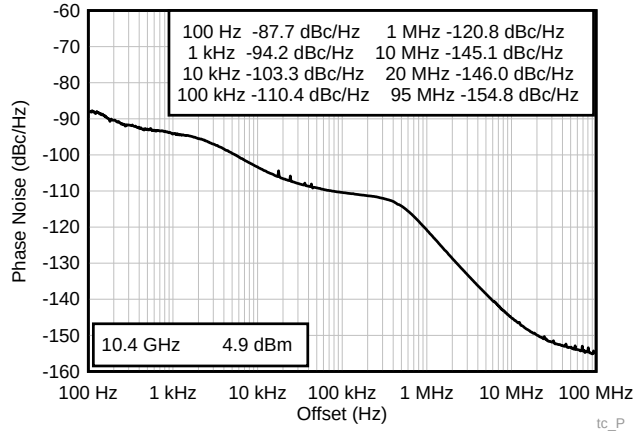
f_{OSC} = 100 MHz
f_{PD} = 200 MHz
Jitter = 53.0 fs (100 Hz - 100 MHz)

图 3. Closed Loop Phase Noise at 8.1 GHz



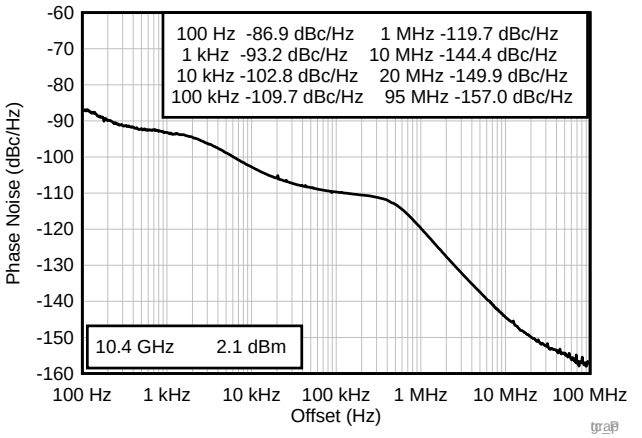
f_{OSC} = 100 MHz
f_{PD} = 200 MHz
Jitter = 56.7 fs (100 Hz - 100 MHz)

图 4. Closed Loop Phase Noise at 9.3 GHz



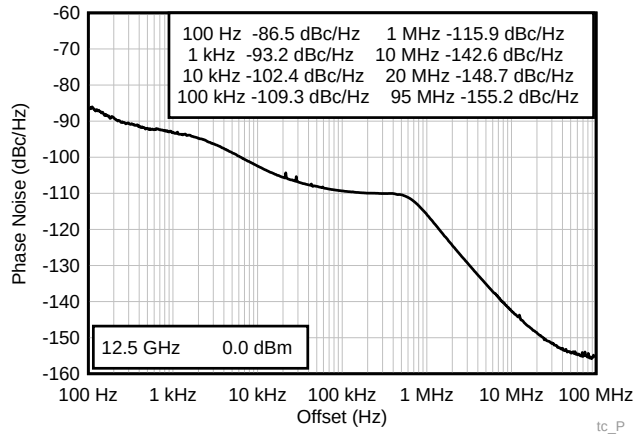
f_{OSC} = 100 MHz
f_{PD} = 200 MHz
Jitter = 57.6 fs (100 Hz - 100 MHz)

图 5. Closed Loop Phase Noise at 10.4 GHz



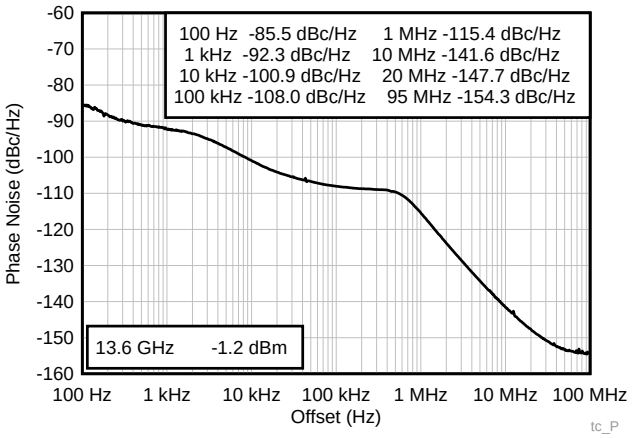
f_{OSC} = 100 MHz
f_{PD} = 200 MHz
Jitter = 57.8 fs (100 Hz - 100 MHz)

图 6. Closed Loop Phase Noise at 11.4 GHz



f_{OSC} = 100 MHz
f_{PD} = 200 MHz
Jitter = 62.4 fs (100 Hz - 100 MHz)

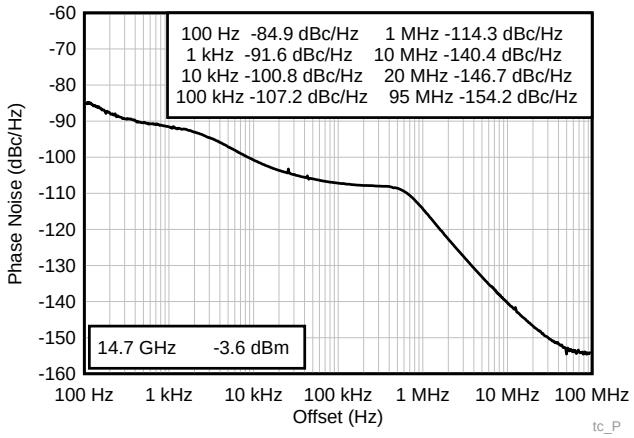
图 7. Closed Loop Phase Noise at 12.5 GHz



f_{OSC} = 100 MHz
f_{PD} = 200 MHz
f_{VCO} = 14 GHz
f_{OUT} = 14 GHz/2 = 3.5 GHz
Jitter = 64.2 fs (100 Hz - 100 MHz)

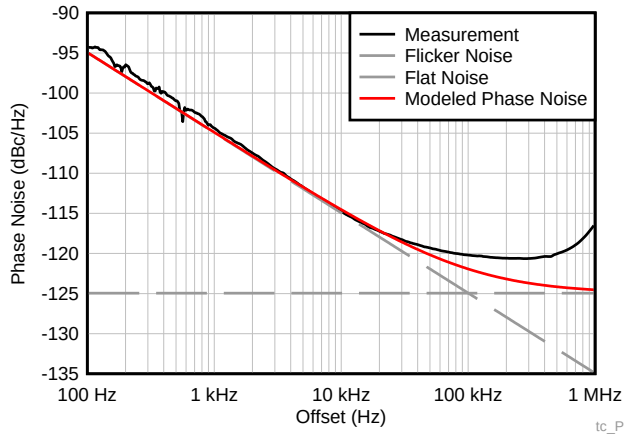
图 8. Closed Loop Phase Noise at 13.6 GHz

Typical Characteristics (接下页)



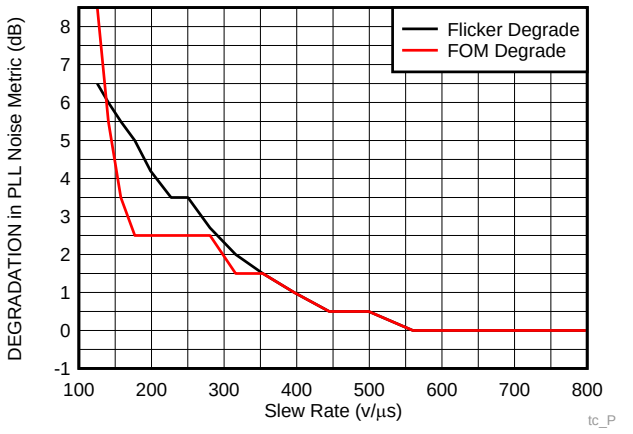
f_{OSC} = 100 MHz
f_{PD} = 200 MHz
Jitter = 65.5 fs (100 Hz - 100 MHz)

图 9. Closed Loop Phase Noise at 14.7 GHz



f_{VCO} = 10 GHz
FOM = -237.5
f_{PD} = 200 MHz
Flicker = -130.5

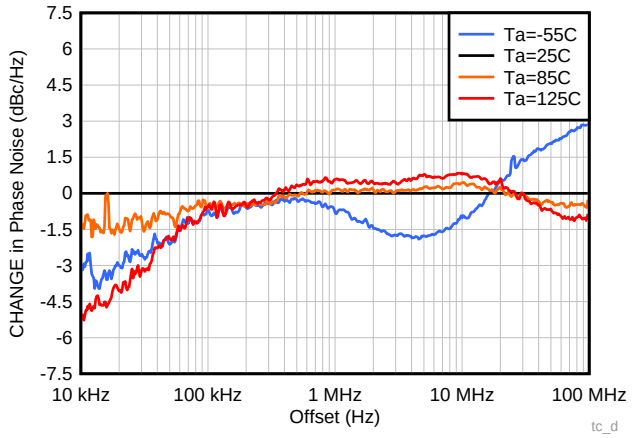
图 10. Calculation of PLL Noise Metrics



f_{OSC} = 200 MHz
f_{VCO} = 14.8 GHz

图 11. PLL Phase Noise Metrics vs. Fosc Slew Rate

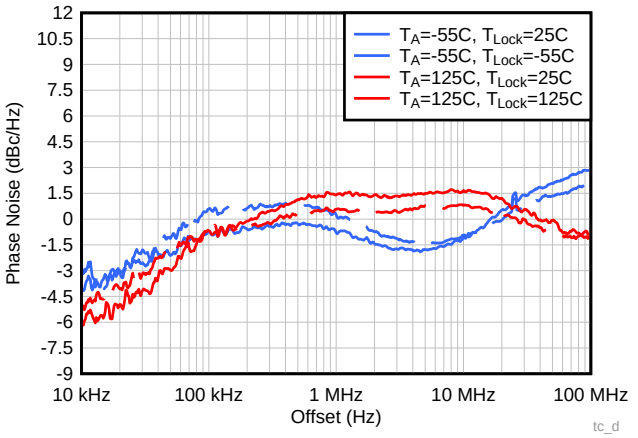
Typical Characteristics (接下页)



f_{VCO} = 10 GHz, Narrow Loop Bandwidth (<100 Hz)

VCO Re-Calibrated at Final Frequency

图 12. CHANGE in VCO Phase Noise Over Temperature



f_{VCO} = 10 GHz, Narrow Loop Bandwidth (<100 Hz)

VCO Calibrated at 25C and Temperature Drifted

图 13. CHANGE in 8 GHz VCO Phase Noise Over Temperature

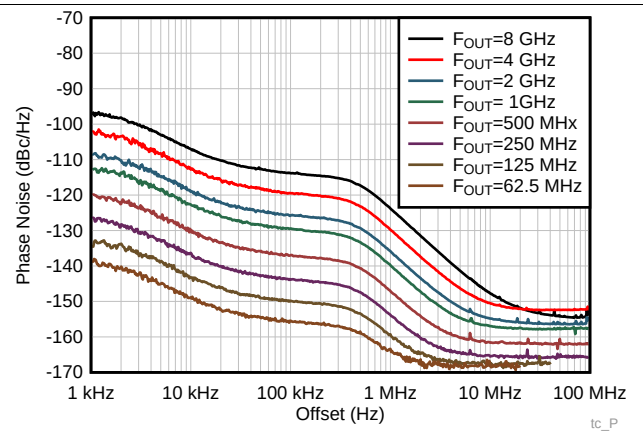
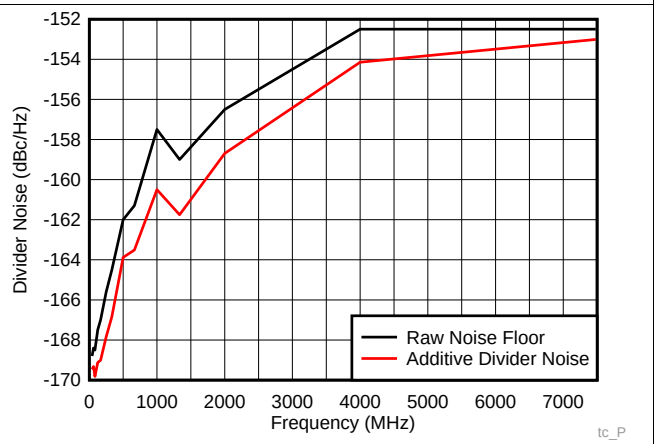


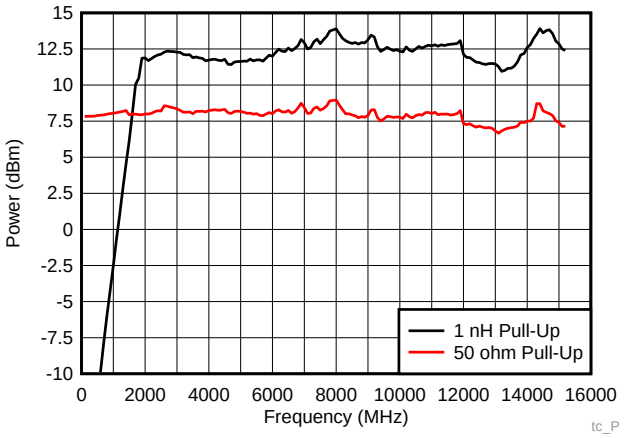
图 14. Divided Output Frequency



This noise adds to the scaled VCO Noise when the channel divider is used.

图 15. Additive VCO Divider Noise Floor

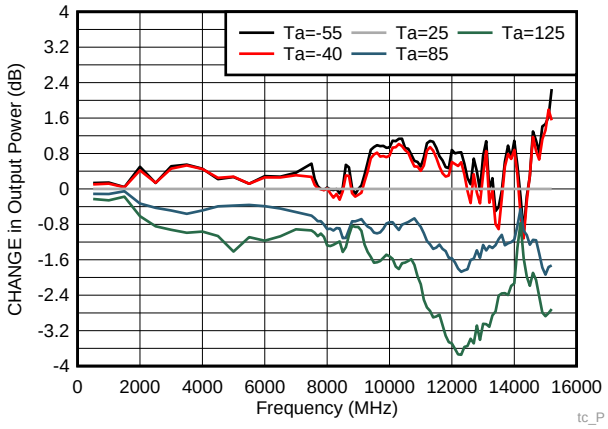
Typical Characteristics (接下页)



Single-Ended Output

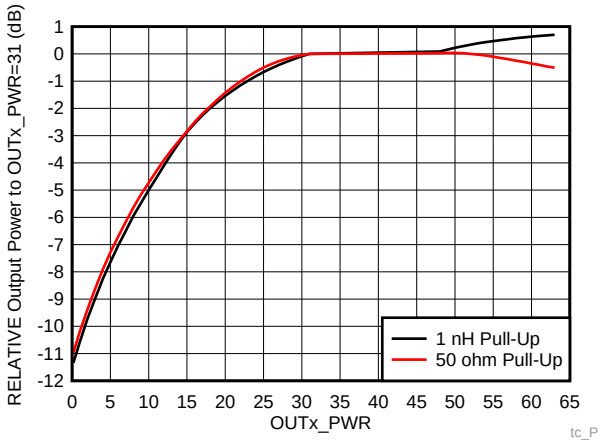
OUTx_PWR = 31

图 16. Output Power vs Pull-up



Single-ended output OUTx_PWR=31

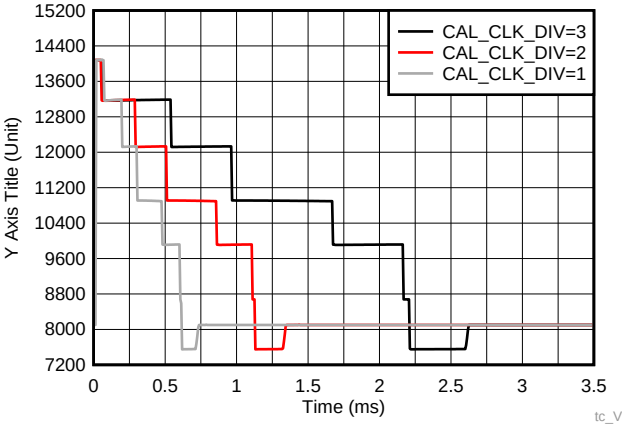
图 17. CHANGE in Output Power vs Temperature



Single-Ended Output

OUTx_PWR=31

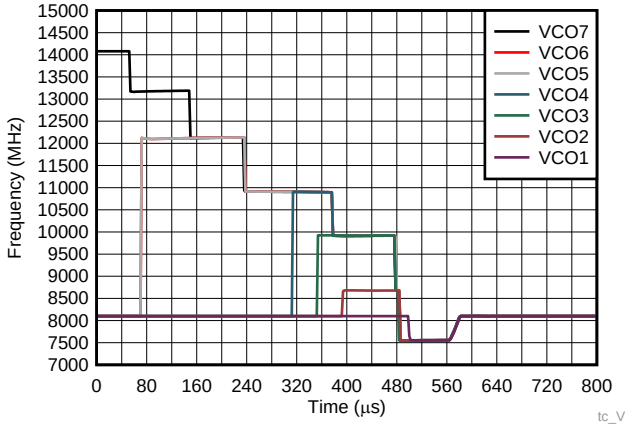
图 18. Impact of OUTx_PWR on Output Power



f_{OSC} = 100 MHz
f_{PD} = 200 MHz

VCO_SEL = VCO7
FCAL_HPFD_ADJ= 3

图 19. Impact of CAL_CLK_DIV on VCO Calibration Time

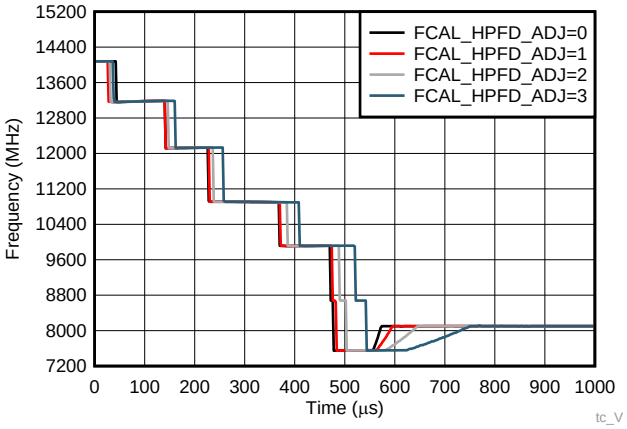


f_{OSC} = 100 MHz
f_{PD} = 200 MHz

FCAL_HPFD_ADJ= 2
CAL_CLK_DIV=2

图 20. Impact of VCO_SEL on VCO Calibration Time

Typical Characteristics (接下页)



f_{OSC} = 100 MHz
f_{PD} = 500 MHz

VCO_SEL=VCO7
CAL_CLK_DIV=2

图 21. Impact of FCAL_HPFD_ADJ on VCO Calibration Time

7 Detailed Description

7.1 Overview

The LMX2615 is a high-performance, wideband frequency synthesizer with integrated VCO and output divider. The VCO operates from 7600 to 15200 MHz and this can be combined with the output divider to produce any frequency in the range of 40 MHz to 15.2 GHz. Within the input path there are two dividers .

The PLL is fractional-N PLL with programmable delta-sigma modulator up to 4^{th} order. The fractional denominator is a programmable 32-bit long, which can provide fine frequency steps easily below 1-Hz resolution as well as be used to do exact fractions like 1/3, 7/1000, and many others.

For applications where deterministic or adjustable phase is desired, the SYNC pin can be used to get the phase relationship between the OSCin and RFout pins deterministic. Once this is done, the phase can be adjusted in very fine steps of the VCO period divided by the fractional denominator.

The ultra-fast VCO calibration is ideal for applications where the frequency must be swept or abruptly changed. The frequency can be manually programmed.

The JESD204B support includes using the RFoutB output to create a differential SYSREF output that can be either a single pulse or a series of pulses that occur at a programmable distance away from the rising edges of the output signal.

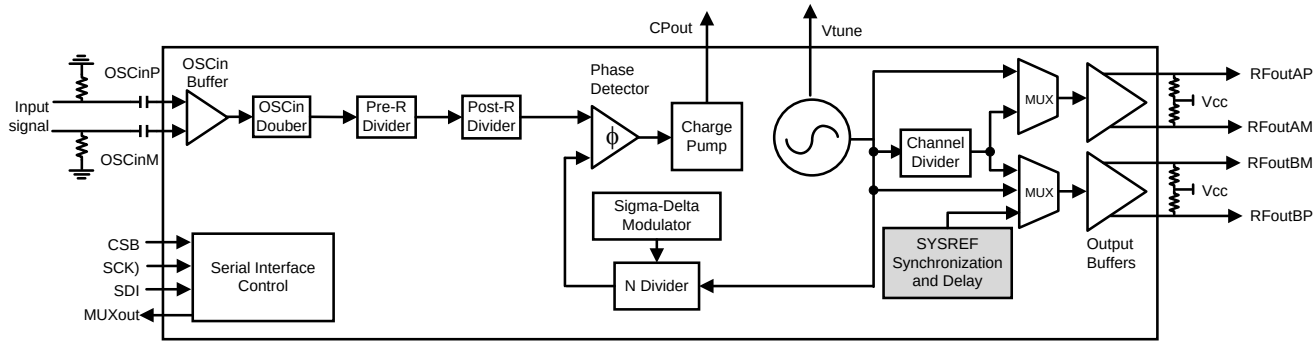
The LMX2615 device requires only a single 3.3 V power supply. The internal power supplies are provided by integrated LDOs, eliminating the need for high performance external LDOs.

表 1 shows the range of several of the doubler, dividers, and fractional settings.

表 1. Range of Doubler, Divider, and Fractional Settings

PARAMETER	MIN	MAX	COMMENTS
Outputs enabled	0	2	
OSCin doubler	0 (1X)	1 (2X)	The low noise doubler can be used to increase the phase detector frequency to improve phase noise and avoid spurs. This is in reference to the OSC_2X bit.
Pre-R divider	1 (bypass)	128	Only use the Pre R divider if the input frequency is too high for the Post R divider.
Post-R divider	1 (bypass)	255	The maximum input frequency for the post-R divider is 250 MHz. Use the Pre R divider if necessary.
N divider	≥ 28	524287	The minimum divide depends on modulator order and VCO frequency. See *N Divider and Fractional Circuitry* for more details.
Fractional numerator/ denominator	1 (Integer mode)	$2^{32} – 1 = 4294967295$	The fractional denominator is programmable and can assume any value between 1 and $2^{32}–1$; it is not a fixed denominator.
Fractional order	0	4	Order 0 is integer mode and the order can be programmed
Channel divider	1 (bypass)	192	This is the series of several dividers. Also, be aware that above 10 GHz, the maximum allowable channel divider value is 6.
Output frequency	40 MHz	15 GHz	This is implied by the minimum VCO frequency divided by the maximum channel divider value.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reference Oscillator Input

The OSCin pins are used as a frequency reference input to the device. The input is high impedance and requires AC-coupling caps at the pin. The OSCin pins can be driven single-ended with a CMOS clock or XO. Differential clock input is also supported, making it easier to interface with high-performance system clock devices such as TI's LMK series clock devices. As the OSCin signal is used as a clock for the VCO calibration, a proper reference signal must be applied at the OSCin pin at the time of programming FCAL_EN.

7.3.2 Reference Path

The reference path consists of an OSCin doubler (OSC_2X), Pre-R divider, and a Post-R divider.

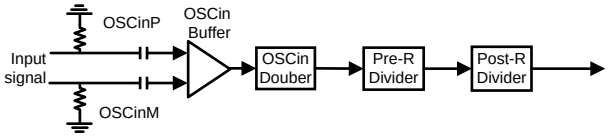


图 22. Reference Path Diagram

The OSCin doubler (OSC_2X) can double up low OSCin frequencies. Pre-R (PLL_R_PRE) and Post-R (PLL_R) dividers both divide frequency down. The phase detector frequency, f_{PD}, is calculated as follows:

$$f_{PD} = f_{OSC} \times OSC\_2X / (PLL\_R\_PRE \times PLL\_R) \quad (1)$$

- If the OSCin doubler is used, the OSCin signal should have a 50% duty cycle as both the rising and falling edges are used.
- If the OSCin doubler is not used, only rising edges of the OSCin signal are used and duty cycle is not critical.

Feature Description (接下页)

7.3.2.1 OSCin Doubler (OSC_2X)

The OSCin doubler allows one to double the input reference frequency up to 400 MHz while adding minimal noise. In some situations it may be advantageous to use the doubler to go to a higher frequency than the maximum phase detector frequency because the Pre-R divider may be able to divide down this frequency to phase detector frequency that is advantageous for fractional spurs.

7.3.2.2 Pre-R Divider (PLL_R_PRE)

The pre-R divider is useful for reducing the input frequency to help meet the maximum 250 MHz input frequency limitation to the PLL-R divider. Otherwise, it does not have to be used.

7.3.2.3 Post-R Divider (PLL_R)

The post-R divider can be used to further divide down the frequency to the phase detector frequency. When it is used (PLL_R > 1), the input frequency to this divider is limited to 250 MHz.

7.3.3 State Machine Clock

The state machine clock is a divided down version of the OSCin signal that is used internally in the device. This divide value 1,2,4, 8, or 16 and is determined by CAL_CLK_DIV programming word (described in the programming section). This state machine clock impacts various features like the VCO calibration and ramping. The state machine clock is calculated as fsmclk = f_{OSC} / $2^{CAL\_CLK\_DIV}$.

7.3.4 PLL Phase Detector and Charge Pump

The phase detector compares the outputs of the Post-R divider and N divider and generates a correction current corresponding to the phase error until the two signals are aligned in phase. This charge-pump current is software programmable to many different levels, allowing modification of the closed loop bandwidth of the PLL. See application section on phase noise due to the charge pump.

7.3.5 N Divider and Fractional Circuitry

The N divider includes fractional compensation and can achieve any fractional denominator from 1 to (2^{32} – 1). The integer portion of N is the whole part of the N divider value, and the fractional portion, N_{frac} = NUM / DEN, is the remaining fraction. In general, the total N divider value is determined by N + NUM / DEN. The N, NUM and DEN are software programmable. The higher the denominator, the finer the resolution step of the output. For example, even when using f_{PD} = 200 MHz, the output can increment in steps of 200 MHz /(2^{32}- 1) = 0.047 Hz. 公式 2 shows the relationship between the phase detector and VCO frequencies. Note that in SYNC mode, there is an extra divider that is not shown in 公式 2.

$$f_{VCO} = f_{pd} \times \left(N + \frac{NUM}{DEN} \right) \quad (2)$$

The sigma-delta modulator that controls this fractional division is also programmable from integer mode to fourth order. To make the fractional spurs consistent, the modulator is reset any time that the R0 register is programmed.

The N divider has minimum value restrictions based on the modulator order and VCO frequency. Furthermore, the PFD_DLY_SEL bit must be programmed in accordance to the 表 2. In SYNC mode, IncludedDivide may be larger than one, otherwise it is just one.

Feature Description (接下页)

表 2. Minimum N Divider Restrictions

FRAC_ORDER	f_{VCO} / IncludedDivide (MHz)	MINIMUM N	PFD_DLY_SEL
0	≤ 12500	29	1
	> 12500	33	2
1	≤ 10000	30	1
	10000-12500	34	2
	>12250	38	3
2	≤ 4000 (SYNC Mode)	31	1
	4000-7500 (SYNC Mode)	31	2
	7500 - 10000	32	2
	>10000	36	3
3	≤ 4000 (SYNC Mode)	33	1
	4000-7500 (SYNC Mode)	37	2
	7500 - 10000	41	3
	>10000	45	4
4	≤ 4000 (SYNC Mode)	45	3
	4000-7500 (SYNC Mode)	49	4
	7500-10000	53	5
	>10000	57	6

7.3.6 MUXout Pin

The MUXout pin can be configured as lock detect indicator for the PLL or as an serial data output (SDO) for the SPI interface to readback registers. Field MUXOUT_LD_SEL (register R0[2]) configures this output

表 3. MUXout Pin Configurations

MUXOUT_LD_SEL	FUNCTION
0	Serial data output for readback
1	Lock detect indicator

When lock detect indicator is selected, there are two types of indicator and they can be selected with the field LD_TYPE (register R59[0]). The first indicator is called “VCOCal” (LD_TYPE=0) and the second indicator is called “Vtune and VCOCal” (LD_TYPE=1).

7.3.6.1 Serial data output for readback

In this mode, the MUXout pin become the serial data output of the SPI interface. This output cannot be tri-stated so no line sharing is possible. Details of this pin operation are described with the serial interface description. Readback is very useful when a device is used is full assist mode and VCO calibration data are retrieve and saved for future use. It can also be used to read back the lock detect status using the field rb_LD_VTUNE(register R110[10:9]).

7.3.6.2 Lock detect indicator set as type “VCOCal”

In this mode the MUXout pin is will be low when the VCO is being calibrated or the lock detect delay timer is running, otherwise it will be high. The programmable timer (LD_DLY, register R60[15:0]) adds an additional delay after the VCO calibration finishes before the lock detect indicator is asserted high. LD_DLY is a 16 bit unsigned quantity that corresponds to the number of phase detector cycles in absolute delay. For example, a phase detector frequency of 100 MHz and the LD_DLY=10000 will add a delay of 100 usec before the indicator is asserted. This indicator will remain in its current state (high or low) until register R0 is programmed with FCAL_EN=1 with a valid input reference. In other words, if the PLL goes out of lock or the input reference goes away when the current state is high, then the current state will remain high.

7.3.6.3 Lock detect indicator set as type "Vtune and VCOCal"

In this mode the MUXout pin is will be high when the VCO calibration has finished, the lock detect delay timer is finished running, and the PLL is locked. This indicator may remain in its current state (high or low) if the OSCin signal is lost. The true status of the indicator will be updated and resume its operation only when a valid input reference to the OSCin pin is returned. An alternative method to monitor the OSCin of the PLL is recommended. This indicator is reliable as long as the reference to OSCin is present.

The output of the device can be automatically muted when lock detect indicator "Vtune and VCOCal" is low. This feature is enabled with the field OUT_MUTE (register R0[9]) asserted.

7.3.7 VCO (Voltage Controlled Oscillator)

The LMX2615 includes a fully integrated VCO. The VCO takes the voltage from the loop filter and converts this into a frequency. The VCO frequency is related to the other frequencies and as follows:

$$f_{VCO} = f_{PD} \times \text{N divider} \times \text{N Included Divide} \quad (3)$$

7.3.7.1 VCO Calibration

To reduce the VCO tuning gain and therefore improve the VCO phase-noise performance, the VCO frequency range is divided into several different frequency bands. The entire range, 7600 to 15200 MHz, covers an octave that allows the divider to take care of frequencies below the lower bound. This creates the need for frequency calibration to determine the correct frequency band given a desired output frequency. The frequency calibration routine is activated any time that the R0 register is programmed with the FCAL_EN = 1. It is important that a valid OSCin signal must present before VCO calibration begins.

The VCO also has an internal amplitude calibration algorithm to optimize the phase noise which is also activated any time the R0 register is programmed.

The optimum internal settings for this are temperature dependent. If the temperature is allowed to drift too much without being re-calibrated, some minor phase noise degradation could result. The maximum allowable drift for continuous lock, ΔT_{CL}, is stated in the electrical specifications. For this device, a number of 125°C means the device never loses lock if the device is operated under recommended operating conditions.

The LMX2615 allows the user to assist the VCO calibration. In general, there are three kinds of assistance, as shown in 表 4:

表 4. Assisting the VCO Calibration Speed

ASSISTANCE LEVEL	DESCRIPTION	VCO_SEL	VCO_SEL_FORCE VCO_CAPCTRL_FORCE VCO_DACISET_FORCE	VCO_CAPCTRL VCO_DACISET
No assist	User does nothing to improve VCO calibration speed.	7	0	Dont Care
Partial assist	Upon every frequency change, before the FCAL_EN bit is checked, the user provides the initial starting VCO_SEL	Choose by table	0	Don't Care
Full assist	The user forces the VCO core (VCO_SEL), amplitude settings (VCO_DACISET), and frequency band (VCO_CAPCTRL) and manually sets the value.	Choose by readback	1	Choose by readback

For the no assist method, just set VCO_SEL=7 and this is done. For partial assist, the VCO calibration speed can be improved by changing the VCO_SEL bit according to the frequency. Note that the frequency is not the actual VCO core range, but actually favors choosing the VCO. This is not only optimal for VCO calibration speed, but required for reliable locking.

表 5. Minimum VCO_SEL for Partial Assist

f_{VCO}	VCO Core (min)
7600 - 8740 MHz	VCO1
8740 - 10000 MHz	VCO2
10000 - 10980 MHz	VCO3
10980 -12100 MHz	VCO4
12100 - 13080 MHz	VCO5
13080 - 14180 MHz	VCO6
14180 - 15200 MHz	VCO7

For fastest calibration time, it is ideal to use the minimum VCO core as recommended in the previous table. The following table shows typical VCO calibration times for this choice in bold as well as showing how long the calibration time is increased if a higher than necessary VCO core is chosen. Realize that these calibration times are specific to these f_{OSC} and f_{PD} conditions specified and at the boundary of two cores, sometimes the calibration time can be increased.

表 6. Typical Calibration times for f_{OSC} = f_{PD} = 100 MHz based on VCO_SEL

f_{VCO}	VCO_SEL						
	VCO7	VCO6	VCO5	VCO4	VCO3	VCO2	VCO1
8.1 GHz	650	540	550	440	360	230	**110**
9.3 GHz	610	530	540	430	320	**220**	Invalid
10.4 GHz	590	520	530	430	**240**	Invalid	
11.4 GHz	340	290	280	**180**	Invalid		
12.5 GHz	270	170	**120**	Invalid			
13.6 GHz	240	**130**	Invalid				
14.7 GHz	**160**	Invalid					

7.3.7.2 Watchdog Feature

The watchdog feature is used to the scenario when radiation during VCO calibration from causes the VCO calibration to fail. When this feature is enabled, the watchdog timer will run during VCO calibration. If this timer runs out before the VCO calibration is finished, then the VCO calibration will be re-started. The WD_DLY word sets how many times this calibration may be restarted by the watchdog feature.

7.3.7.3 RECAL Feature

The RECAL feature is used to mitigate the scenario when the VCO is in lock, but then radiation causes it to go out of lock. When the RECAL_EN pin is high, if the PLL loses lock and stays out of lock for a time specified by the LD_DLY word, then it will trigger a VCO re-calibration.

7.3.7.4 Determining the VCO Gain

The VCO gain varies between the seven cores and is the lowest at the lowest end of the band and highest at the highest end of each band. For a more accurate estimation, use 表 7:

表 7. VCO Gain

f1	f2	Kvco1	Kvco2
7600	8740	78	114
8740	10000	91	125
10000	10980	112	136
10980	12100	136	168
12100	13080	171	206
13080	14180	188	218
14180	15200	218	248

Based in this table, the VCO gain can be estimated for an arbitrary VCO frequency of f_{VCO} as:

$$Kvco = Kvco1 + (Kvco2-Kvco1) \times (f_{VCO} – f1) / (f2 – f1) \quad (4)$$

7.3.8 Channel Divider

To go below the VCO lower bound of 7600 MHz, the channel divider can be used. The channel divider consists of four segments, and the total division value is equal to the multiplication of them. Therefore, not all values are valid.

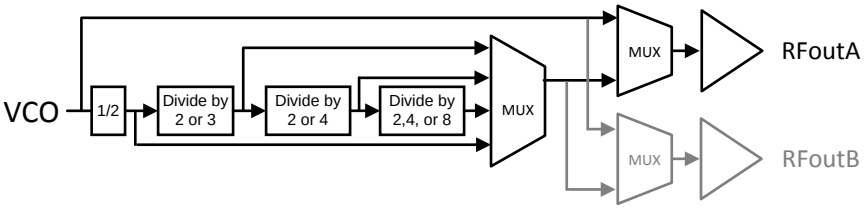


图 23. Channel Divider

When the channel divider is used, there are limitations on the values. 表 8 shows how these values are implemented and which segments are used.

表 8. Channel Divider Segments

EQUIVALENT DIVISION VALUE	FREQUENCY LIMITATION	OutMin (MHz)	OutMax (MHz)	CHDIV[4:0]	SEG0	SEG1	SEG2	SEG3
2	None	3800	7600	0	2	1	1	1
4		1900	3800	1	2	2	1	1
6		1266.667	2533.333	2	2	3	1	1
8	$f_{VCO} \leq 11.5$ GHz	950	1437.5	3	2	2	2	1
12		633.333	958.333	4	2	3	2	1
16		475	718.75	5	2	2	4	1
24		316.667	469.167	6	2	3	4	1
32		237.5	359.375	7	2	2	8	1
48		158.333	239.583	8	2	3	8	1
64		118.75	179.688	9	2	2	8	2
72		105.556	159.722	10	2	3	6	2
96		79.167	119.792	11	2	3	8	2
128		59.375	89.844	12	2	2	8	4
192		39.583	59.896	13	2	3	8	4
Invalid	n/a	n/a	n/a	14-31	n/a	n/a	n/a	n/a

The channel divider is powered up whenever an output (OUTx_MUX) is selected to the channel divider or SysRef, regardless of whether it is powered down or not. When an output is not used, TI recommends selecting the VCO output to ensure that the channel divider is not unnecessarily powered up.

表 9. Channel Divider

OUTA MUX	OUTB MUX	CHANNEL DIVIDER
Channel Divider	X	Powered up
X	Channel Divider or SYSREF	Powered up
All Other Cases		Powered down

7.3.9 Output Buffer

The RF output buffer type is open collector and requires an external pull-up to Vcc. This component may be a 50-Ω resistor or an inductor. The inductor has less controlled impedance, but higher power. For the inductor case, it is often helpful to follow this with a resistive pad. The output power can be programmed to various levels or disabled while still keeping the PLL in lock. If using a resistor, limit OUTx_PWR setting to 31; higher than this tends to actually reduce power. Note that states 32 through 47 are redundant and should be ignored. In other words, after state 31, the next higher power setting is 48.

表 10. OUTx_PWR Recommendations

f_{OUT}	Restrictions	Comments
10 MHz ≤ f_{OUT} ≤ 5 GHz	None	At lower frequencies, the output buffer impedance is high, so the 50-Ω pull-up will make the output impedance look somewhat like 50-Ω. Typically, maximum output power is near a setting of OUTx_PWR=50.
5 GHz < f_{OUT} ≤ 10 GHz	OUTx_PWR ≤ 31	In this range, parasitic inductances have some impact, so the output setting is restricted.
10 GHz < f_{OUT}	OUTx_PWR ≤ 20	At these higher frequency ranges, it is best to keep below 20 for highest power and optimal noise floor.

7.3.10 Powerdown Modes

The LMX2615 can be powered up and down using the CAL Pin or the POWERDOWN bit. When the device comes out of the powered down state, either by resuming the POWERDOWN bit to zero or by pulling back CAL Pin HIGH (if it was powered down by CAL Pin), register R0 must be programmed with FCAL_EN high again to re-calibrate the device.

7.3.11 Treatment of Unused Pins

This device has several pins for many features and there is a preferred way to treat these pins if not needed. For the input pins, a series resistor is recommend, but they can be directly shorted.

表 11. Recommended Treatment of Pins

Pins	SPI Mode	Pin Mode	Recommended Treatment if NOT Used
FS0,FS1,FS2,FS3,FS4,FS5,FS6,FS7	Never Used	Always Used	GND with 1 kΩ.
CAL	Never Used	Sometimes Used	VCC with 1 kΩ
SYNC, SysRefReq	Sometimes Used	Never Used	GND with 1 kΩ
OSCinP,OSCinM	Always Used	Always Used	GND with 50 Ω to ground after AC coupling Cap. If one side of complimentary side is used and other side is not, impedance looking out should be similar for both of these pins.
SCK, SDI	Always Used	Never Used	GND with 1 kΩ
CSB	Always Used	Never Used	VCC with 1 kΩ
RECAL_EN	Sometimes Used	Sometimes Used	Internally pulled to VCC with 200 kΩ
RFoutXX	Sometimes Used	Sometimes Used	VCC with 50 Ω. If one side of complimentary side is used and the other side is not, impedance looking out should be similar for both of these pins.
MUXOUT	Sometimes Used	Sometimes Used	GND with 10 kΩ

7.3.12 Phase Synchronization

7.3.12.1 General Concept

The SYNC pin allows one to synchronize the LMX2615 such that the delay from the rising edge of the OSCin signal to the output signal is deterministic. Initially, the devices are locked to the input, but are not synchronized. The user sends a synchronization pulse that is reclocked to the next rising edge of the OSCin pulse. After a given time, t_1, the phase relationship from OSCin to f_{OUT} will be deterministic. This time is dominated by the sum of the VCO calibration time, the analog setting time of the PLL loop, and the MASH_RST_CNT if used in fractional mode.

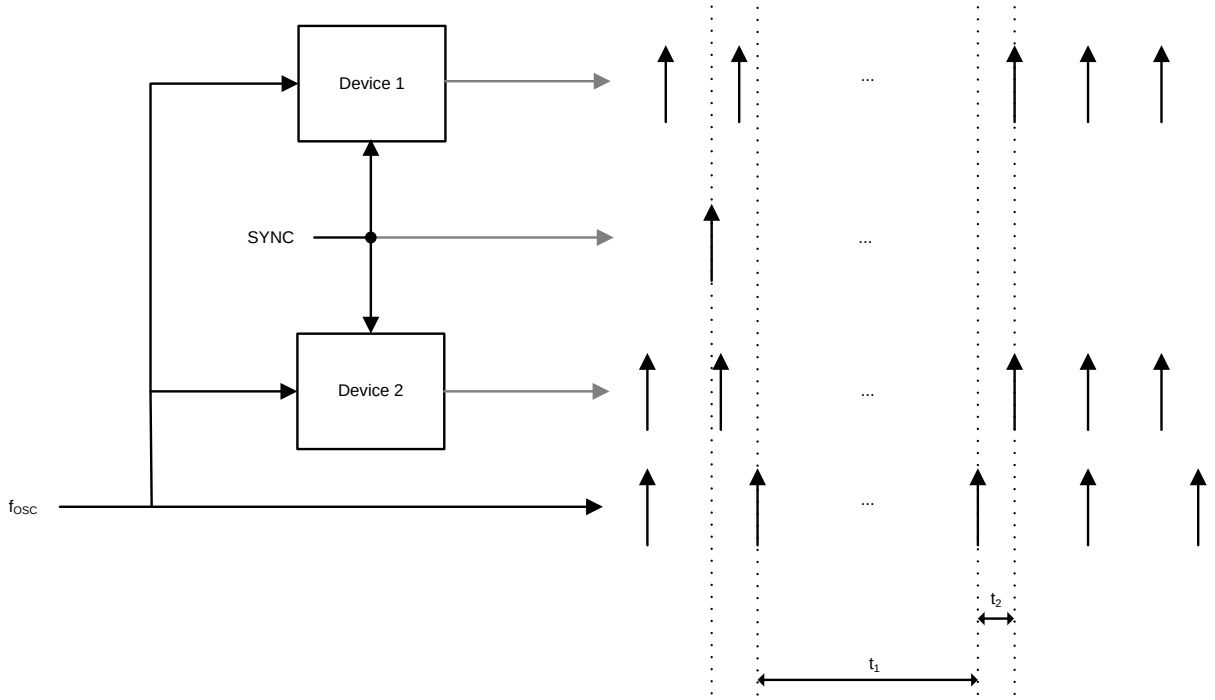


图 24. Devices Are Now Synchronized to OSCin Signal

When the SYNC feature is enabled, part of the channel divide may be included in the feedback path.

表 12. IncludedDivide with VCO_PHASE_SYNC = 1

OUTx_MUX	CHANNEL DIVIDER	IncludedDivide
OUTA_MUX = OUTB_MUX = 1 ("VCO")	Don't Care	1
All Other Valid Conditions	Divisible by 3, but NOT 24 or 192	SEG0 × SEG1 = 6
	All other values	SEG0 × SEG1 = 4

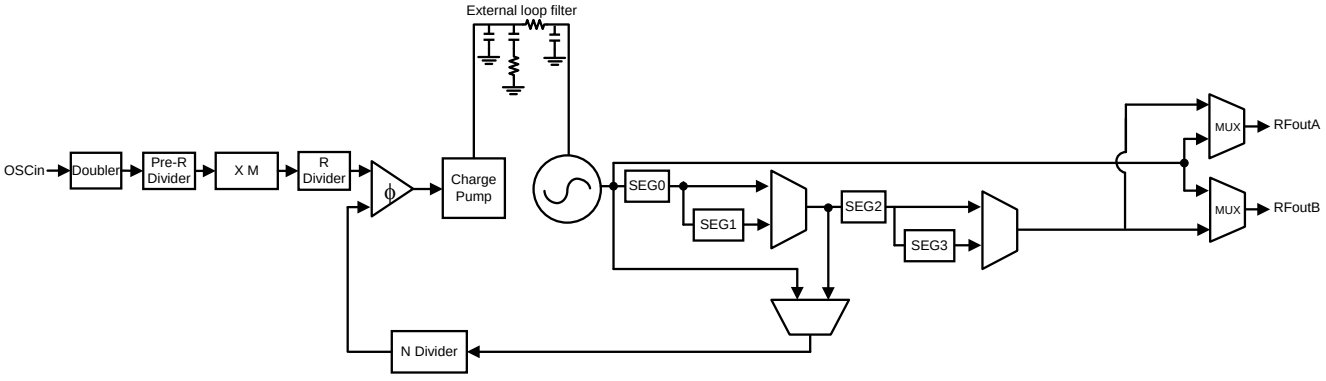


图 25. Phase SYNC Diagram

7.3.12.2 Categories of Applications for SYNC

The requirements for SYNC depend on certain setup conditions. In cases that the SYNC is not timing critical, it can be done through software by toggling the VCO_PHASE_SYNC bit from 0 to 1. The 图 26 gives the different categories. When it is timing critical, then it must be done through the pin and the setup and hold times for the OSCin pin are critical. For timing critical sync (Category 3) ONLY, adhere to the following guidelines.

表 13. SYNC Pin Timing Characteristics for Category 3 SYNC

Parameter	Description	Min	Max	Unit
f_{OSC}	Input reference Frequency		40	MHz
t_{SETUP}	Setup time between SYNC and OSCin rising edges	2.5		ns
t_{HOLD}	Hold time between SYNC and OSCin rising edges	2.5		ns

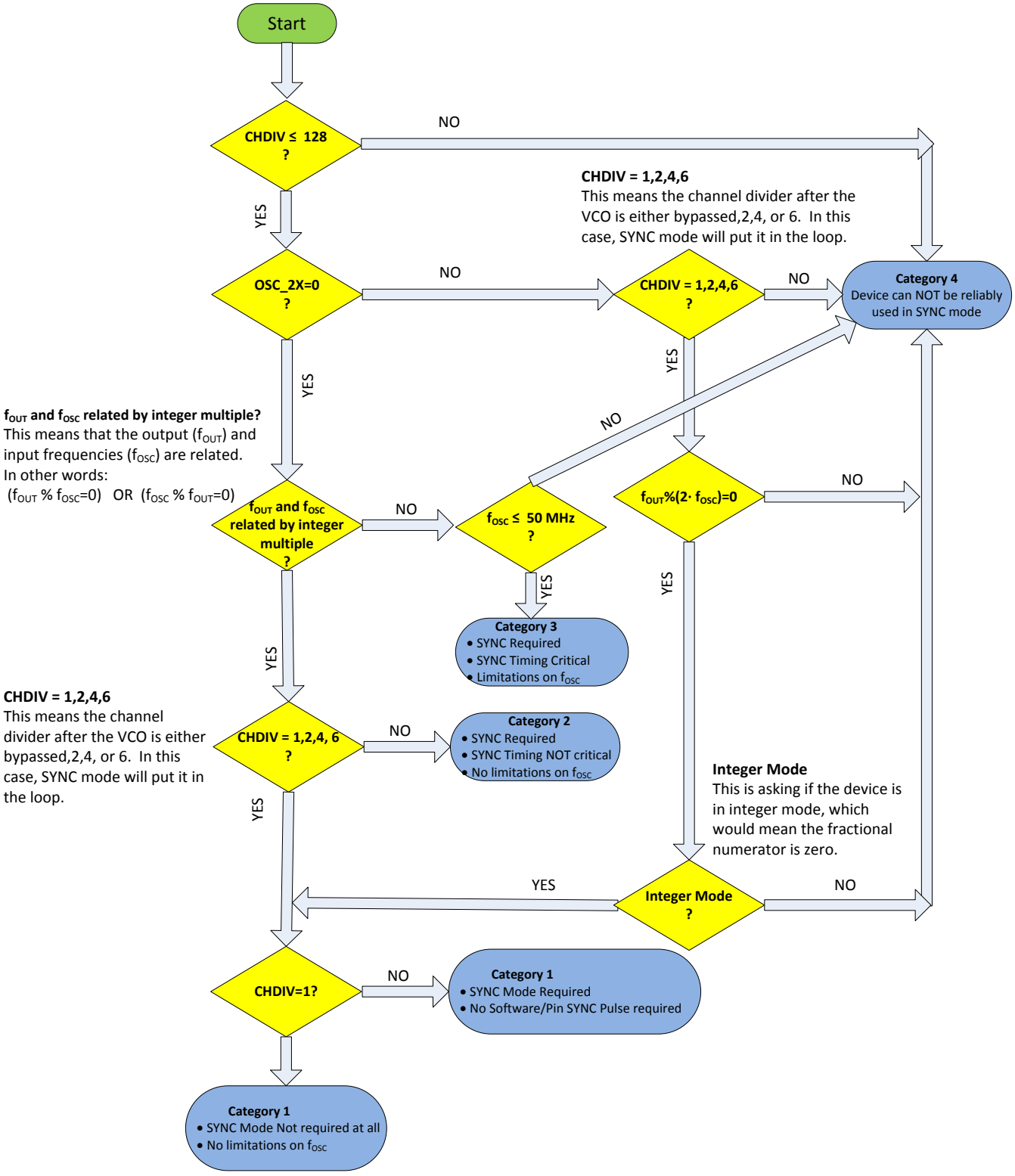


图 26. Determining the SYNC Category

7.3.12.3 Procedure for Using SYNC

This procedure must be used to put the device in SYNC mode.

1. Use the flowchart to determine the SYNC category.
2. Make determinations for OSCin and using SYNC based on the category
    1. If Category 4, SYNC cannot be performed in this setup.
    2. If category 3, ensure that the maximum f_{OSC} frequency for SYNC is not violated and there are hardware accommodations to use the SYNC pin.
3. If the channel divide is used, determine the included channel divide value which will be 2 × SEG1 of the channel divide:
    1. If OUTA_MUX is not channel divider and OUTB_MUX is not channel divider or SysRef, then IncludedDivide = 1.
    2. Otherwise, IncludedDivide = 2 × SEG1. In the case that the channel divider is 2, then IncludedDivide=4.
4. If not done already, divide the N divider and fractional values by the included channel divide to account for the included channel divide.
5. Program the device with the VCO_PHASE_SYNC = 1. Note that this does not count as applying a SYNC to device (for category 2).
6. Apply the SYNC, if required
    1. If category 2, VCO_PHASE_SYNC can be toggled from 0 to 1. Alternatively, a rising edge can be sent to the SYNC pin and the timing of this is not critical.
    2. If category 3, the SYNC pin must be used, and the timing must be away from the rising edge of the OSCin signal.

7.3.12.4 SYNC Input Pin

The SYNC input pin can be driven either in CMOS. However, if not using SYNC mode (VCO_PHASE_SYNC = 0), then the INPIN_IGNORE bit must be set to one, otherwise it causes issues with lock detect. If the pin is desired for to be used and VCO_PHASE_SYNC=1, then set INPIN_IGNORE = 0.

7.3.13 Phase Adjust

The MASH_SEED word can use the sigma-delta modulator to shift output signal phase with respect to the input reference. If a SYNC pulse is sent (software or pin) or the MASH is reset with MASH_RST_N, then this phase shift is from the initial phase of zero. If the MASH_SEED word is written to, then this phase is added. The phase shift is calculated as below.

$$\text{Phase shift in degrees} = 360 \times (\text{MASH\_SEED} / \text{PLL\_DEN}) \times (\text{IncludedDivide}/\text{CHDIV}) \quad (5)$$

Example:

Mash seed = 1

Denominator = 12

Channel divider = 16

Phase shift (VCO_PHASE_SYNC=0) = 360 × (1/12) × (1/16) = 1.875 degrees

Phase Shift (VCO_PHASE_SYNC=1) = 360 × (1/12) × (4/16) = 7.5 degrees

There are several considerations when using MASH_SEED

- Phase shift can be done with a FRAC_NUM=0, but FRAC_ORDER must be greater than zero. For FRAC_ORDER=1, the phase shifting only occurs when MASH_SEED is a multiple of PLL_DEN.
- For the 2nd order modulator, PLL_N≥45, for the 3rd order modulator, PLL_N≥49, and for the fourth order modulator, PLL_N≥54.

When using MASH_SEED in the case where IncludedDivide>1, there are several additional considerations in order to get the phase shift to be monotonically increasing with MASH_SEED.

- It is recommended to use MASH_ORDER <=2.
- When using the 2nd order modulator for VCO frequencies below 10 GHz (when IncludedDivide=6) or 9 GHz (when IncludedDivide=4), it may be necessary to increase the PLL_N value much higher or change to first

order modulator. When this is necessary depends on the VCO frequency, IncludedDivide, and PLL_N value.

7.3.14 Fine Adjustments for Phase Adjust and Phase SYNC

Phase SYNC refers to the process of getting the same phase relationship for every power up cycle and each time assuming that a given programming procedure is followed. However, there are some adjustments that can be made to get the most accurate results. As for the consistency of the phase SYNC, the only source of variation could be if the VCO calibration chooses a different VCO core and capacitor, which can introduce a bimodal distribution with about 10 ps of variation. If this 10 ps is not desirable, then it can be eliminated by reading back the VCO core, capcode, and DACISET values and forcing these values to ensure the same calibration settings every time. The delay through the device varies from part to part and can be on the order of 60 ps. This part to part variation can be calibrated out with the MASH_SEED. The variation in delay through the device also changes on the order of +2.5 ps/°C, but devices on the same board likely have similar temperatures, so this will somewhat track. In summary, the device can be made to have consistent delay through the part and there are means to adjust out any remaining errors with the MASH_SEED. This tends only to be an issue at higher output frequencies when the period is shorter.

7.3.15 SYSREF

The LMX2615 can generate a SYSREF output signal that is synchronized to f_{OUT} with a programmable delay. This output can be a single pulse, series of pulses, or a continuous stream of pulses. To use the SYSREF capability, the PLL must first be placed in SYNC mode with VCO_PHASE_SYNC = 1.

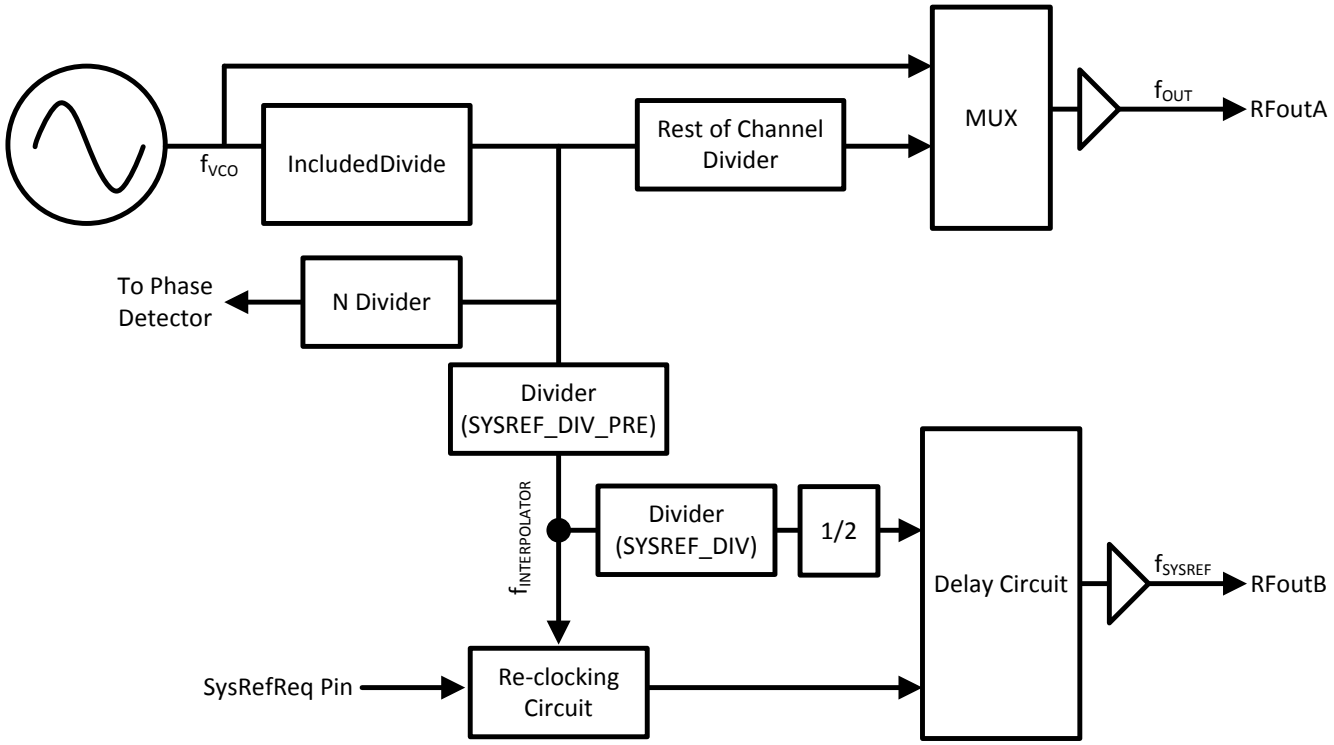


图 27. SYSREF Setup

As 图 27 shows, the SYSREF feature uses IncludedDivide and SYSREF_DIV_PRE divider to generate $f_{INTERPOLATOR}$. This frequency is used for re-clocking of the rising and falling edges at the SysRefReq pin. In master mode, the $f_{INTERPOLATOR}$ is further divided by 2×SYSREF_DIV to generate finite series or continuous stream of pulses.

表 14. SYSREF Setup

PARAMETER	MIN	TYP	MAX	UNIT
f_{VCO}	7600		15200	MHz
$f_{INTERPOLATOR}$	0.8		1.5	GHz
IncludedDivide		4 or 6		
SYSREF_DIV_PRE	1, 2, or 4			
SYSREF_DIV	4,6,8, ..., 4098			
$f_{INTERPOLATOR}$	$f_{PRESYSREF} = f_{VCO}$ /(IncludedDivide × SYSREF_DIV_PRE)			
f_{SYSREF}	$f_{SYSREF} = f_{INTERPOLATOR}$ / (2 × SYSREF_DIV)			
Delay step size		9		ps
Pulses for pulsed mode (SYSREF_PULSE_CNT)	0		15	n/a

The delay can be programmed using the JESD_DAC1_CTRL, JESD_DAC2_CTRL, JESD_DAC3_CTRL, and JESD_DAC4_CTRL words. By concatenating these words into a larger word called "SYSREFPHASESHIFT", the relative delay can be found. The sum of these words must always be 63.

表 15. SysRef Delay

SYSREFPHASESHIFT	DELAY	JESD_DAC1	JESD_DAC2	JESD_DAC3	JESD_DAC4
0	Minimum	36	27	0	0
...				0	0
36		0	63	0	0
37		62	1	0	0
...					
99		0	0	63	0
100		0	0	62	1
...					
161		0	0	1	62
162		0	0	0	63
163		1	0	0	62
225		63	0	0	0
226		62	1	0	0
247	Maximum	41	22	0	0
> 247	Invalid	Invalid	Invalid	Invalid	Invalid

7.3.15.1 Programmable Fields

表 16 has the programmable fields for the SYSREF functionality.

表 16. SYSREF Programming Fields

FIELD	PROGRAMMING	DEFAULT	DESCRIPTION
SYSREF_EN	0 = Disabled 1 = enabled	0	Enables the SYSREF mode. SYSREF_EN must be 1 if and only if OUTB_MUX=2 (SysRef)
SYSREF_DIV_PRE	1: DIV1 2: DIV2 4: DIV4 Other states: invalid		The output of this divider is the $f_{INTERPOLATOR}$.
SYSREF_REPEAT	0 = Master mode 1 = Repeater mode	0	In master mode, the device creates a series of SYSREF pulses. In repeater mode, SYSREF pulses are generated with the SysRefReq pin.
SYSREF_PULSE	0 = Continuous mode 1 = Pulsed mode	0	Continuous mode continuously makes SYSREF pulses, where pulsed mode makes a series of SYSREF_PULSE_CNT pulses
SYSREF_PULSE_CNT	0 to 15	4	In the case of using pulsed mode, this is the number of pulses. Setting this to zero is an allowable, but not practical state.
SYSREF_DIV	0: Divide by 4 1: Divide by 6 2: Divide by 8 ... 2047: Divide by 4098	0	The SYSREF frequency is at the VCO frequency divided by this value.

7.3.15.2 Input and Output Pin Formats

7.3.15.2.1 SYSREF Output Format

The SYSREF output comes in differential format through RFoutB. This will have a minimum voltage of about 2.3 V and a maximum of 3.3 V. If DC coupling cannot be used, there are two strategies for AC coupling.

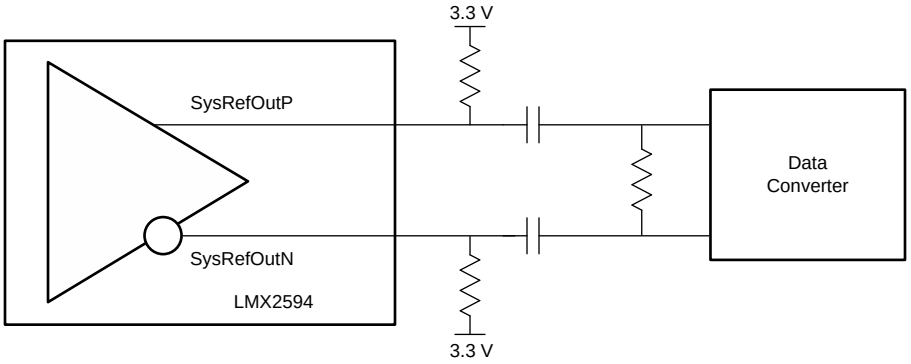


图 28. SYSREF Output

1. Send a series of pulses to establish a DC-bias level across the AC-coupling capacitor.
2. Establish a bias voltage at the data converter that is below the threshold voltage by using a resistive divider.

7.3.15.3 Examples

The SysRef can be used in a repeater mode, which just echos the input, after being re-clocked to the $f_{INTERPOLATOR}$ frequency and then RFout, or it can be used in a repeater. In repeater mode, it can repeat 1,2,4,8, or infinite (continuous) pulses. The frequency for repeater mode is equal to the RFout frequency divided by the SYSREF divider.

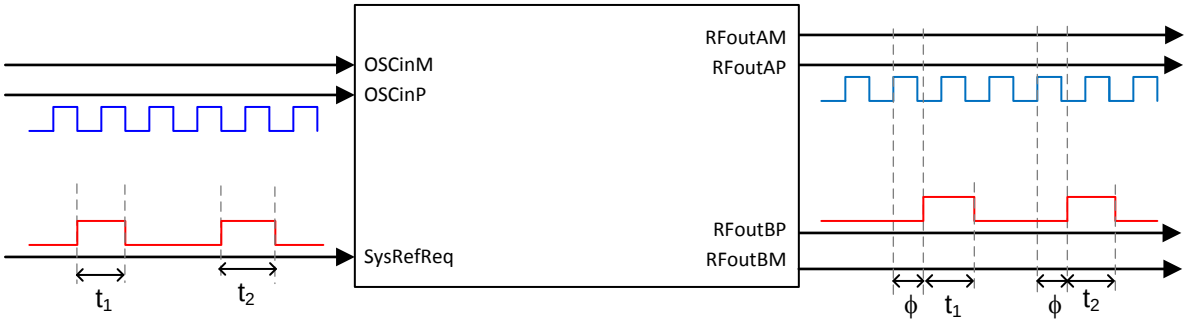


图 29. SYSREF Out In Repeater Mode

In master mode, the SysRefReq pin is pulled high to allow the SysRef output.

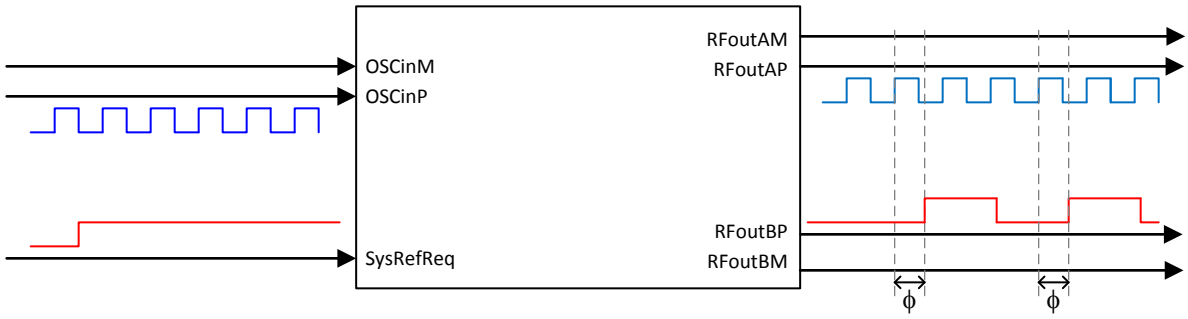


图 30. Figure 1. SYSREF Out In Pulsed/Continuous Mode

7.3.15.4 SYSREF Procedure

To use SYSREF, do the these steps:

1. Put the device in SYNC mode using the procedure already outlined.
2. Figure out IncludedDivide the same way it is done for SYNC mode.
3. Calculate the SYSREF_DIV_PRE value such that the interpolator frequency ($f_{INTERPOLATOR}$) is in the range of 800 to 1500 MHz. $f_{INTERPOLATOR} = f_{VCO}$/IncludedDivide/SYSREF_DIV_PRE. Make this frequency a multiple of f_{OSC} if possible.
4. If using master mode (SYSREF_REPEAT = 0), ensure SysRefReq pin is high, ensure the SysRefReq pin is high.
5. If using repeater mode (SYSREF_REPEAT = 1), set up the pulse count if desired. Pulses are created by toggling the SysRefReq pin.
6. Adjust the delay between the RFoutA and RFoutB signal using the JESD_DACx_CTL fields.

7.3.16 Pin Modes

The LMX2615-SP has 8 pins that can be used to program pre-selected modes. A few rules of operation for these pin modes are as folows:

- Set the pin mode as desired. Pin Mode 0 is SPI mode
- If a single frequency is desired, tie CAL should be tied to supply through 1 kohm resistance and and RECAL_EN shoudl be left open.
- The rise time for the supply needs to be <50 ms.
- Fractional denominator for all pin modes is 4250000
- Some words can be overwritten in pin mode including OUTx_PWR, OUTx_EN, RESET, and POWERDOWN
  When changing between pin modes, after the pins are changed, the CAL pin needs to be toggled
- If the FS7 pin is low, then only the RFoutA output is active. If the FS7 pin is high, then both the RFoutA and RFoutB outputs are active.

The following table shows all the pin modes

表 17. Pin Modes

Mode	f_{OSC} (MHz)	f_{PD} (MHz)	CPG (mA)	f_{OUT} (MHz)	CHDIV	f_{VCO} (MHz)	N	Fraction
0	SPI Mode							
1	10	20	15	160	48	7680	384	0/4250000000
2	10	10	15	395	24	9480	948	0/4250000000
3	10	20	15	720	12	8640	432	0/4250000000
4	10	20	15	1280	6	7680	384	0/4250000000
5	100	200	15	300	32	9600	48	0/4250000000
6	100	200	15	1000	8	8000	40	0/4250000000
7	100	200	15	1200	8	9600	48	0/4250000000
8	20	40	15	6199.855	2	12399.71	309	4219187500/4250000000
9	100	200	15	2000	4	8000	40	0/4250000000
10	50	100	15	250	32	8000	80	0/4250000000
11	50	100	15	500	16	8000	80	0/4250000000
12	50	100	15	850	12	10200	102	0/4250000000
13	20	40	15	5654.912	2	11309.824	282	3168800000/4250000000
14	10	20	15	1517.867839	6	9107.207034	455	1531494725/4250000000
15	10	20	15	1708.670653	6	10252.02392	512	2555082575/4250000000
16	50	100	15	2500	4	10000	100	0/4250000000
17	Reserved. Do not use this pin mode.							
18	10	20	15	3035.735678	4	12142.94271	607	625326300/4250000000
19	50	100	15	3200	4	12800	128	0/4250000000

表 17. Pin Modes (接下页)

Mode	f_{OSC} (MHz)	f_{PD} (MHz)	CPG (mA)	f_{OUT} (MHz)	CHDIV	f_{VCO} (MHz)	N	Fraction
20	10	20	15	3417.341306	4	13669.36522	683	1990110100/4250000000
21	50	100	15	4500	2	9000	90	0/4250000000
22	50	100	15	4800	2	9600	96	0/4250000000
23	50	100	15	5350	2	10700	107	0/4250000000
24	50	100	15	6800	2	13600	136	0/4250000000
25	10	20	15	6834	2	13668	683	1700000000/4250000000
26	10	20	15	6834.682611	2	13669.36522	683	1990109675/4250000000
27	10	20	15	6834.6875	2	13669.375	683	1992187500/4250000000
28	10	20	15	6834.75	2	13669.5	683	2018750000/4250000000
29	50	100	15	9600	1	9600	96	0/4250000000
30	50	100	15	9650	1	9650	96	2125000000/4250000000
31	50	100	15	13500	1	13500	135	0/4250000000
32	100	100	15	70	128	8960	89	2550000000/4250000000
33	18.75	37.5	15	393.75	24	9450	252	0/4250000000
34	18.75	37.5	15	422.4990441	24	10139.97706	270	1697399952/4250000000
35	37.5	75	15	422.4990441	24	10139.97706	135	848699976/4250000000
36	20	40	15	6785.552	2	13571.104	339	1179800000/4250000000
37	20	40	15	2088.38	4	8353.52	208	3561500000/4250000000
38	100	100	15	2210	4	8840	88	1700000000/4250000000
39	100	100	15	2238	4	8952	89	2210000000/4250000000
40	20	40	15	2254.35	4	9017.4	225	1848750000/4250000000
41	20	40	15	2270	4	9080	227	0/4250000000
42	20	40	15	2280	4	9120	228	0/4250000000
43	18.75	37.5	15	6759.984705	2	13519.96941	360	2263199800/4250000000
44	37.5	75	15	6759.984705	2	13519.96941	180	1131599900/4250000000
45	20	40	15	8125	1	8125	203	531250000/4250000000
46	20	40	15	8175	1	8175	204	1593750000/4250000000
47	20	40	15	8200	1	8200	205	0/4250000000
48	20	40	15	8210	1	8210	205	1062500000/4250000000
49	20	40	15	8212.5	1	8212.5	205	1328125000/4250000000
50	20	40	15	8275	1	8275	206	3718750000/4250000000
51	20	40	15	8300	1	8300	207	2125000000/4250000000
52	20	40	15	8400	1	8400	210	0/4250000000
53	20	40	15	8450	1	8450	211	1062500000/4250000000
54	20	40	15	8460	1	8460	211	2125000000/4250000000
55	20	40	15	8484	1	8484	212	425000000/4250000000
56	20	40	15	8496	1	8496	212	1700000000/4250000000
57	20	40	15	8212	1	8212	205	1275000000/4250000000
58	10	20	15	12860	1	12860	643	0/4250000000
59	10	20	15	13000	1	13000	650	0/4250000000
60	10	20	15	13022.5	1	13022.5	651	531250000/4250000000
61	10	20	15	13125	1	13125	656	1062500000/4250000000
62	10	20	15	13222.5	1	13222.5	661	531250000/4250000000
63	20	40	15	12209.697	1	12209.697	305	1030306250/4250000000
64	10	20	15	13390	1	13390	669	2125000000/4250000000
65	10	20	15	13417.5	1	13417.5	670	3718750000/4250000000
66	20	40	15	12689.697	1	12689.697	317	1030412500/4250000000

表 17. Pin Modes (接下页)

Mode	f_{OSC} (MHz)	f_{PD} (MHz)	CPG (mA)	f_{OUT} (MHz)	CHDIV	f_{VCO} (MHz)	N	Fraction
67	20	40	15	13906.667	1	13906.667	347	2833368750/4250000000
68	20	40	15	14192.727	1	14192.727	354	3477243750/4250000000
69	10	20	15	8212.5	1	8212.5	410	2656250000/4250000000
70	100	50	15	1250	8	10000	200	0/4250000000
71	50	100	15	1250	8	10000	100	0/4250000000
72	18.75	37.5	15	1875	6	11250	300	0/4250000000

7.4 Device Functional Modes

表 18. Device Functional Modes

MODE	DESCRIPTION	SOFTWARE SETTINGS
RESET	Registers are held in their reset state. This device does have a power on reset, but it is good practice to also do a software reset if there is any possibility of noise on the programming lines, especially if there is sharing with other devices. Also realize that there are registers not disclosed in the data sheet that are reset as well.	RESET = 1 POWERDOWN = 0
POWERDOWN	Device is powered down.	POWERDOWN = 1 or CAL Pin = Low
Pin Mode	Device settings are determined by pin states.	One of FS0, FS1, ... FS7 pins is NOT low
Normal operating mode	This is used with at least one output on as a frequency synthesizer and the device can be controlled through the SPI interface	ALL of FS0, FS1, ... FS7 pins are low
SYNC mode	This is used where part of the channel divider is in the feedback path to ensure deterministic phase.	VCO_PHASE_SYNC = 1
SYSREF mode	In this mode, RFoutB is used to generate pulses for SYSREF.	VCO_PHASE_SYNC =1, SYSREF_EN = 1

7.5 Programming

When not in pin mode, the LMX2615 is programmed using 24-bit shift registers. The shift register consists of a R/W bit (MSB), followed by a 7-bit address field and a 16-bit data field. For the R/W bit, 0 is for write, and 1 is for read. The address field ADDRESS[6:0] is used to decode the internal register address. The remaining 16 bits form the data field DATA[15:0]. While CSB is low, serial data is clocked into the shift register upon the rising edge of clock (data is programmed MSB first). When CSB goes high, data is transferred from the data field into the selected register bank. See 图 1 for timing details.

7.5.1 Recommended Initial Power-Up Sequence

For the most reliable programming, TI recommends this procedure:

1. Apply power to device.
2. Program RESET = 1 to reset registers.
3. Program RESET = 0 to remove reset.
4. Program registers as shown in the register map in REVERSE order from highest to lowest.
   - Programming of register R114 is only needed one wants to change the default states for WD_CNTRL or WD_DLY.
   - Programming of registers R113 down to R76 is not required, but if they are programmed, they should be done so as the register map shows.
   - Programming of registers R75 down to R0 is required. Registers in this range that only 1's and 0's should also be programmed in accordance to the register map. Do NOT assume that the power on reset state and the recommended value are the same. Also, in the register descriptions, it lists a "Reset" value. This is actually the recommended value that should match the main register map table; it is not necessarily the power on reset value.
5. Wait 10 ms
6. Program register R0 one additional time with FCAL_EN = 1 to ensure that the VCO calibration runs from a stable state.

7.5.2 Recommended Sequence for Changing Frequencies

The recommended sequence for changing frequencies is as follows:

1. Change the N divider value.
2. Program the PLL numerator and denominator.
3. Program FCAL_EN (R0[3]) = 1.

7.6 Register Maps

7.6.1 Register Map

表 19. Complete Register Map Table

REG	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	VCO_PHASE_SYNC	1	0	0	0	OUT_MUTE	FCAL_HPFD_ADJ		0	0	1	FCAL_EN	MUXOUT_LD_SEL	RESET	POWERDOWN
R1	0	0	0	0	1	0	0	0	0	0	0	0	1	CAL_CLK_DIV		
R2	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
R3	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0
R4	0	0	0	0	1	1	1	0	0	1	0	0	0	0	1	1
R5	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0
R6	0	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0
R7	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	0
R8	0	VCO_DACISET_FORCE	1	0	VCO_CAPCTRL_FORCE	0	0	0	0	0	0	0	0	0	0	0
R9	0	0	0	OSC_2X	0	1	1	0	0	0	0	0	0	1	0	0
R10	0	0	0	1	0	0	0	0	1	1	0	1	1	0	0	0
R11	0	0	0	0	PLL_R							1	1	0	0	0
R12	0	1	0	1	0	0	0	0	PLL_R_PRE							
R13	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R14	0	0	0	1	1	1	1	0	0	CPG			0	0	0	0
R15	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	1
R16	0	0	0	0	0	0	0	VCO_DACISET								
R17	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0
R18	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
R19	0	0	1	0	0	1	1	1	VCO_CAPCTRL							
R20	1	1	VCO_SEL			VCO_SEL_FORCE	0	0	0	1	0	0	1	0	0	0
R21	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
R22	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R23	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0
R24	0	0	0	0	0	1	1	1	0	0	0	1	1	0	1	0
R25	0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	0
R26	0	0	0	0	1	1	0	1	1	0	1	1	0	0	0	0
R27	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R28	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0
R29	0	0	1	1	0	0	0	1	1	0	0	0	1	1	0	0
R30	0	0	1	1	0	0	0	1	1	0	0	0	1	1	0	0
R31	0	SEG1_EN	0	0	0	0	1	1	1	1	1	0	1	1	0	0
R32	0	0	0	0	0	0	1	1	1	0	0	1	0	0	1	1
R33	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1
R34	0	0	0	0	0	0	0	0	0	0	0	0	0	PLL_N[18:16]		

Register Maps (接下页)

表 19. Complete Register Map Table (接下页)

R35	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R36	PLL_N[15:0]															
R37	1	0	PFD_DLY_SEL						0	0	0	0	0	1	0	0
R38	PLL_DEN[31:16]															
R39	PLL_DEN[15:0]															
R40	MASH_SEED[31:16]															
R41	MASH_SEED[15:0]															
R42	PLL_NUM[31:16]															
R43	PLL_NUM[15:0]															
R44	0	0	OUTA_PWR						OUTB_PD	OUTA_PD	MASH_RESET_N	0	0	MASH_ORDER		
R45	1	1	0	OUTA_MUX		0	0	0	1	1	OUTB_PWR					
R46	0	0	0	0	0	1	1	1	1	1	1	1	1	1	OUTB_MUX	
R47	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
R48	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
R49	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0
R50	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R51	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R52	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0
R53	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R54	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R55	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R56	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R57	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R58	INPIN_IGNORE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R59	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LD_TYPE
R60	LD_DLY															
R61	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
R62	0	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0
R63	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R64	0	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0
R65	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R66	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0
R67	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R68	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0
R69	MASH_RST_COUNT[31:16]															
R70	MASH_RST_COUNT[15:0]															
R71	0	0	0	0	0	0	0	0	SYSREF_DIV_PRE			SYSREF_PULSE	SYSREF_EN	SYSREF_REPEAT	0	0
R72	0	0	0	0	0	SYSREF_DIV										
R73	0	0	0	0	JESD_DAC2_CTRL						JESD_DAC1_CTRL					
R74	SYSREF_PULSE_CNT				JESD_DAC4_CTRL						JESD_DAC3_CTRL					
R75	0	0	0	0	1	CHDIV					0	0	0	0	0	0

Register Maps (接下页)

表 19. Complete Register Map Table (接下页)

R76	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
R77	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R78	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
R79	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R80	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R81	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R82	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R83	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R84	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R85	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R86	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R87	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R88	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R89	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R90	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R91	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R92	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R93	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R94	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R95	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R96	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R97	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R98	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R99	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R100	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R101	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R102	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R103	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R104	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R105	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0
R106	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
R107	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R108	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1
R109	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R110	0	0	0	0	0	rb_LD_VTUNE		0	rb_VCO_SEL			0	0	0	0	0
R111	0	0	0	0	0	0	0	0	rb_VCO_CAPCTRL							
R112	0	0	0	0	0	0	0	rb_VCO_DACISET								
R113	rb_IO_STATUS															
R114	0	0	0	0	0	0	WD_DLY							WD_CNTRL		

Table 20 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 20 should be considered as reserved locations and the register contents should not be modified.

Table 20. Device Registers

Address	Acronym	Register Name	Section
0x0	R0		Go
0x1	R1		Go

Table 20. Device Registers (continued)

Address	Acronym	Register Name	Section
0x8	R8		Go
0x9	R9		Go
0xB	R11		Go
0xC	R12		Go
0xE	R14		Go
0x10	R16		Go
0x13	R19		Go
0x14	R20		Go
0x1F	R31		Go
0x22	R34		Go
0x24	R36		Go
0x25	R37		Go
0x26	R38		Go
0x27	R39		Go
0x28	R40		Go
0x29	R41		Go
0x2A	R42		Go
0x2B	R43		Go
0x2C	R44		Go
0x2D	R45		Go
0x2E	R46		Go
0x3A	R58		Go
0x3B	R59		Go
0x3C	R60		Go
0x45	R69		Go
0x46	R70		Go
0x47	R71		Go
0x48	R72		Go
0x49	R73		Go
0x4A	R74		Go
0x4B	R75		Go
0x6E	R110		Go
0x6F	R111		Go
0x70	R112		Go
0x71	R113		Go
0x72	R114		Go

Complex bit access types are encoded to fit into small table cells. Table 21 shows the codes that are used for access types in this section.

Table 21. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		

Table 21. Device Access Type Codes (continued)

Access Type	Code	Description
-n		Value after reset or the default value

7.6.1.1 R0 Register (Address = 0x0) [reset = X]

R0 is shown in Figure 31 and described in Table 22.

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Figure 31. R0 Register

7	6	5	4	3	2	1	0
FCAL_HPFD_ADJ	RESERVED			FCAL_EN	MUXOUT_LD_SEL	RESET	POWERDOWN
R/W-0x0	R-0x0			R/W-0x1	R/W-0x1	R/W-0x0	R/W-0x0

Table 22. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
14	VCO_PHASE_SYNC	R/W	X	Phase Sync Mode Enable. In this state, part of the channel divider is put in the feedback path to ensure determinisic phase. The action of toggling this bit from 0 to 1 also sends an asynchronous SYNC pulse. 0x0 = Phase SYNC disabled 0x1 = Phase SYNC enabled
13-10	RESERVED	R	X	
9	OUT_MUTE	R/W	X	0x1 = Mute output (RFOUTA/B) during FCAL
8-7	FCAL_HPFD_ADJ	R/W	0x0	Adjustment to decrease the state machine clock for the VCO calibration speed based on phase detector frequency.
6-4	RESERVED	R	0x0	
3	FCAL_EN	R/W	0x1	Writing register R0 with this bit set to a '1' enables and triggers the VCO frequency calibration.
2	MUXOUT_LD_SEL	R/W	0x1	Selects the functionality of the MUXout Pin 0x0 = Readback 0x1 = Lock Detect
1	RESET	R/W	0x0	Register Reset. This resets all registers and state machines. After writing a '1', you must write a '0' to remove the reset.It is recommended to toggle the RESET bit before programming the part to ensure consistent performance. 0x0 = Normal Operation 0x1 = Reset
0	POWERDOWN	R/W	0x0	Powers down device. 0x0 = Normal Operation 0x1 = Powered Down

7.6.1.2 R1 Register (Address = 0x1) [reset = 0x4]

R1 is shown in Figure 32 and described in Table 23.

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Figure 32. R1 Register

7	6	5	4	3	2	1	0
RESERVED					CAL_CLK_DIV		
R-0x0					R/W-0x4		

Table 23. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	
2-0	CAL_CLK_DIV	R/W	0x4	Divides down the Fosc frequency to the state machine clock (SM_CLK) frequency. SM_CLK = Fosc/($2^{CAL\_CLK\_DIV}$). Ensure that the state machine clock frequency 50 MHz or less. 0x0 = Up to 50 MHz 0x1 = Up to 100 MHz 0x2 = Up to 200 MHz 0x3 = Up to 400 MHz 0x4 = Up to 800 MHz 0x5 = Greater than 800 MHz

7.6.1.3 R8 Register (Address = 0x8) [reset = X]

R8 is shown in Figure 33 and described in Table 24.

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Figure 33. R8 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0x0							

Table 24. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
14	VCO_DACISET_FORCE	R/W	X	Forces VCO_DACISET Value. Useful for fully assisted VCO calibration and debugging purposes.
13-12	RESERVED	R	X	
11	VCO_CAPCTRL_FORCE	R/W	X	Forces VCO_CAPCTRL value. Useful for fully assisted VCO calibration and debugging purposes.
10-0	RESERVED	R	0x0	

7.6.1.4 R9 Register (Address = 0x9) [reset = X]

R9 is shown in Figure 34 and described in Table 25.

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Figure 34. R9 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0x0							

Table 25. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
12	OSC_2X	R/W	X	Reference Path Doubler 0x0 = Disabled 0x1 = Enable
11-0	RESERVED	R	0x0	

7.6.1.5 R11 Register (Address = 0xB) [reset = 0x10]

R11 is shown in Figure 35 and described in Table 26.

Return to Summary Table.

Figure 35. R11 Register

7	6	5	4	3	2	1	0
PLL_R				RESERVED			
R/W-0x1				R-0x0			

Table 26. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
11-4	PLL_R	R/W	0x1	PLL R divider Value
3-0	RESERVED	R	0x0	

7.6.1.6 R12 Register (Address = 0xC) [reset = 0x1]

R12 is shown in Figure 36 and described in Table 27.

Return to Summary Table.

Figure 36. R12 Register

7	6	5	4	3	2	1	0
PLL_R_PRE							
R/W-0x1							

Table 27. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL_R_PRE	R/W	0x1	PLL Pre-R divider value

7.6.1.7 R14 Register (Address = 0xE) [reset = 0x70]

R14 is shown in Figure 37 and described in Table 28.

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Figure 37. R14 Register

7	6	5	4	3	2	1	0
RESERVED	CPG			RESERVED			
R-0x0	R/W-0x7			R-0x0			

Table 28. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	
6-4	CPG	R/W	0x7	Effective charge pump gain . This is the sum of the up and down currents.
3-0	RESERVED	R	0x0	

7.6.1.8 R16 Register (Address = 0x10) [reset = 0x80]

R16 is shown in Figure 38 and described in Table 29.

Return to Summary Table.

Figure 38. R16 Register

7	6	5	4	3	2	1	0
VCO_DACISET							
R/W-0x80							

Table 29. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
8-0	VCO_DACISET	R/W	0x80	Programmable current setting for the VCO that is applied when VCO_DACISET_FORCE=1.

7.6.1.9 R19 Register (Address = 0x13) [reset = 0xB7]

R19 is shown in Figure 39 and described in Table 30.

Return to Summary Table.

Figure 39. R19 Register

7	6	5	4	3	2	1	0
VCO_CAPCTRL							
R/W-0xB7							

Table 30. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VCO_CAPCTRL	R/W	0xB7	Programmable band within VCO core that applies when VCO_CAPCTRL_FORCE=1. Valid values are 183 to 0, where the higher number is a lower frequency.

7.6.1.10 R20 Register (Address = 0x14) [reset = X]

R20 is shown in Figure 40 and described in Table 31.

Return to Summary Table.

Figure 40. R20 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0x0							

Table 31. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
13-11	VCO_SEL	R/W	X	User specified start VCO for calibration. Also is the VCO core that is forced by VCO_SEL_FORCE
10	VCO_SEL_FORCE	R/W	X	Force the VCO_SEL Value
9-0	RESERVED	R	0x0	

7.6.1.11 R31 Register (Address = 0x1F) [reset = X]

R31 is shown in Figure 41 and described in Table 32.

Return to Summary Table.

Figure 41. R31 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0x0							

Table 32. R31 Register Field Descriptions

Bit	Field	Type	Reset	Description
14	SEG1_EN	R/W	X	Enables first divide by 2 in channel divider.
13-0	RESERVED	R	0x0	

7.6.1.12 R34 Register (Address = 0x22) [reset = 0x0]

R34 is shown in Figure 42 and described in Table 33.

Return to Summary Table.

Figure 42. R34 Register

7	6	5	4	3	2	1	0
RESERVED					PLL_N_18:16		
R-0x0					R/W-0x0		

Table 33. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	
2-0	PLL_N_18:16	R/W	0x0	Upper 3 bits of N mash, total 19 bits, split as 16 + 3

7.6.1.13 R36 Register (Address = 0x24) [reset = 0x46]

R36 is shown in Figure 43 and described in Table 34.

Return to Summary Table.

Figure 43. R36 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_N															
R/W-0x46															

Table 34. R36 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_N	R/W	0x46	PLL N divider value

7.6.1.14 R37 Register (Address = 0x25) [reset = 0x400]

R37 is shown in Figure 44 and described in Table 35.

Return to Summary Table.

Figure 44. R37 Register

15	14	13	12	11	10	9	8
RESERVED		PFD_DLY_SEL					
R-0x0		R/W-0x4					
7	6	5	4	3	2	1	0
RESERVED							
R-0x0							

Table 35. R37 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	
13-8	PFD_DLY_SEL	R/W	0x4	Programmable phase detector delay. This should be programmed based on VCO frequency, fractional order, and N divider value. DLY = (PFD_DLY_SEL + 3)*4*VCO_cycle.
7-0	RESERVED	R	0x0	

7.6.1.15 R38 Register (Address = 0x26) [reset = 0xFD51]

R38 is shown in Figure 45 and described in Table 36.

Return to Summary Table.

Figure 45. R38 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_DEN_31:16															
R/W-0xFD51															

Table 36. R38 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_DEN_31:16	R/W	0xFD51	Fractional Denominator(MSB)

7.6.1.16 R39 Register (Address = 0x27) [reset = 0xDA80]

R39 is shown in Figure 46 and described in Table 37.

Return to Summary Table.

Figure 46. R39 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_DEN															
R/W-0xDA80															

Table 37. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_DEN	R/W	0xDA80	Fractional Denominator

7.6.1.17 R40 Register (Address = 0x28) [reset = 0x0]

R40 is shown in Figure 47 and described in Table 38.

Return to Summary Table.

Figure 47. R40 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASH_SEED_31:16															
R/W-0x0															

Table 38. R40 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_SEED_31:16	R/W	0x0	MASH_SEED(MSB)

7.6.1.18 R41 Register (Address = 0x29) [reset = 0x0]

R41 is shown in Figure 48 and described in Table 39.

Return to Summary Table.

Figure 48. R41 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASH_SEED															
R/W-0x0															

Table 39. R41 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_SEED	R/W	0x0	Sets the initial state of the fractional engine. Useful for producing a phase shift and fractional spur optimization.

7.6.1.19 R42 Register (Address = 0x2A) [reset = 0x0]

R42 is shown in Figure 49 and described in Table 40.

Return to Summary Table.

Figure 49. R42 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_NUM_31:16															
R/W-0x0															

Table 40. R42 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_NUM_31:16	R/W	0x0	Fractional Numerator (MSB)

7.6.1.20 R43 Register (Address = 0x2B) [reset = 0x0]

R43 is shown in Figure 50 and described in Table 41.

Return to Summary Table.

Figure 50. R43 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_NUM															
R/W-0x0															

Table 41. R43 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_NUM	R/W	0x0	Fractional Numerator

7.6.1.21 R44 Register (Address = 0x2C) [reset = 0x1FA3]

R44 is shown in Figure 51 and described in Table 42.

Return to Summary Table.

Figure 51. R44 Register

15	14	13	12	11	10	9	8
RESERVED		OUTA_PWR					
R-0x0		R/W-0x1F					
7	6	5	4	3	2	1	0

OUTB_PD	OUTA_PD	MASH_RESET_N	RESERVED	MASH_ORDER
R/W-0x1	R/W-0x0	R/W-0x1	R-0x0	R/W-0x3

Table 42. R44 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	
13-8	OUTA_PWR	R/W	0x1F	Sets current that controls output power for output A. 0 is minimum current, 63 is maximum current.
7	OUTB_PD	R/W	0x1	\nPowers down output B
6	OUTA_PD	R/W	0x0	Powers down output A
5	MASH_RESET_N	R/W	0x1	Active low reset for MASH
4-3	RESERVED	R	0x0	
2-0	MASH_ORDER	R/W	0x3	MASH Order

7.6.1.22 R45 Register (Address = 0x2D) [reset = X]

R45 is shown in Figure 52 and described in Table 43.

Return to Summary Table.

Figure 52. R45 Register

7	6	5	4	3	2	1	0
RESERVED		OUTB_PWR					
R-0x0		R/W-0x1F					

Table 43. R45 Register Field Descriptions

Bit	Field	Type	Reset	Description
12-11	OUTA_MUX	R/W	X	\nSelects input to OUTA output
10-6	RESERVED	R	0x0	
5-0	OUTB_PWR	R/W	0x1F	Sets current that controls output power for output B. 0 is minimum current, 63 is maximum current.

7.6.1.23 R46 Register (Address = 0x2E) [reset = 0x1]

R46 is shown in Figure 53 and described in Table 44.

Return to Summary Table.

Figure 53. R46 Register

7	6	5	4	3	2	1	0
RESERVED						OUTB_MUX	
R-0x0						R/W-0x1	

Table 44. R46 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	
1-0	OUTB_MUX	R/W	0x1	\nSelects input to the OUTB output

7.6.1.24 R58 Register (Address = 0x3A) [reset = X]

R58 is shown in Figure 54 and described in Table 45.

Return to Summary Table.

Figure 54. R58 Register

7	6	5	4	3	2	1	0
RESERVED							
R-0x0							

Table 45. R58 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	INPIN_IGNORE	R/W	X	Ignore SYNC and SYSREF pins when VCO_PHASE_SYNC=0. This bit should be set to 1 unless VCO_PHASE_SYNC=1
14-0	RESERVED	R	0x0	

7.6.1.25 R59 Register (Address = 0x3B) [reset = 0x1]

R59 is shown in Figure 55 and described in Table 46.

Return to Summary Table.

Figure 55. R59 Register

7	6	5	4	3	2	1	0
RESERVED							LD_TYPE
R-0x0							R/W-0x1

Table 46. R59 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	
0	LD_TYPE	R/W	0x1	Lock Detect Type. VCOCal lock detect asserts a high output after the VCO has finished calibration and the LD_DLY timout counter is finished. Vtune and VCOCal lock detect asserts a high output when VCOCal lock detect would assert a signal and the tuning voltage to the VCO is within acceptable limits. 0x0 = VCOCal Lock Detect 0x1 = VCOCal and Vtune Lock Detect

7.6.1.26 R60 Register (Address = 0x3C) [reset = 0x9C4]

R60 is shown in Figure 56 and described in Table 47.

Return to Summary Table.

Figure 56. R60 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LD_DLY															
R/W-0x9C4															

Table 47. R60 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	LD_DLY	R/W	0x9C4	For the VCOCal lock detect, this is the delay in phase detector cycles that is added after the calibration is finished before the VCOCal lock detect is asserted high.

7.6.1.27 R69 Register (Address = 0x45) [reset = 0x0]

R69 is shown in Figure 57 and described in Table 48.

Return to Summary Table.

Figure 57. R69 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASH_RST_COUNT_31:16															
R/W-0x0															

Table 48. R69 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_RST_COUNT_31:16	R/W	0x0	Upper 16 bits of MASH_RST_CNT.

7.6.1.28 R70 Register (Address = 0x46) [reset = 0xC350]

R70 is shown in Figure 58 and described in Table 49.

Return to Summary Table.

Figure 58. R70 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASH_RST_COUNT															
R/W-0xC350															

Table 49. R70 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASH_RST_COUNT	R/W	0xC350	MASH reset count is used to add a delay when using phase SYNC. The delay should be set at least four times the PLL lock time. This delay is expressed in state machine clock periods.\nOne of these periods is equal to $2^{CAL\_CLK\_DIV}$/Fosc

7.6.1.29 R71 Register (Address = 0x47) [reset = 0x80]

R71 is shown in Figure 59 and described in Table 50.

Return to Summary Table.

Figure 59. R71 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	6	5	4	3	2	1	0
SYSREF_DIV_PRE			SYSREF_PULSE	SYSREF_EN	SYSREF_REPEAT	RESERVED	
R/W-0x4			R/W-0x0	R/W-0x0	R/W-0x0	R-0x0	

Table 50. R71 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0x0	
7-5	SYSREF_DIV_PRE	R/W	0x4	This divider is used to get the frequency input to the SYSREF interpolater within accetable limits
4	SYSREF_PULSE	R/W	0x0	When in master mode (SYSREF_REPEAT=0), this allows multiple pulses (as determined by SYSREF_PULSE_CNT) to be sent out whenever the SysRefReq pin goes high.
3	SYSREF_EN	R/W	0x0	Enable SYREF mode. 0x0 = Disabled 0x1 = Enabled

Table 50. R71 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	SYSREF_REPEAT	R/W	0x0	Defines the SYSREF mode. 0x0 = Master mode. In this mode, SYSREF pulses are generated continuously at the output. 0x1 = Repeater Mode. In this mode, SYSREF pulses are generated in respolse to the SysRefReq pin.
1-0	RESERVED	R	0x0	

7.6.1.30 R72 Register (Address = 0x48) [reset = 0x1]

R72 is shown in Figure 60 and described in Table 51.

Return to Summary Table.

Figure 60. R72 Register

15	14	13	12	11	10	9	8
RESERVED					SYSREF_DIV		
R-0x0					R/W-0x1		
7	6	5	4	3	2	1	0
SYSREF_DIV							
R/W-0x1							

Table 51. R72 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	
10-0	SYSREF_DIV	R/W	0x1	This divider further divides the output frequency for the SYSREF.

7.6.1.31 R73 Register (Address = 0x49) [reset = 0x3F]

R73 is shown in Figure 61 and described in Table 52.

Return to Summary Table.

Figure 61. R73 Register

15	14	13	12	11	10	9	8
RESERVED				JESD_DAC2_CTRL			
R-0x0				R/W-0x0			
7	6	5	4	3	2	1	0
JESD_DAC2_CTRL		JESD_DAC1_CTRL					
R/W-0x0		R/W-0x3F					

Table 52. R73 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	
11-6	JESD_DAC2_CTRL	R/W	0x0	Programmable delay adjustment for SysRef mode
5-0	JESD_DAC1_CTRL	R/W	0x3F	Programmable delay adjustment for SysRef mode

7.6.1.32 R74 Register (Address = 0x4A) [reset = 0x0]

R74 is shown in Figure 62 and described in Table 53.

Return to Summary Table.

Figure 62. R74 Register

15	14	13	12	11	10	9	8
SYSREF_PULSE_CNT				JESD_DAC4_CTRL			
R/W-0x0				R/W-0x0			
7	6	5	4	3	2	1	0
JESD_DAC4_CTRL		JESD_DAC3_CTRL					
R/W-0x0		R/W-0x0					

Table 53. R74 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	SYSREF_PULSE_CNT	R/W	0x0	Used in SYSREF_REPEAT mode to define how many pulses are sent.
11-6	JESD_DAC4_CTRL	R/W	0x0	Programmable delay adjustment for SysRef mode
5-0	JESD_DAC3_CTRL	R/W	0x0	Programmable delay adjustment for SysRef mode

7.6.1.33 R75 Register (Address = 0x4B) [reset = 0x0]

R75 is shown in Figure 63 and described in Table 54.

Return to Summary Table.

Figure 63. R75 Register

15	14	13	12	11	10	9	8
RESERVED					CHDIV		
R-0x0					R/W-0x0		
7	6	5	4	3	2	1	0
CHDIV		RESERVED					
R/W-0x0		R-0x0					

Table 54. R75 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	
10-6	CHDIV	R/W	0x0	Channel divider (Equivalent Division) controls divider value of each segment of the channel divider
5-0	RESERVED	R	0x0	

7.6.1.34 R110 Register (Address = 0x6E) [reset = 0x0]

R110 is shown in Figure 64 and described in Table 55.

Return to Summary Table.

Figure 64. R110 Register

15	14	13	12	11	10	9	8
RESERVED					rb_LD_VTUNE		RESERVED
R-0x0					R-0x0		R-0x0
7	6	5	4	3	2	1	0
rb_VCO_SEL			RESERVED				
R-0x0			R-0x0				

Table 55. R110 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	
10-9	rb_LD_VTUNE	R	0x0	Readback field for the lock detect. 0x0 = Unlocked (Fvco Low) 0x1 = Invalid 0x2 = Locked 0x3 = Unlocked (Fvco High)
8	RESERVED	R	0x0	
7-5	rb_VCO_SEL	R	0x0	Readback
4-0	RESERVED	R	0x0	

7.6.1.35 R111 Register (Address = 0x6F) [reset = 0x0]

R111 is shown in Figure 65 and described in Table 56.

Return to Summary Table.

Figure 65. R111 Register

7	6	5	4	3	2	1	0
rb_VCO_CAPCTRL							
R-0x0							

Table 56. R111 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	rb_VCO_CAPCTRL	R	0x0	Readback field for the actual VCO_CAPCTRL value that is chosen by the VCO calibration.

7.6.1.36 R112 Register (Address = 0x70) [reset = 0x0]

R112 is shown in Figure 66 and described in Table 57.

Return to Summary Table.

Figure 66. R112 Register

7	6	5	4	3	2	1	0
rb_VCO_DACISET							
R-0x0							

Table 57. R112 Register Field Descriptions

Bit	Field	Type	Reset	Description
8-0	rb_VCO_DACISET	R	0x0	Readback field for the actual VCO_DACISET value that is chosen by the VCO calibration.

7.6.1.37 R113 Register (Address = 0x71) [reset = 0x0]

R113 is shown in Figure 67 and described in Table 58.

Return to Summary Table.

Figure 67. R113 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rb_IO_STATUS															
R-0x0															

Table 58. R113 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	rb_IO_STATUS	R	0x0	Reads back status of mode pins. <0> RECAL_EN, <1-8> Pin Modes

7.6.1.38 R114 Register (Address = 0x72) [reset = 0x26F]

R114 is shown in Figure 68 and described in Table 59.

Return to Summary Table.

Figure 68. R114 Register

15	14	13	12	11	10	9	8
RESERVED						WD_DLY	
R-0x0						R/W-0x4D	
7	6	5	4	3	2	1	0
WD_DLY						WD_CNTRL	
R/W-0x4D						R/W-0x7	

Table 59. R114 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	
9-3	WD_DLY	R/W	0x4D	Delay for the internal watchdog timer. It is internally multiplied by 2^{14}. Default value is 25 ms with 50 MHz SM CLK.
2-0	WD_CNTRL	R/W	0x7	Watchdog Control 0x0 = Digital Watchdog disabled. 0x1 = Watchdog triggers 1 time 0x2 = Watchdog triggers up to 2 times 0x3 = Watchdog triggers up to 3 times 0x4 = Watchdog triggers up to 4 times 0x5 = Watchdog triggers up to 5 times 0x6 = Watchdog triggers up to 6 times 0x7 = Watchdog retriggers as many times as necessary with no limit.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 OSCin Configuration

OSCin supports single or differential-ended clock. There must be a AC -coupling capacitor in series before the device pin. The OSCin inputs are high impedance CMOS with internal bias voltage. TI recommends putting termination shunt resistors to terminate the differential traces (if there are 50-Ω characteristic traces, place 50-Ω resistors). The OSCin and OSCin* side must be matched in layout. A series AC-coupling capacitors must immediately follow OSCin pins in the board layout, then the shunt termination resistors to ground must be placed after.

Input clock definitions are shown in 图 69:

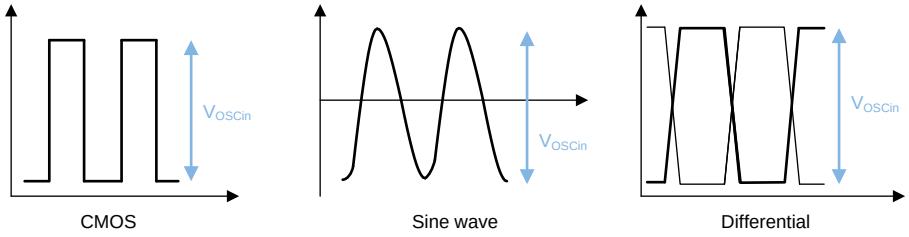


图 69. Input Clock Definitions

8.1.2 OSCin Slew Rate

The slew rate of the OSCin signal can have an impact on the spurs and phase noise of the LMX2615 if it is too low. In general, the best performance is for a high slew rate, but lower amplitude signal, such as LVDS.

8.1.3 RF Output Buffer Power Control

The OUTA_PWR and OUTB_PWR registers control the amount of drive current for the output. This current creates a voltage accross the pull-up component and load. It is generally recommended to keep the OUTx_PWR setting at 31 or less as higher settings consume more current consumption and can also lead to higher output power. Optimal noise floor is typically obtained by setting OUTx_PWR in the range of 15 to 25.

8.1.4 RF Output Buffer Pullup

The choice of output buffer components is very important and can have a profound impact on the output power. The pull-up component can be a resistor or inductor or combination thereof. The signal swing is created is created by a current this pull-up, so a higher impedance implies a higher signal swing. However, as this pull-up component can be treated as if it is in parallel with the load impedance, there are diminishing returns as the impedance gets much larger than the load impedance. The output impedance of the device varies as a function of frequency and is a complex number, but typically has a magnitude on the order of 100 ohms, but this decreases with frequency.

The output can be used differentially or single-ended. If using single-ended, the pullup is still needed, and user needs to terminate the unused complimentary side such that the impedance as seen from the pin looking out is similar to the pin that is being used. Following are some typical components that might be useful.

Application Information (接下页)

表 60. Output Pullup Configuration

COMPONENT	VALUE	PART NUMBER
Inductor	1 nH, 13.6 GHz SRF	Toko LL1005-FH1N0S
	3.3 nH, 6.8 GHz SRF	Toko LL1005-FH3N3S
	10 nH, 3.8 GHz SRF	Toko LL1005-FH10NU
Resistor	50 Ω	Vishay FC0402E50R0BST1
Capacitor	Varies with frequency	ATC 520L103KT16T ATC 504L50R0FTNCFT

8.1.4.1 Resistor Pullup

One strategy for the choice of the pull-up component is to a resistor (R). This is typically chosen to be 50-Ω and under the assumption that the part output impedance is high, then the output impedance will theoretically be 50 ohms, regardless of output frequency. As the output impedance of the device is not infinite, the output impedance when the pull-up resistor is used will be less than 50 ohms, but reasonably close. There will be some drop across the resistor, but this does not seem to have a large impact on signal swing for a 50-Ω resistor provided that OUTx_PWR≤31.

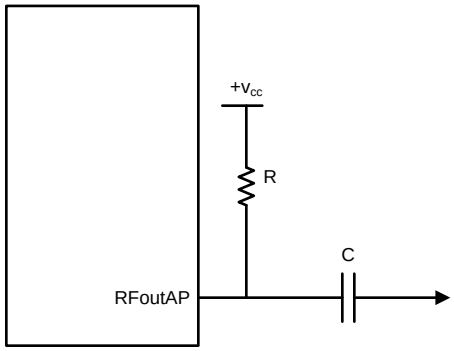


图 70. Resistor Pullup

8.1.4.2 Inductor Pullup

Another strategy is to choose an inductor pull-up (L). This allows a higher impedance without any concern of creating any DC drop across the component. Ideally, the inductor should be chosen large enough so that the impedance is high relative to the load impedance and also be operating away from its self-resonant frequency. For instance, consider a 3.3 nH pull-up inductor with a self-resonant frequency of 7 GHz driving a 25-Ω spectrum analyzer input. This inductor theoretically has j50-Ω input impedance around 2.4 GHz. At this frequency, this in parallel with load is about j35-Ω, which is a 3 dB power reduction. At 1.4 GHz, this inductor has impedance of about 29-Ω. This in parallel with the 50-Ω load has a magnitude of 25-Ω, which is the same as you would get with the 50-Ω pull-up. The main issue with the inductor pull-up is the impedance does not look nicely matched to the load.

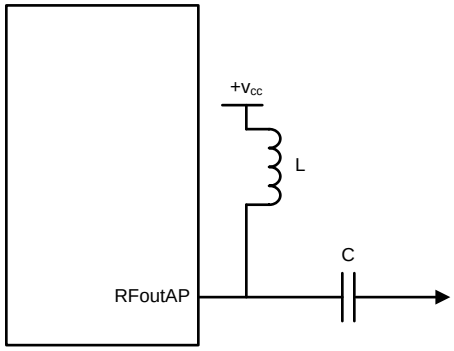


图 71. Inductor Pullup

As the output impedance is not so nicely matched, but there is higher output power, it makes sense to use a resistive pad to get the best impedance control. A 6 dB pad (R1 =18-Ω, R2=68-Ω) is likely more attenuation than necessary; 3 dB or even 1 dB might suffice. Two AC coupling capacitor is required before the pad. In the configuration below, one of them is placed by the resistor to ground to minimize the number of components in the high frequency path for lower loss.

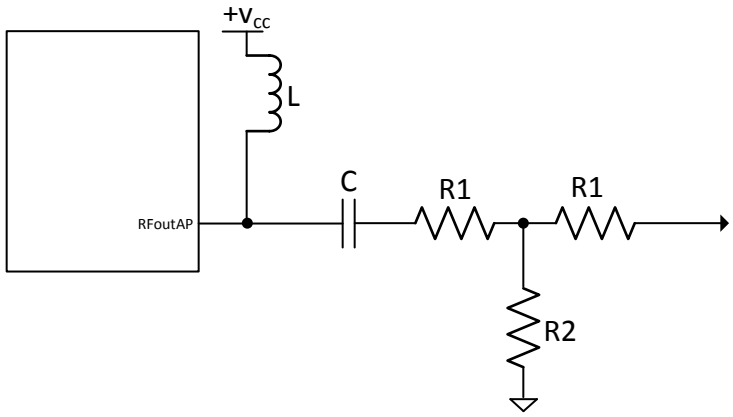


图 72. Inductor Pullup With Pad

For the resistive pad, here are some common values:

表 61. Resitive T-Pad Values

Attenuation	R1	R2
1 dB	2.7 Ω	420 Ω
2 dB	5.6 Ω	220 Ω
3 dB	6.8 Ω	150 Ω
4 dB	12 Ω	100 Ω
5 dB	15 Ω	82 Ω
6 dB	18 Ω	68 Ω

8.1.4.3 Combination Pullup

The resistor gives a good low frequency response, while the inductor gives a good high frequency response with worse matching. It is desirable to have the impedance of the pull-up to be high, but if a resistor is used, then there could be too much DC drop. If an inductor is used, it is hard to find one good at low frequencies and around its self-resonant frequency. One approach to address this is to use a series resistor and inductor followed by resistive pad.

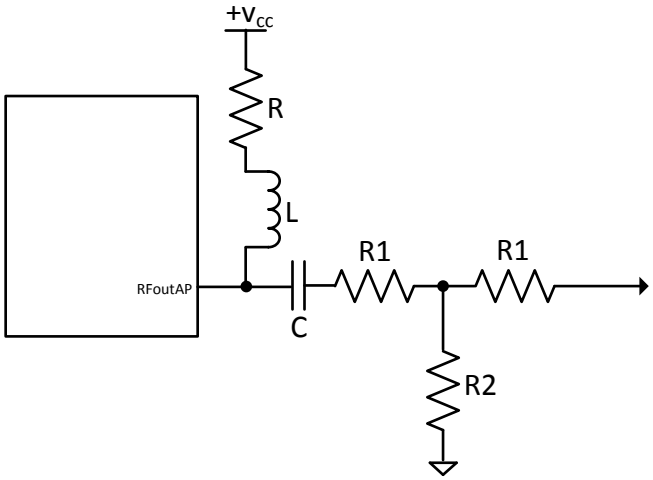


图 73. Inductor and Resistor Pullup

8.1.5 RF Output Treatment for the Complimentary Side

Regardless of whether both sides of the differential outputs are used, both sides should see a similar load.

8.1.5.1 Single-Ended Termination of Unused Output

The unused output should see a roughly the same impedance as looking out of the pin to minimize harmonics and get the best output power. As placement of the pull-up components is critical for the best output power, the routing does not need to be perfectly symmetrical; it makes sense to give highest priority routing to the used output (RFoutA in this case).

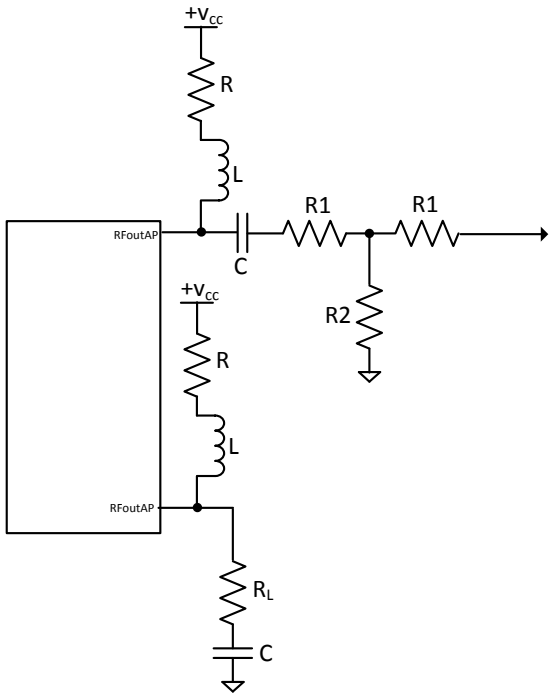


图 74. Termination of Unused Output

8.1.5.2 Differential Termination

For differential termination this can be done by doing the same termination to both sides, or it is also possible to connect the grounds together. This approach can also be accompanied by a differential to single-ended balun for the highest possible output power.

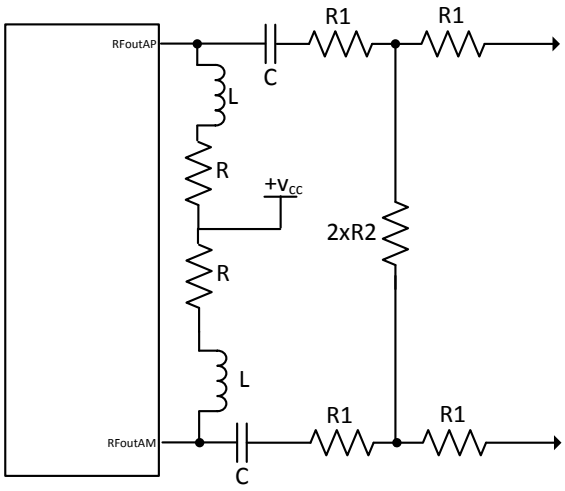


图 75. Termination of Unused Output

8.2 Typical Application

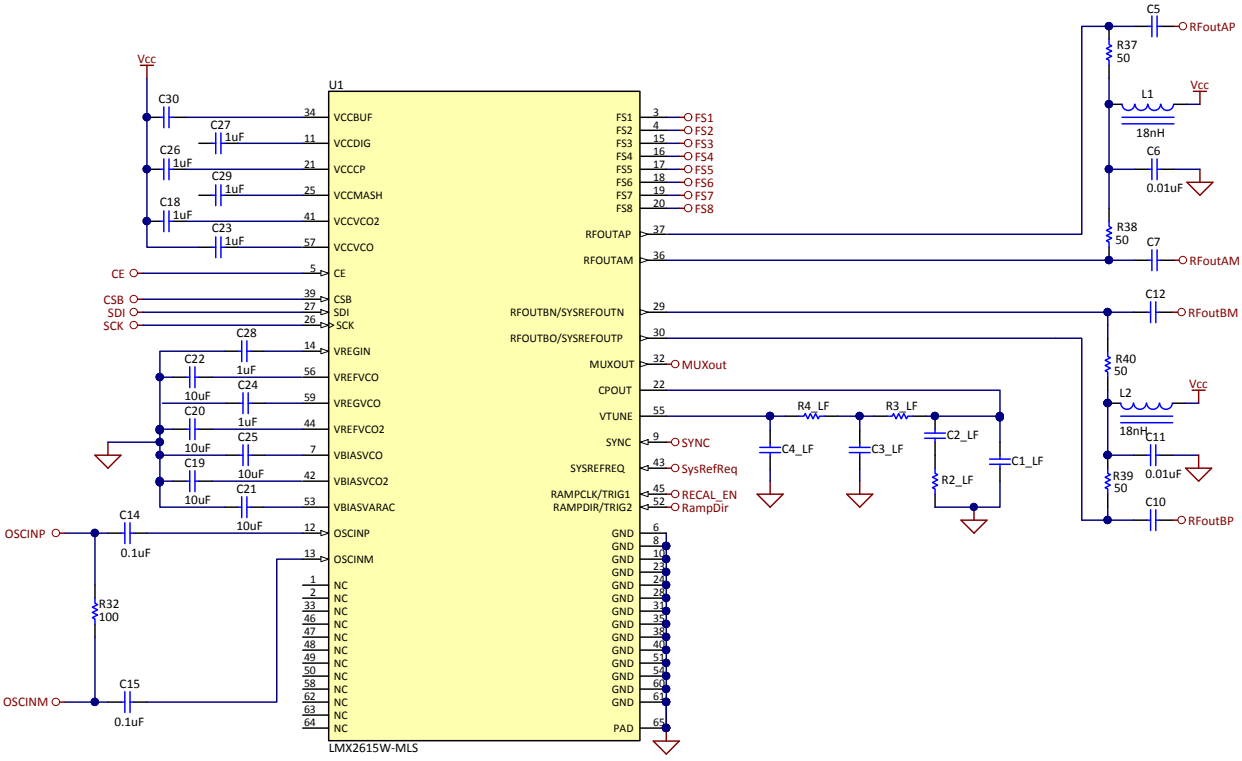


图 76. Typical Application Schematic

Typical Application (接下页)

8.2.1 Design Requirements

The design of the loop filter is complex and is typically done with software. The PLLatinum Sim software is an excellent resource for doing this and the design is shown in图 77. For those interested in the equations involved, the PLL Performance, Simulation, and Design Handbook (SNAA106) goes into great detail as to theory and design of PLL loop filters.

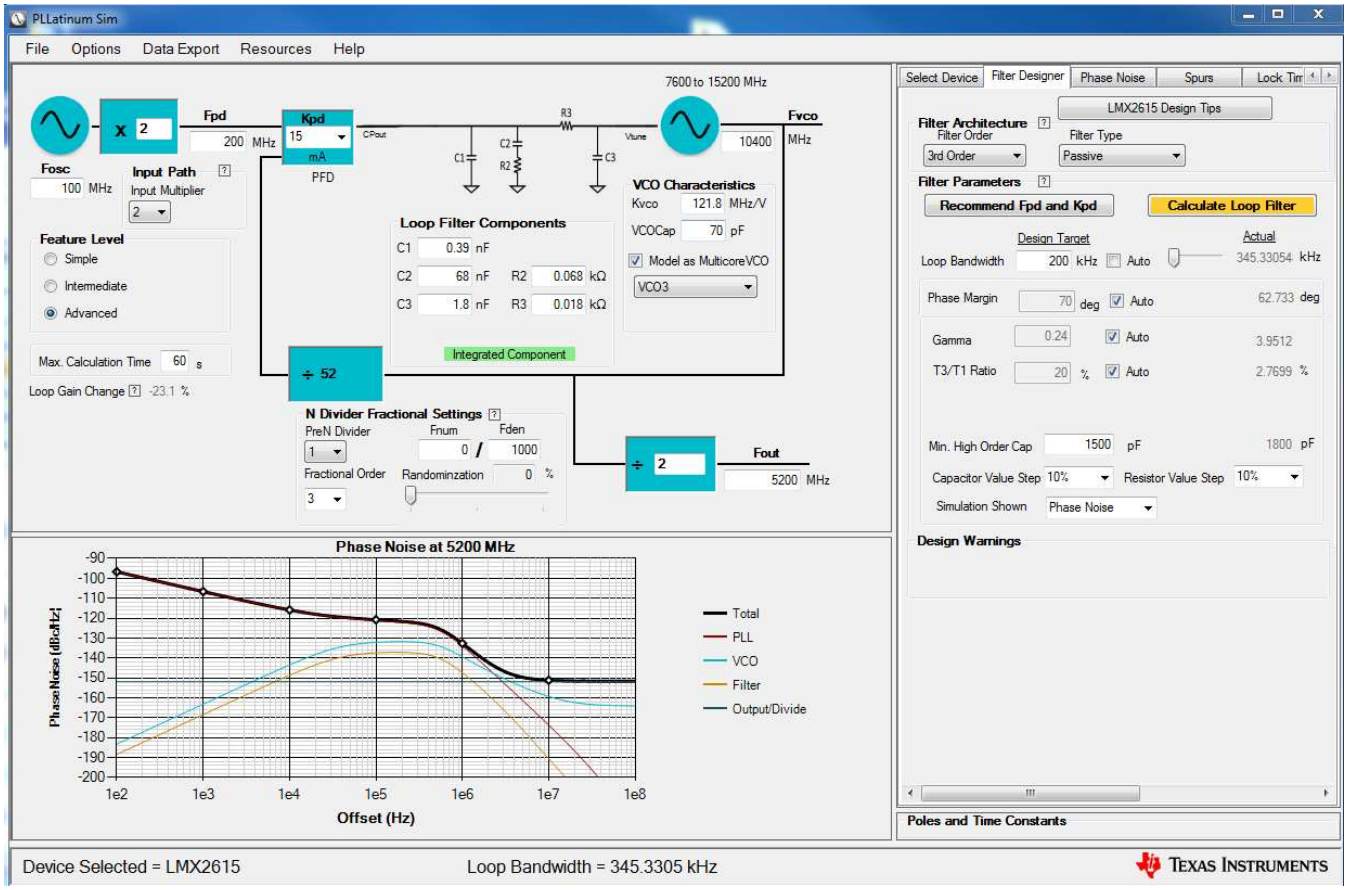


图 77. PLLatinum Sim Tool

8.2.2 Detailed Design Procedure

The integration of phase noise over a certain bandwidth (jitter) is an performance specification that translates to signal-to-noise ratio. Phase noise inside the loop bandwidth is dominated by the PLL, while the phase noise outside the loop bandwidth is dominated by the VCO. Generally, jitter is lowest if loop bandwidth is designed to the point where the two intersect. A higher phase margin loop filter design has less peaking at the loop bandwidth and thus lower jitter. The tradeoff with this is that longer lock times and spurs must be considered in design as well.

Typical Application (接下页)

8.2.3 Application Curve

Using the settings described, the performance measured using a clean 100-MHz input reference is shown. Note the loop bandwidth is about 350 kHz, as simulations predict.

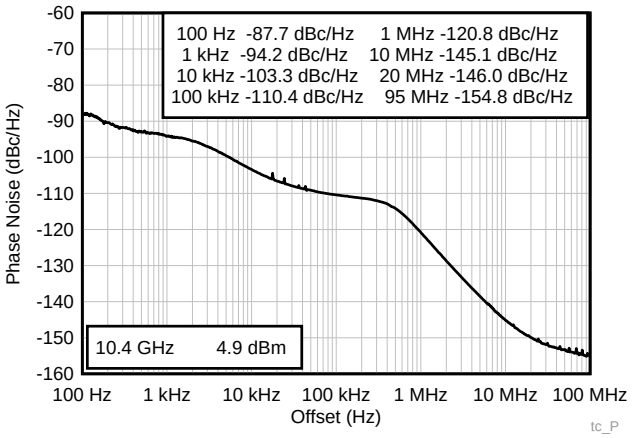


图 78. Results for Loop Filter Design

9 Power Supply Recommendations

TI recommends placement of bypass capacitors close to the pins. Consult the EVM instructions for layout examples. If fractional spurs are a large concern, using a ferrite bead to each of these power supply pins can reduce spurs to a small degree. This device has integrated LDOs, which improves the resistance to power supply noise. However, the pullup components on the RFoutA and RFoutB pins on the outputs have a direct connection to the power supply, so extra care must be made to ensure that the voltage is clean for these pins.

10 Layout

10.1 Layout Guidelines

In general, the layout guidelines are similar to most other PLL devices. Here are some specific guidelines.

- GND pins may be routed on the package back to the DAP.
- The OSCin pins, these are internally biased and must be AC coupled.
- If not used, the SysRefReq may be grounded to the DAP.
- For optimal VCO phase noise in the 200kHz - 1 MHz range, it is ideal that the capacitor closest to the Vtune pin be at least 3.3 nF. As requiring this larger capacitor may restrict the loop bandwidth, this value can be reduced (to say 1.5 nF) at the expense of VCO phase noise.
- For the outputs, keep the pullup component as close as possible to the pin and use the same component on each side of the differential pair.
- If a single-ended output is needed, the other side must have the same loading and pullup. However, the routing for the used side can be optimized by routing the complementary side through a via to the other side of the board. On this side, use the same pullup and make the load look equivalent to the side that is used.
- Ensure DAP on device is well-grounded with many vias, preferably copper filled.
- Have a thermal pad that is as large as the LMX2615 exposed pad. Add vias to the thermal pad to maximize thermal performance.
- Use a low loss dielectric material, such as Rogers 4350B, for optimal output power.

10.2 Layout Example

In addition to the layout guidelines already given, here are some additional comments for this specific layout example

- The most critical part of the layout that the placement of the pull-up components (R37, R38, R39, and R40) is close to the pin for optimal output power.
- For this layout, most of the loop filter (C1_LF, C2_LF, C3_LF, R2_LF, R3_LF, and R4_LF) are on the back side of the board. However note that C4_LF is on the top side right next to the Vtune pin. In the event that this C4_LF capacitor would be open, it is recommended to move one of loop capacitors in this spot. For instance, if a 3rd order loop filter was used, technically C3_LF would be non-zero and C4_LF would be open. However, for this layout example that is designed for a 4th order loop filter, it would be optimal to make R3_LF = 0 ohm, C3_LF = open, and C4_LF to be whatever C3_LF would have been.

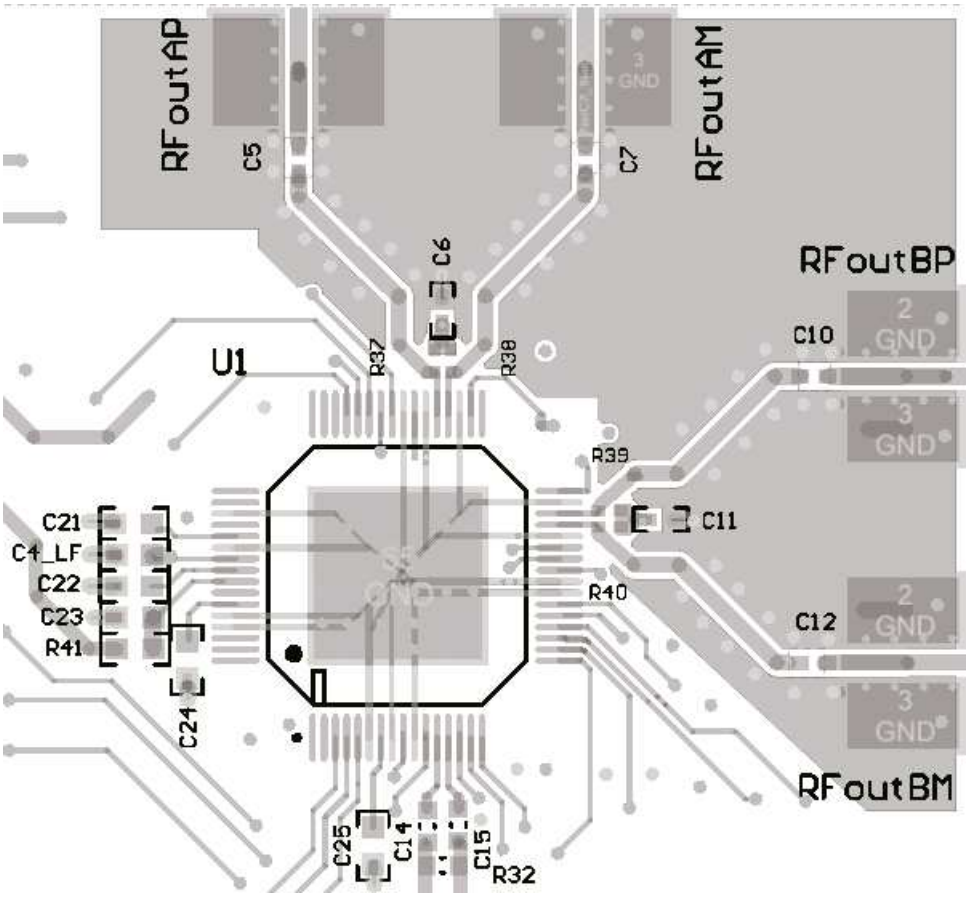
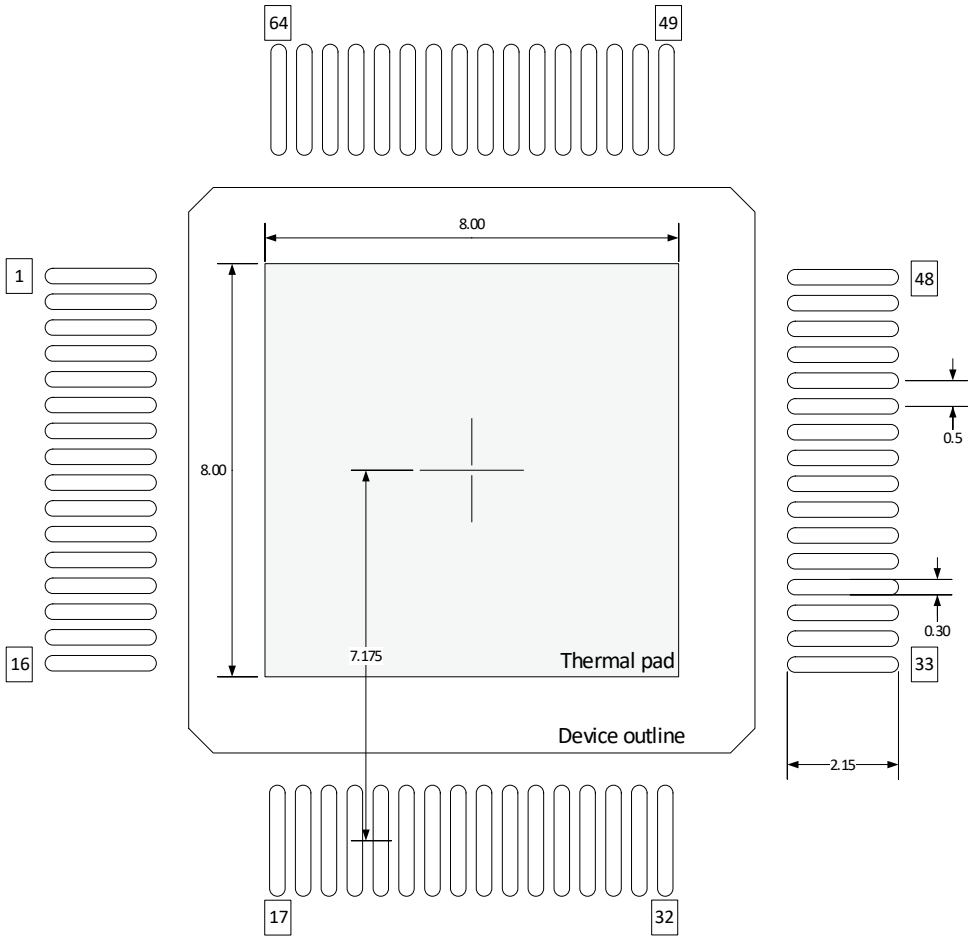


图 79. LMX2615 Layout Example

10.3 Footprint Example on PCB Layout



1. All dimensions in millimeters.
2. Top view

图 80. LMX2615 PCB Layout

10.4 Radiation Environments

Careful consideration must be given to environmental conditions when using a product in a radiation environment.

10.4.1 Total Ionizing Dose

Radiation Hardness assured (RHA) products are those part numbers with a total ionizing dose (TID) level specified in the ordering information. Testing and qualification of these product is done on a wafer level according to MIL-STD-883, test method 1019. Wafer level TID data are available with lot shipments.

10.4.2 Single Event Effect

One time single event effect (SEE), including single event latch-up (SEL), single event functional interrupt (SEFI) and single event upset (SEU), testing was performed according to EIA/JEDEC Standard, EIA/JEDEC57. A test report is available upon request.

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

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11.1.2 开发支持

德州仪器 (TI) 在 www.ti.com.cn 提供了多种辅助开发的软件工具。其中包括：

- EVM 软件，用于了解如何对器件和 EVM 板进行编程。
- EVM 板说明，用于了解典型测量数据、详细测量条件以及完整设计的信息。
- PLLatinum Sim 程序，用于设计回路滤波器以及对相位噪声和杂散进行仿真。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- *《AN-1879 分数 N 频率合成》*(SNAA062)
- *《PLL 性能、仿真和设计手册》*(SNAA106)

11.3 商标

All trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

12.1 工程样片

工程样片 (LMX2615W-MPR) 具有与运行器件 (LMX2615W-MLS) 相同的封装、引脚、编程和典型性能。这些器件在室温下经过测试，符合电气规范，但尚未经历或通过全面的生产流程或测试。工程样片可能被 QCI 拒绝，无法通过全面的生产测试（如辐射或可靠性测试）。

12.2 封装机械信息

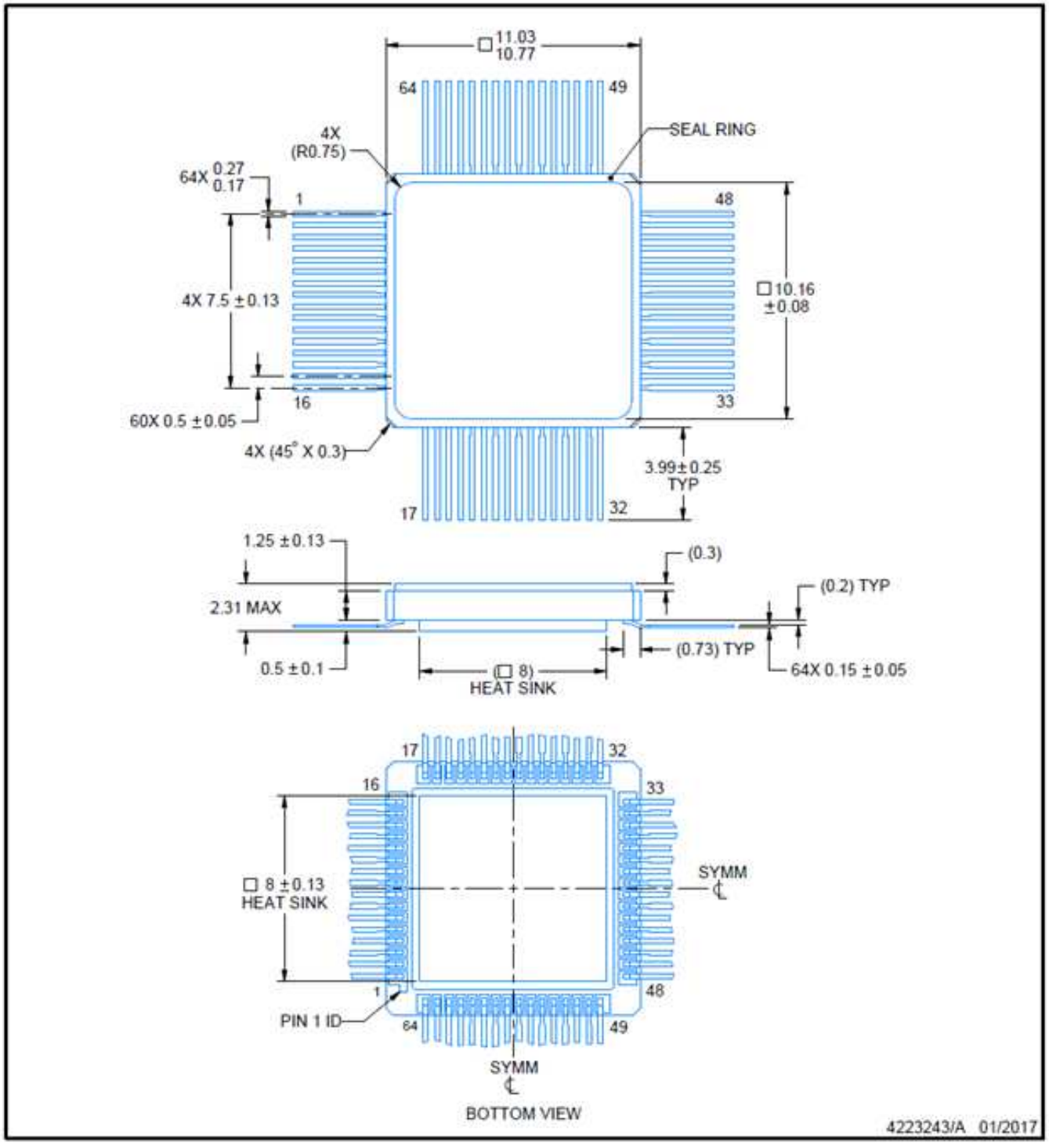


图 **81.** 封装机械信息

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962R1723601VXC	ACTIVE	CFP	HBD	64	14	RoHS & Green	NIAU	Level-1-NA-UNLIM	-55 to 125	5962R1723601VXC LMX2615WRQMLV	Samples
LMX2615-MKT-MS	ACTIVE	CFP	HBD	64	1	TBD	Call TI	Call TI	25 to 25	LMX2615-MKT-MS MECHANICAL	Samples
LMX2615W-MPR	ACTIVE	CFP	HBD	64	14	RoHS & Green	NIAU	Level-1-NA-UNLIM	25 to 25	LMX2615W-MPR ENG SAMPLE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

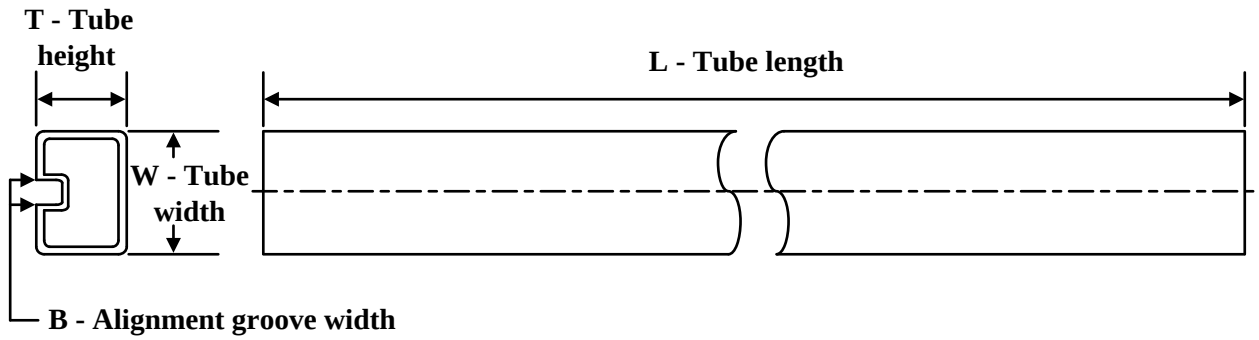
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

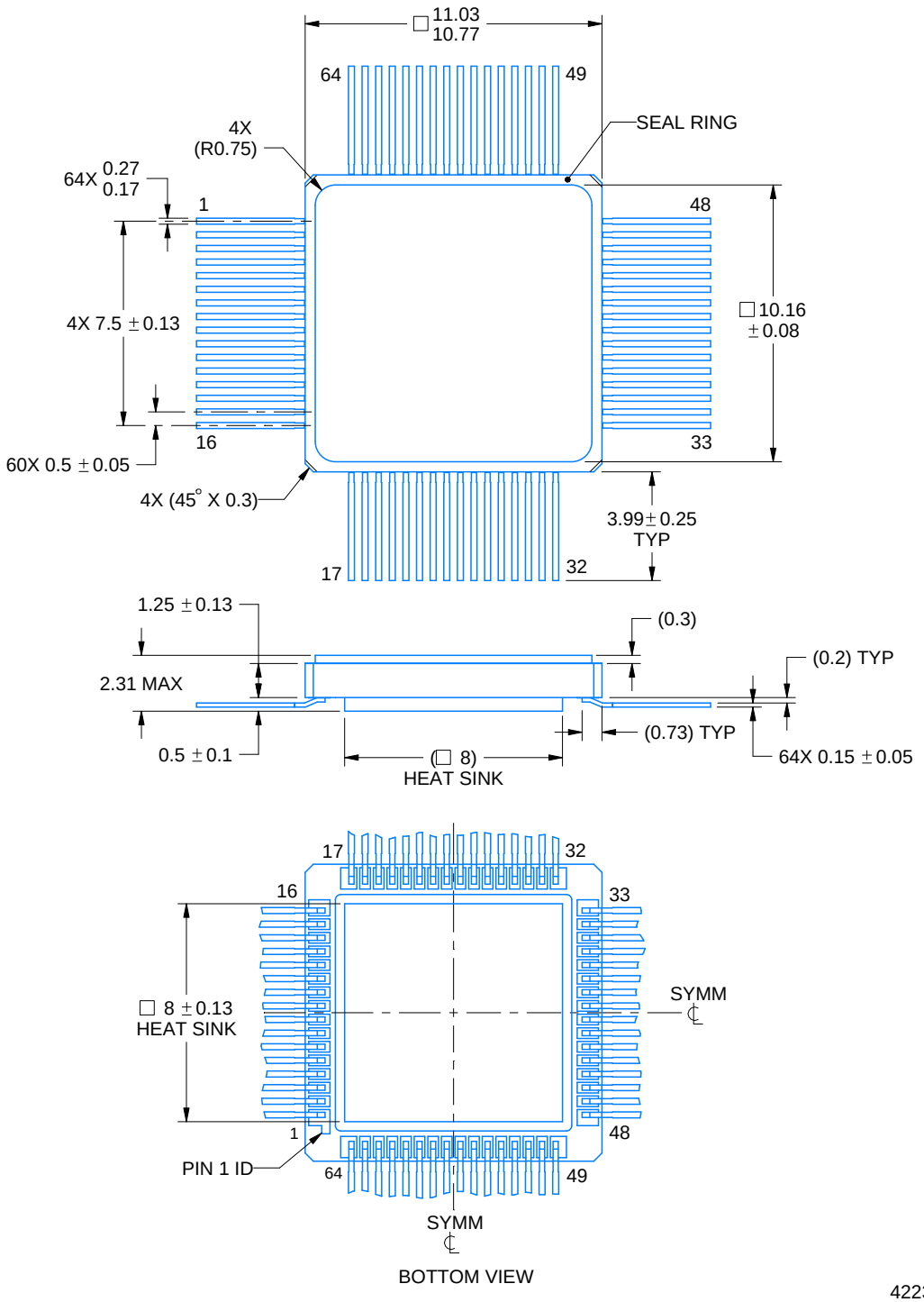
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R1723601VXC	HBD	CFP (HSL)	64	14	495	33	11176	16.51
LMX2615W-MPR	HBD	CFP (HSL)	64	14	495	33	11176	16.51

PACKAGE OUTLINE

HBD0064A

CFP - 2.31 mm max height

CERAMIC FLATPACK



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. Ground pad to be electronic connected to heat sink and seal ring.
5. The leads are gold plated and can be solder dipped.

重要声明和免责声明

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