TI 参考设计：TIDA-01004
采用 100 万像素成像仪、Bayer 视频输出和同轴电缆供电技术的汽车摄像头模块设计

说明

TIDA-01004 参考设计是一种高速串行视频接口，通过此接口，可将远程汽车摄像头模块连接到显示器或机器视觉处理系统。此设计使用 TI 的 FPD-Link III SerDes 技术，可传输未经压缩的百万像素视频数据和双向控制信号，并通过同轴电缆进行供电。

资源

TIDA-01004	摄像头模块	设计文件夹
DS90UB933-Q1	FPD-Link III 串行器	产品文件夹
TPS62170-Q1	降压转换器	产品文件夹
TPS62231-Q1	降压转换器	产品文件夹
TPS3808G18-Q1	电压监控器	产品文件夹

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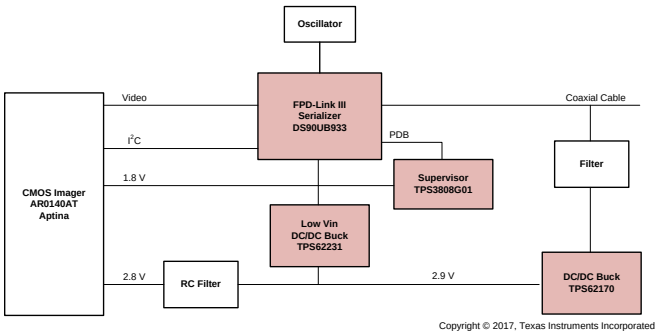
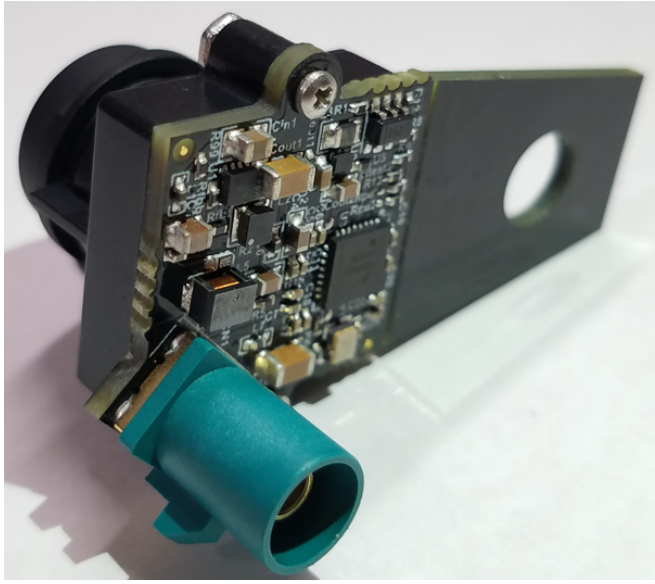
特性

- 设计经过空间优化，可安装在 20 x 20mm 的单块 PCB 上
- 经过电源优化，减小了尺寸，提高了效率
- 配备 ON Semiconductor 的 100 万像素传感器 AR0140AT，可提供 10 位或 12 位原始图像数据
- 配备适用于数字视频、电源、控制和诊断的单个 Rosenberger Fakra 同轴电缆连接器
- 适用于 ASIL B 应用的诊断和内置 自检 (BIST)
- 包含设计注意事项和 BOM 分析

应用

- ADAS 视觉系统
- 环视系统
- 后置摄像头





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1 System Description

For many automotive safety systems, small cameras are required. This TI Design addresses these needs by combining a 1-megapixel imager with a 1.9-Gbit/s serializer and providing the necessary power supply for both. All of this functionality is contained on a 20×20-mm circuit board. The only connection required by the system is a single 50-Ω coaxial cable.

A combined signal containing the DC power, the FPD-Link front and back channels enter the board through the FAKRA coax connector. The filter shown in 图 1 blocks all of the high-speed content of the signal (without significant attenuation) while allowing the DC (power) portion of the signal to pass through inductor L5.

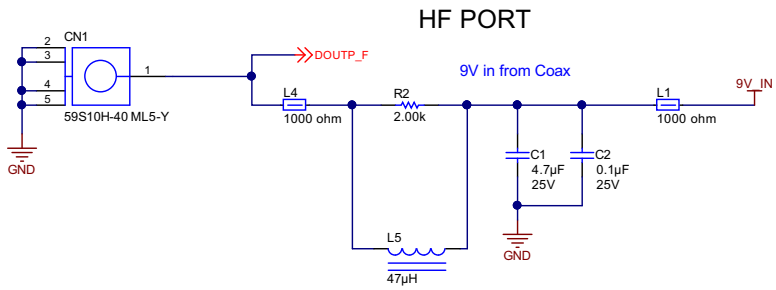

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图 1. FPD-Link III Signal Path

The DC portion is connected to the input of the TPS62170 buck converter to output 2.9 V. The other 1.8-V rail required by the serializer and the imager are created by TPS62231 buck converter.

The high-frequency portion of the signal is connected directly to the serializer. This is the path that the video data and the control back channel will take between the serializer and deserializer.

The output of the CMOS imager is connected through a parallel digital video port to the serializer. This 10- or 12-bit video data (with two sync signals) is converted to a single high-speed serial stream that is transmitted over a single LVDS pair to the deserializer located on the other end of the coax cable.

On the same coax cable, there is separate low latency bidirectional control channel that transmits control information from an I^2C port. This control channel is independent of video blanking period. It is used by the system microprocessor to configure and control the imager.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage	Power over coax (POC)	4	12	17	V
P_{TOTAL}	Total power consumption	V_{POC} = 12 V	—	0.6	1	W
F_{PCLK}	Pixel clock frequency	—	37.5	—	100	MHz

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2 System Overview

2.1 Block Diagram

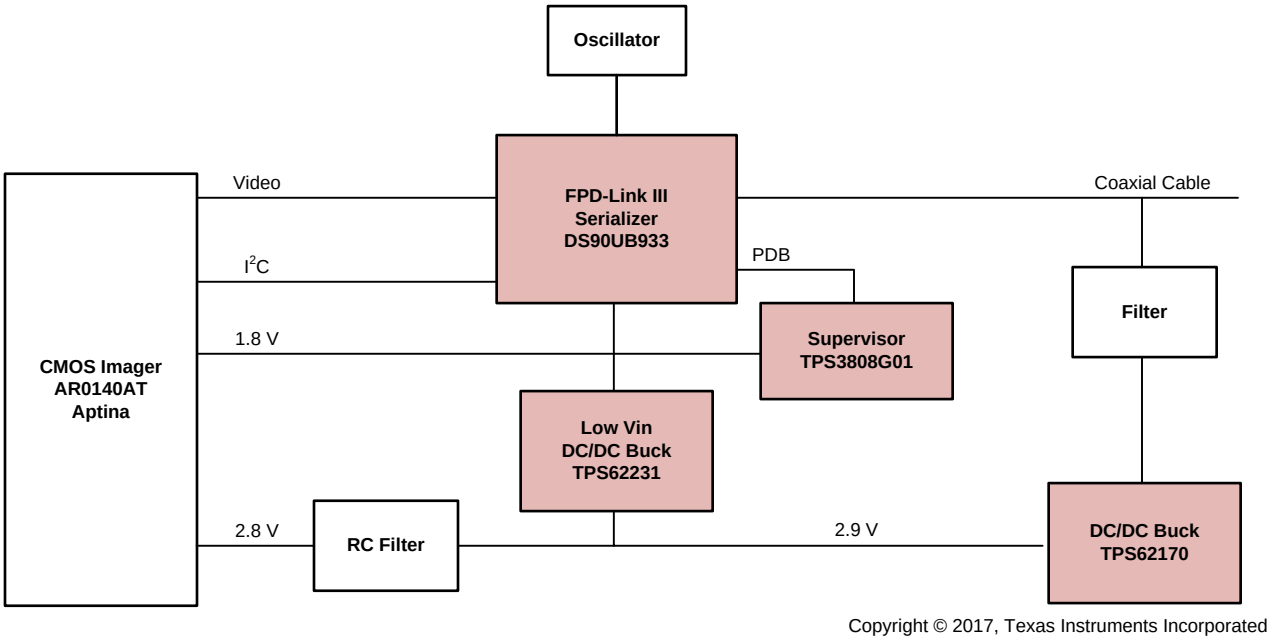

图 **2. Camera Block Diagram**

2.2 Highlighted Products

This TI Design uses the following TI products:

- DS90UB933-Q1: the serializer portion of a chipset that offers a FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coaxial cable or differential pair. This chipset incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The serializer and deserializer pair is targeted for connections between imagers and video processors in an electronic control unit (ECU)
- TPS62170-Q1: an automotive qualified step-down DC converter optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response
- TPS62231-Q1: an automotive qualified fixed-output voltage, 500-mA step-down DC converter. The high switching frequency of up to 3.8 MHz allows for small inductors and a fast transient response
- TPS3808G18-Q1: a supply voltage supervisor that monitors supply voltage and keeps a device from powering on until a certain supply voltage threshold is reached. In this case, the supervisor keeps the PDB pin of the serializer in the low state until the supply reaches 1.67 V

Find more information on each device and why they were chosen for this application in the following subsections.

TIDUCR4 — http://www-s.ti.com/sc/techlit/TIDUCR4
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2.2.1 AR0140AT Imager

Available from the ON semiconductor, this imager is a ¼-inch 1.0 megapixel, a CMOS imager with high dynamic range (HDR). It is suitable for automotive systems and can provide a 10- or 12-bit parallel output. Some additional features of the imager are:

- Supports image sizes: 1280×800 and 720p (16:9) images
- Low power consumption
- Requires two voltage rails (1.8 V and 2.8 V)
- Can be configured using an I^2C-compatible two-wire serial interface

2.2.2 DS90UB933-Q1

Using a serializer to combine 12-bit video with a bidirectional control signal onto one coax or twisted pair greatly simplifies system complexity, cost, and cabling requirements. The parallel video input of the DS90UB933-Q1 mates well with the 12-bit parallel video output of the AR0140AT imager. Once combined with the filters for the power over coax (POC), video, I^2C control, diagnostics, and power can all be transmitted up to 15 meters on a single inexpensive coax cable. For more information on the cable itself, see the application report *Cable Requirements for the DS90UB913A and DS90UB914A* (SNLA229).

2.2.3 TPS62170-Q1

To keep the camera small, the power supply must be small. It must also be power efficient while not adding measurable noise to the video from the imager. Often, these two requirements stand in opposition. A switching power supply is more efficient than a linear regulator, but it can add noise to the system.

Camera sensor circuits usually are sensitive to noise at frequencies below 1 MHz. To avoid interference with the AM radio band, staying above 2 MHz is desirable in automotive applications. This means that the TPS62170-Q1 switching regulator operating at 2.25 MHz meets both requirements. This high switching frequency also helps to reduce the size of the discrete components in the circuit.

2.2.4 TPS62231-Q1

This device is simpler to design with because it is a fixed-voltage step down converter. The TPS6223x series features a switching frequency of up to 3.8 MHz, which avoids the AM radio band.

One additional feature of the TPS62231-Q1 not available on the TPS62170-Q1 is a MODE pin. By pulling this pin up, PWM mode can be forced across the full load range. However, with the typical load current of this system, the PWM mode option would provide any benefits.

2.2.5 TPS3808G18-Q1

The PDB pin of the serializer allows the device to be held in a power-down mode until the voltages in the rest of the system have stabilized. It is important that the ID(X) and MODE pins, supply rails, and oscillator of the serializer are stable when the device comes out of the reset.

The supply voltage supervisor manages a safe power-on of the serializer by monitoring the 1.8-V supply voltage rail. This device holds the PDB pin of the serializer in the low state, preventing the serializer from turning on, until the 1.8-V supply voltage rail reaches a threshold voltage, about 1.67 V in this case. Once this threshold voltage is reached, there is a hard 20-ms delay until the supervisor releases the serializer from reset.

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2.3 Design Considerations

The following subsections discuss the considerations behind the design of each subsection of the system.

2.3.1 PCB and Form Factor

This TI Design was not intended to fit any particular form-factor. The only goal of the design with regards to the PCB was to make as compact a solution as possible. The square portion of the board is 20 mm × 20 mm. The area near the board edge in the second image is reserved for attaching the optics housing that holds the lens.

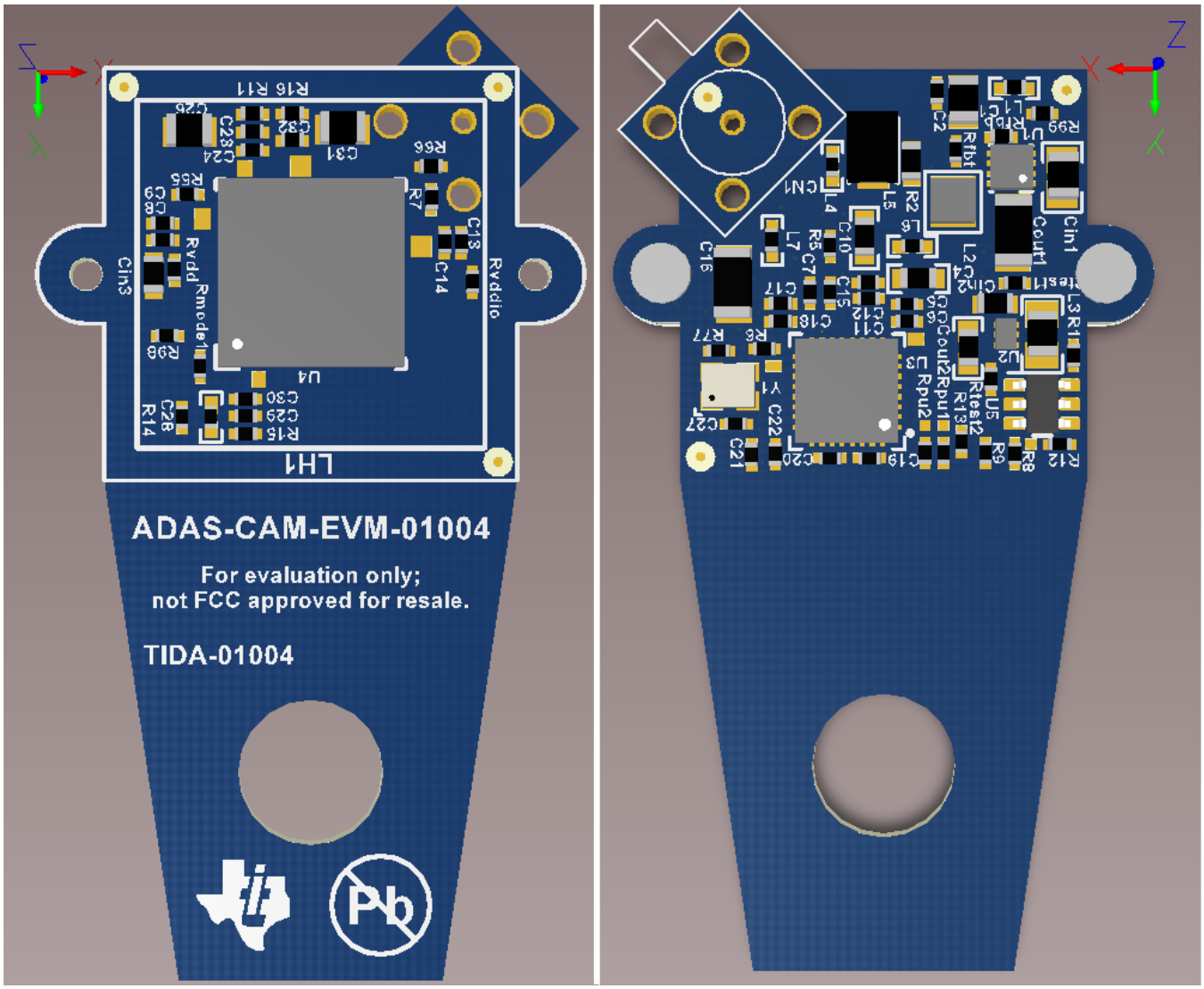

图 **3. PCB Top and Bottom Views**

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2.3.2 Power Supply Design

2.3.2.1 POC Filter

One of the most critical portions of a design that uses POC is the filter circuitry. The goal is twofold:

1. Deliver a clean DC supply to the input of the switching regulators, and
2. Protect the FPDLink communication channels from noise coupled backwards from the rest of the system

The DS90UB933/DS90UB934 SerDes devices used in this system communicate over two carrier frequencies, 1 GHz at full speed ("forward channel") and a lower frequency between 2 and 4 MHz ("back channel") determined by the deserializer device. The filter must attenuate this rather large band spanning both carriers, hoping to pass only DC. Luckily, by filtering the back channel frequency, this TI Design also filters the frequencies from the switching power supplies on the board.

For the POC design, to enable the forward channel and back channel to pass uninterrupted over the coax, a impedance of > 1 kΩ across the 2-MHz to 1-GHz bandwidth is required. By using a 47-µH inductor with very wide high impedance characteristics for the low to mid frequencies in series with a ferrite bead to filter at the 1-GHz range, noise suppression can be obtained for the DC line. In addition, a 2-kΩ resistance in parallel with the 47-µH inductor will bring the impedance up further for all frequency ranges. With this approach, the solution size can be minimized on board for the POC inductor filtering. See the application report *Sending Power Over Coax in DS90UB913A Designs* (SNLA224) for more details.

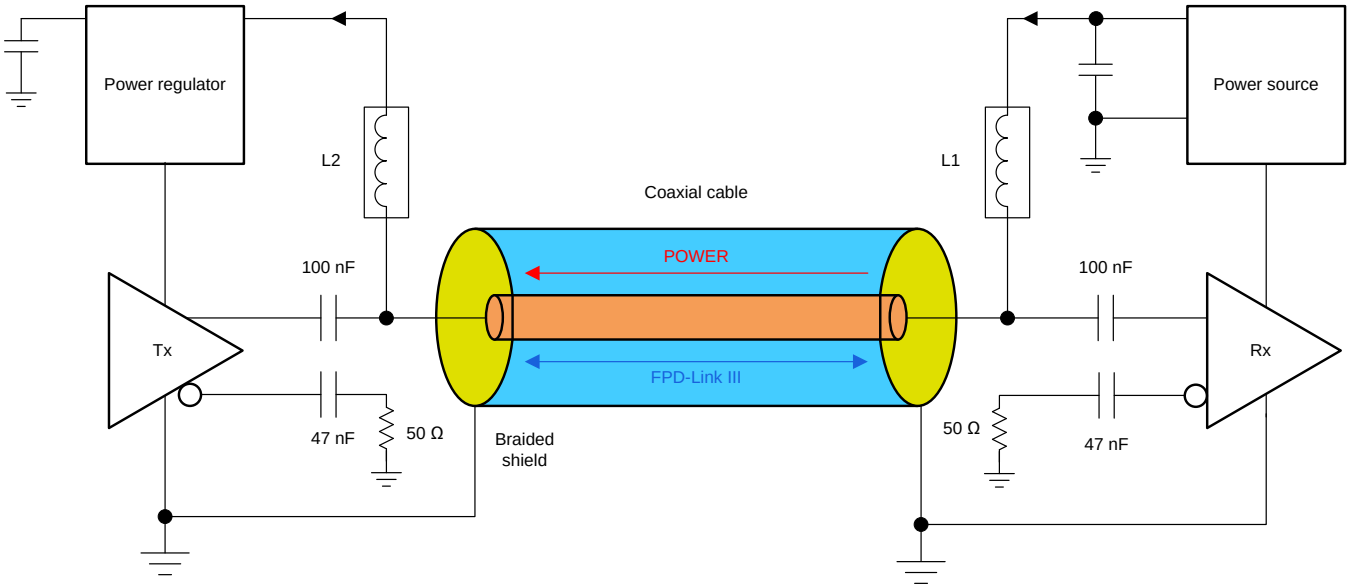

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图 **4. Power Over Coax**

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2.3.2.2 Power Supply Considerations

Because this TI Design is targeted at automotive applications, there are a few considerations that constrict design choices. In addition, there are few systems-level specifications that shaped the overall design:

- The total solution size needs to be minimized to meet size requirement of this design, which is less than 20 mm × 20 mm. This means choosing parts that integrate FETs, diodes, compensation networks, and feedback resistor dividers to eliminate external circuitry.
- To avoid interference with the AM radio band, all switching frequencies need to be greater than 1700 kHz or lower than 540 kHz. Lower switching frequencies are less desirable in this case because they require large inductors and can still produce harmonics in the AM band. For this reason, this TI Design looks at higher frequency switchers.
- All devices need to be AEC Q100-Q1 rated.

Before choosing parts, know the input voltage range, rails needed, and current required by each rail. In this case, the input voltage is a pre-regulated 9-V supply coming in over coax. The range is discussed later, but this is the nominal value. This system has only two main ICs, which will consume the majority of the power. The requirements for each supply on these devices are shown in 表 2:

表 2. Power Budget

PARAMETER	VOLTAGE (V)	CURRENT (TYP) (A)	CURRENT (MAX) (A)	POWER (TYP) (W)	POWER (MAX) (W)
DS90UB933-Q1					
VDDT	1.8	0.0610	0.080	0.1098	0.1440
VDDIO	1.8	0.0015	0.003	0.0027	0.0054
AR0140T					
VDD	1.8	0.1200	0.140	0.2160	0.2520
VDDIO	1.8	0.0180	0.025	0.0324	0.0450
VAA	2.8	0.0350	0.045	0.0980	0.1260
VAA_PIX	2.8	0.0030	0.004	0.0084	0.0112
VDD_PLL	2.8	0.0060	0.008	0.0168	0.0224
RAIL TOTAL					
1.8-V rail	1.8	0.2005	0.248	0.3609	0.4464
2.8-V rail	2.8	0.0440	0.057	0.1232	0.1596
OVERALL TOTAL	—	0.2445	0.305	0.4841	0.6060

Summing these values, the 1.8-V rail requires 248 mA and the 2.8-V requires 57 mA. If choosing to cascade these power supplies, then the 2.8-V regulator will actually need to source the current for the 1.8-V rail as well. This neglects the consumption of passive components, oscillator, IC quiescent currents, and so on, but this is a good ballpark number.

Because the input and output voltages, output current requirements, and total wattage consumption are known, calculate what the input currents will look like with 公式 1:

$$P_{OUT} = P_{IN} = I_{IN} \times V_{IN} \rightarrow 606\ \text{mW} = I_{IN} \times 9\ \text{V} \rightarrow I_{IN} = 67.33\ \text{mA}\ (\text{max}) \tag{1}$$

These numbers gives a good starting point for selecting the parts and topology for the regulators as well as inductor selections later on. However, this does not take into account the efficiencies of the power supplies.

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As previously mentioned, the parts in the power supply need to be Q100 rated, switch outside the AM band, and satisfy the voltage and current requirements as listed. Because the input voltage is a regulated voltage that will always be greater than any of the power rail needs, only choose from step-down converters and LDOs.

The key feature of the system is the small size, so integration of external circuitry is a high priority. Integrating FETs, compensation networks, and sometimes feedback, can significantly reduce total solution size. Many buck regulators integrate everything but the input/output caps and the inductor into very small packages. High integration also loses a lot of efficiency across different operating points. However, this TI Design sacrifices some efficiency for size and simplicity reasons.

Ultimately, two device families are good candidates, the TPS621x0 (TPS62170 for the 2.9-V rail), TPS621x1 (possibly the TPS62171 as an option for the 1.8-V rail), and TPS6223x (TPS62231 is the fixed 1.8-V option).

Because there are only two rails, the TIDA-01004 could have either a parallel topology (both rails being fed by the input voltage) or a cascaded topology (one rail is fed by the input voltage, and then feeds the second rail). This design guide presents a few sample options, including buck regulator only (which is what the final design uses), buck+LDO, and LDO-only solutions.

Clearly the largest trade-off with using LDOs is that the efficiency drops significantly, raising the total power draw to over 1 W. This TI Design is a lower-power design; however, in some situations a designer may sacrifice the efficiency to avoid the inherent noise and EMI issues associated with switching power supplies.

Another decision to make is parallel versus cascaded topologies. In this case, the parallel topology is actually the most efficient. However, it presents a few problems, especially in the case of the TPS62170+TPS62171 parallel combination. The first issue is that the TPS62170 would be running in discontinuous mode, which could potentially introduce noise into the system that is different from the typical switching frequency. The second issue is that the design now has two different regulators introducing noise backwards to the input. Because they have similar switching frequencies, this could cause low-frequency beat frequencies that are very difficult to filter out. This TI Design sacrifices efficiency to avoid these possible issues.

Ultimately, this TI Design uses the TPS62170 and TPS62231 cascaded topology. It is significantly more efficient than designs using LDOs, although not the most efficient design available. However, it is lower in cost than the more efficient options. Functionally, the cascaded topology means that the output current is sufficient such that neither device will operate in discontinuous mode, allowing better predictions and control of the switching noise produced by the devices, and operate with better efficiency.

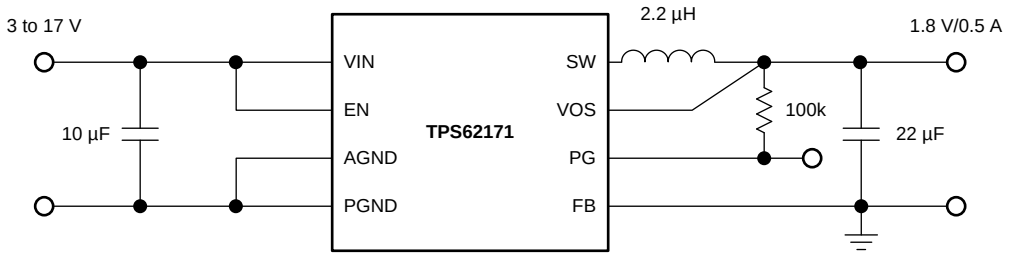

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图 **5. Typical Application Circuit**

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Component selection and design theory can be found in the Application Information section of the device datasheet[2].

2.3.2.2.1 Choosing the Output Inductor

As mentioned in 节 2.3.2.2, the switching frequency of the converter must remain above 2 MHz. This means that the converter must always operate in continuous mode. Because input voltage and output voltage are fixed and the output current is almost constant and can be predicted easily, the minimum inductance, L, for the converter to operate with continuous inductor current can be calculated using 公式 2:

$$L = \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{2 \times V_{IN} \times I_{OUT} \times f} = \frac{2.9\ V\left(14\ V - 2.9\ V\right)}{2 \times 14\ V \times 0.2445\ A \times 2.1\,MHz} = 2.24\ \mu H \tag{2}$$

Because 2.24 µH is just above a standard 2.2-µH inductor value, the next higher value of 3.3 µH is chosen.

2.3.2.2.2 Choosing the Output Capacitor

Because the device is internally compensated, it is only stable for certain component values in the LC output filter. The application note on optimizing the output filter[6] has the chart of stable values shown in 表 3. The value 3.3 µH is on this chart and with these recommended values, this TI Design uses a 22-µF output capacitor and remains in the stable region of effective corner frequencies.

表 3. Stability versus Effective LC Corner Frequency

NOMINAL INDUCTANCE VALUE	NOMINAL CERAMIC CAPACITANCE VALUE (EFFECTIVE = ½ NOMINAL)								
	4.7 µF	10.0 µF	22 µF	47 µF	100 µF	200 µF	400 µF	800 µF	1600 µF
	EFFECTIVE CORNER FREQUENCIES (kHz)								
0.47 µH	151.4	103.8	70.0	47.9	32.8	23.2	16.4	11.6	8.2
1.00 µH	103.8	71.2	48.0	32.8	22.5	15.9	11.3	8.0	5.6
2.2 µH	70.0	48.0	32.4	22.1	15.2	10.7	7.6	5.4	3.8
3.3 µH	57.2	39.2	26.4	18.1	12.4	8.8	6.2	4.4	3.1
4.7 µH	47.9	32.8	22.1	15.1	10.4	7.3	5.2	3.7	2.6
10.0 µH	32.8	22.5	15.2	10.4	7.1	5.0	3.6	2.5	1.8

	Recommended for TPS6213x/TPS6214x/TPS6215x/TPS6216x/TPS6217x
	Recommended for TPS6213x/TPS6214x/TPS6215x only
	Stable without Cff (within recommended LC corner frequency range)
	Stable without Cff (outside recommended LC corner frequency range)
	Unstable

With the inductance value chosen, the design now needs an inductor with a proper saturation current. This is going to be the combination of the steady-state supply current as well as the inductor ripple current. The current rating needs to be sufficiently high but minimized as much as possible to reduce the physical size of the inductor. Calculate the inductor ripple current (from the datasheet[2]) using 公式 3:

$$\Delta I_L = V_{OUT} \times \left(\frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{L \times f_{SW}} \right) \tag{3}$$

The parameters for this TI Design using the TPS62170 are:

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- V_{OUT} = 2.9 V
- V_{IN} = 14 V
- L = 3.3 µH
- f_{SW} = 2.25 MHz

which yields an inductor current of ΔI_L = 310 mA. The maximum current draw of the system through this regulator is 305 mA. Finally, 公式 4 gives the minimum saturation:

$$L_{SAT} \geq \left(I_{MAX} + \frac{I_{RIPPLE}}{2}\right) \times 1.2 = \left(305\ \text{mA} + \frac{310\ \text{mA}}{2}\right) \times 1.2 = 410\ \text{mA} \tag{4}$$

The TIDA-01004 uses a Coilcraft® XPL2010-332MLB, which has a saturation current of 700 mA and with a 20% drop in inductance. This part comes in a very small 1.9×2.0-mm package.

The output voltage is determined by the resistor divider to the feedback pin. 公式 5 calculates the output voltage, which is aimed for 3.3 V_{OUT}, but it needs to work with readily available resistor values:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \rightarrow V_{OUT} = \left(\frac{R1}{R2} + 1\right) \times V_{REF} = \left(\frac{261\ \text{k}\Omega}{100\ \text{k}\Omega} + 1\right) \times 0.8\ \text{V} = 2.89\ \text{V} \tag{5}$$

This gives a close enough output voltage to the desired 2.9 V. For improved accuracy, all FB resistor dividers must use components with 1% or better tolerance.

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2.3.2.3 TPS62231-Q1

This device is easier to design with than the TPS62170 because it is a simpler, fixed voltage device. However, the considerations are quite similar. Following the same procedure as the TPS62170, select the output LC filter for this supply. This converter is stable with a 1- or 2.2-µH inductor and a 4.7-µF capacitor. The larger inductance was chosen in this case in part to reduce ripple current (important for keeping the regulator in continuous mode), but also to use the same inductor for both regulators, reducing the unique BOM count. The previous equations can be used to find a minimum L_{SAT} of 360 mA, which the inductor covers easily.

The only additional feature of this device not present on the TPS62170 is the mode select pin. Pulling this pin up forces PWM mode. With a typical load current, the PFM/PWM mode option would not provide additional efficiency benefits.

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3 Getting Started Hardware

The TIDA-01004 needs only one connection to a system with a compatible deserializer over the FAKRA connector as shown in 图 6.

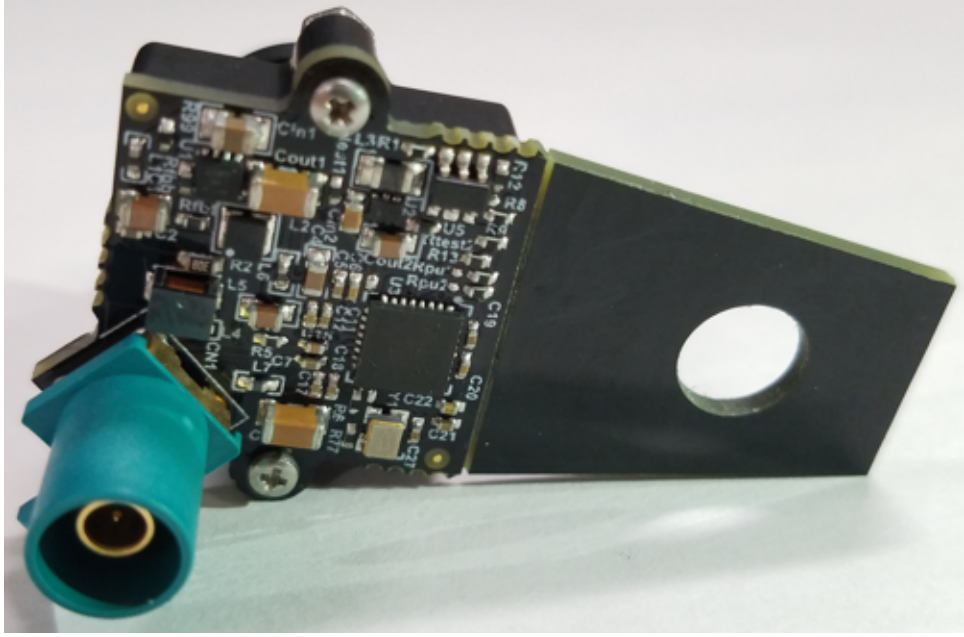

图 **6. Getting Started With Board**

3.1 Video Output Hardware Setup

The setup for testing video output on the TIDA-01004 camera module is displayed in 图 7. The TIDA-01004 includes a DS90UB933, which connects over POC to a DS90UB934EVM. The DS90UB934EVM is connected to a Demo3 evaluation board from OnSemi through an MSB aligned adapter board so that the AR0140AT can communicate to DevWare X software. Tuning the video output characteristics for the AR0140AT imager can be done from DevWare X software over the I^{2}C back channel. In addition to the main setup of the video data signal chain, an Aardvark I^{2}C adapter is used to run initialization scripts on the deserializer, serializer, and imager before DevWare X programs the sensor.

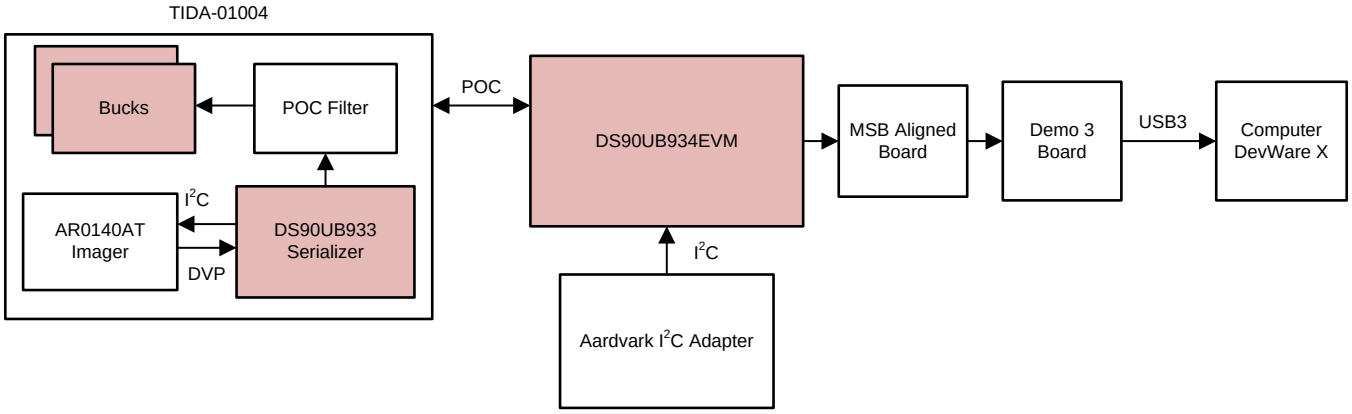

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图 **7. Video Output Setup Block Diagram**

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3.2 FPD-Link III I²C Initialization

With the setup in 图 7 connected, the DS90UB934EVM is supplied a 12-V supply, which powers the DS90UB934 and also the POC to provide input power to the TIDA-01004. Now that the AR0140AT, DS90UB933, and DS90UB934 have power, the initialization can begin. By connecting the SCL, SDA, and GND pins from the Aardvark I²C adapter to the J4 I²C header on the DS90UB934, the FPD-Link III signal chain can be set up. The writes to initialize the link are as follows:

- Deserializer slave I²C address 0x60 (8-bit) or 0x30 (7-bit):
  - Register 0x4C with 0x01: Enables write enable for Port 0
  - Register 0x58 with 0x58: I²C passthrough enabled
  - Register 0x5C with 0xB0: Sets serializer Alias to B0
  - Register 0x5D with 0x20: Sets slave ID for imager to 20
  - Register 0x65 with 0x20: Sets slave alias for imager to 20
  - Register 0x6D with 0x7E: Configures port to coax mode and FPD III to raw 12 HF mode
- Serializer slave I²C address 0xB0 (8-bit) or 0x58 (7-bit on Aardvark)
  - Register 0x0D with 0x99: Sets GPO0/1 on serializer, disables remote deserializer control

3.3 AR0140AT Initialization

Once the FPD-Link III setup is done, DevWare X can now be loaded to begin AR0140AT configuration and video transmission. When DevWare X is loaded, select the AR0140AT-REV2.xsdat sensor data file. After the sensor data file is loaded, at the startup wizard screen click *Finish* and then select *Parallel* (default: HDR 720p60fps). Next, click *Presets* at the top left and load the initialization file for the TIDA-01004.

Lastly, before streaming video, ensure that exposure and white balance are adjusted for best picture quality. This can be done in the *Control* menu at top left. Under the *Control* menu, go to the *Exposure* section and check the *Software Auto Exposure* box. In the *White Balance* section, check the box for *Software White Balance and Color Correction (CCM)* and the button *Automatic WB*. At this point, click play in DevWare to see video output from the TIDA-01004. Video quality can also be improved by focusing the lens.

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4 Testing and Results

4.1 Characterization Test Setup

For the following tests to verify power supply and I²C communication, the camera was connected to a multiple camera surround view system (see 图 8).

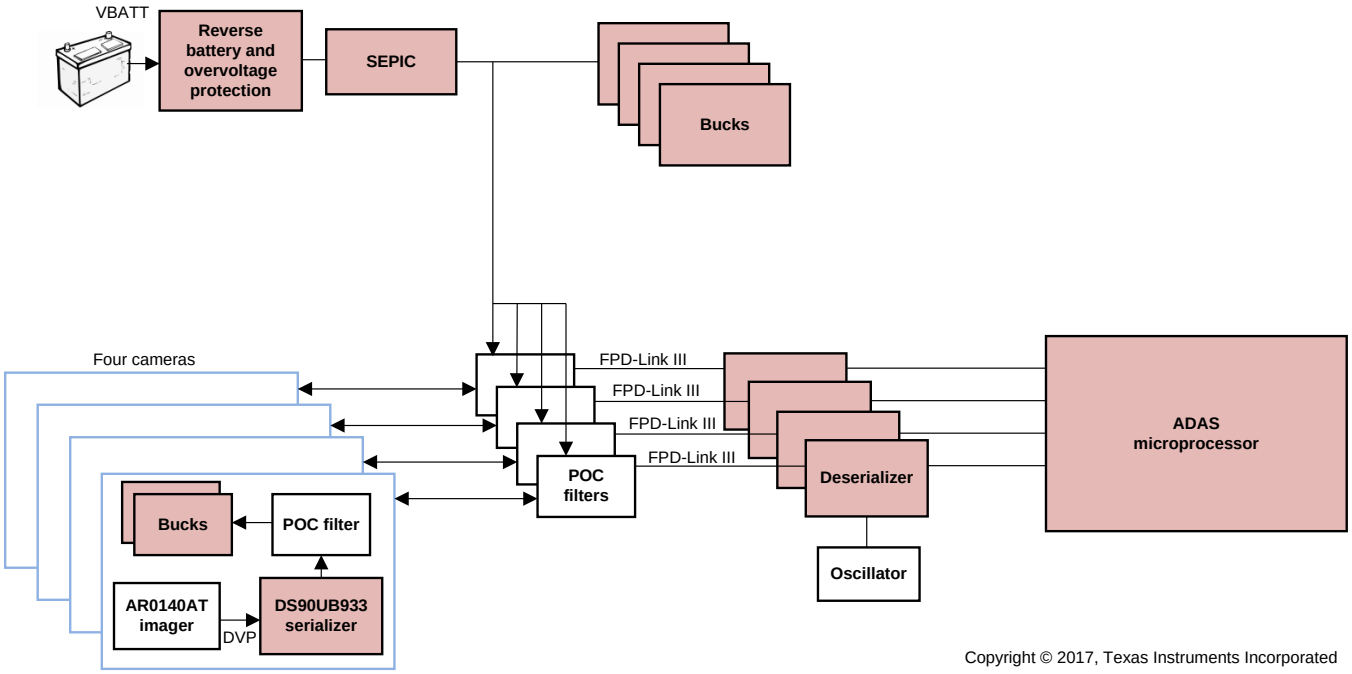

图 8. Simplified Surround View Block Diagram

4.1.1 Power Supplies Startup

图 9 shows the probe setup to measure the power sequence turn and ripple for the 12-V input from POC, 2.9-V input for imager, and 1.8-V input for the imager and serializer.

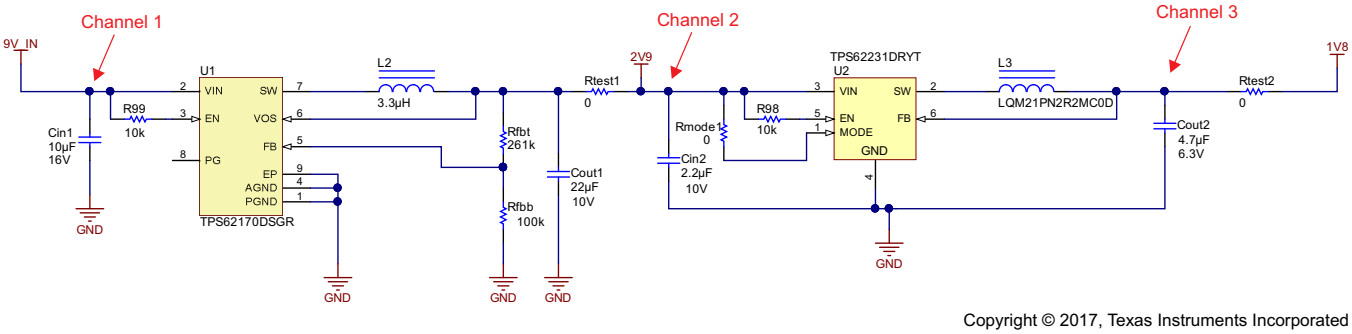

图 9. Measuring All Power Supplies

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4.1.2 Power Supply Startup—1.8-V Rail and Serializer PDB Setup

In order for the serializer to be initialized after the 1.8-V power supply comes up, the TPS3808G01 is configured as shown in 图 10 to ensure PDB pin comes up with a delay.

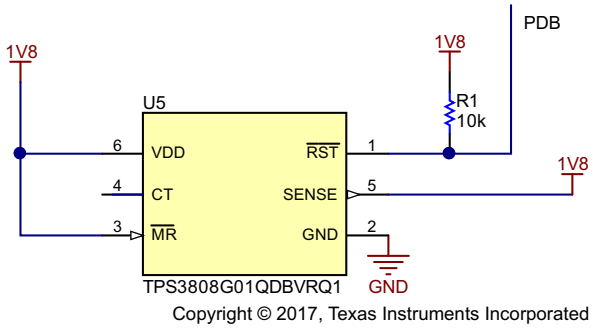

图 10. PDB Startup Delay Circuitry

4.1.3 Setup for Verifying I²C Communications

For this test, a logic analyzer with I²C decode is used to monitor the I²C traffic on the buses. The two buses of interest are:

1. I²C connection from serializer to imager (shown as I2C_camera)
2. I²C connection from microprocessor to deserializer (shown as I2C_uC)

Make connections to both the clock and data lines of each bus as shown in 图 11.

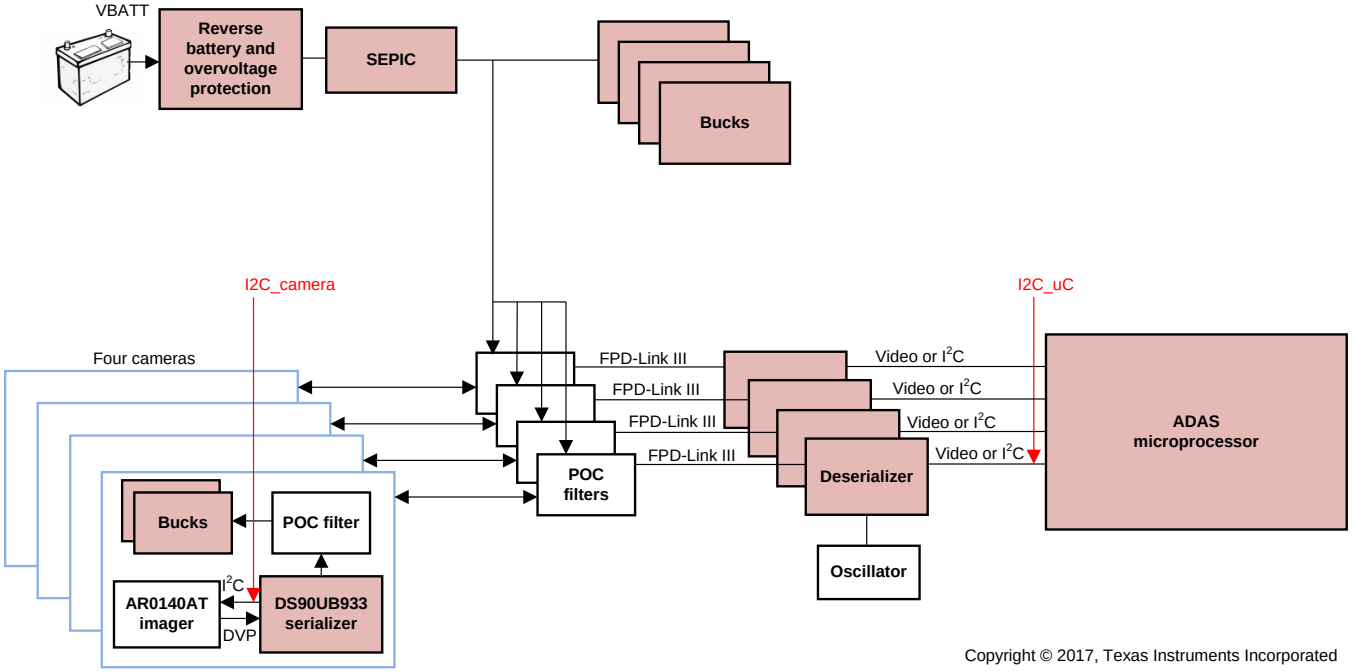

图 11. Setup for Monitoring I²C Transactions

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4.2 Characterization Test Data

The following sections show the test data from verifying the functionality of the camera design.

4.2.1 Power Supplies Startup

Power startup behavior for the input power supply, 2.8-V, and 1.8-V system supplies are shown in 图 12. The startup sequence shows that when the 12-V input reaches minimum input turnon voltage for the TPS62170, the 2.8-V starts turning on. The same behavior is exhibited for the 1.8-V input, which starts turning on when 2.8 V has reached a high enough voltage to pull up the 1.8-V enable.

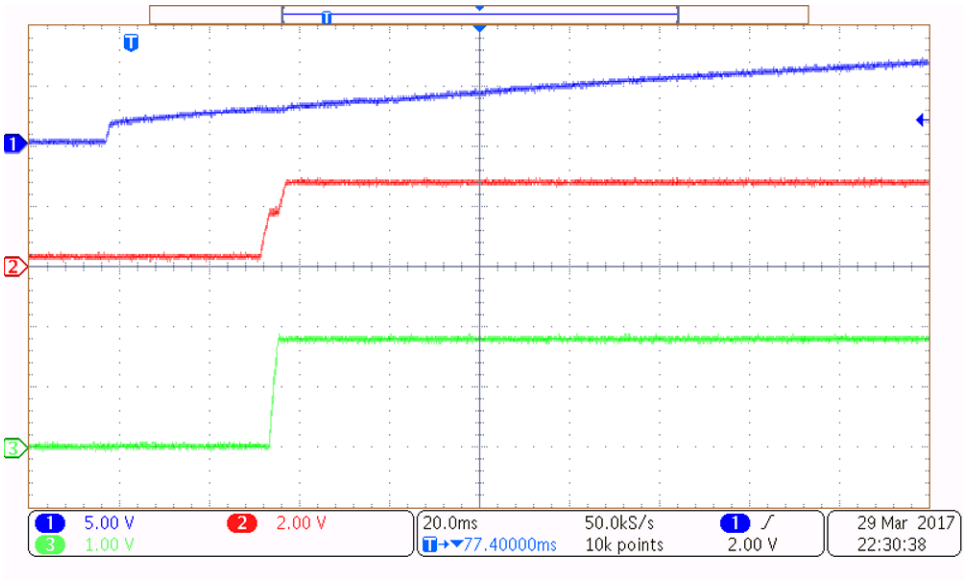

图 12. Power Supplies Startup

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4.2.2 Power Supply Startup—1.8-V Rail and PDB

The only startup requirement is that the PDB pin of the serializer remains low until the supply rails of the system stabilize at their final voltages. The power supply startup is shown in 图 13.

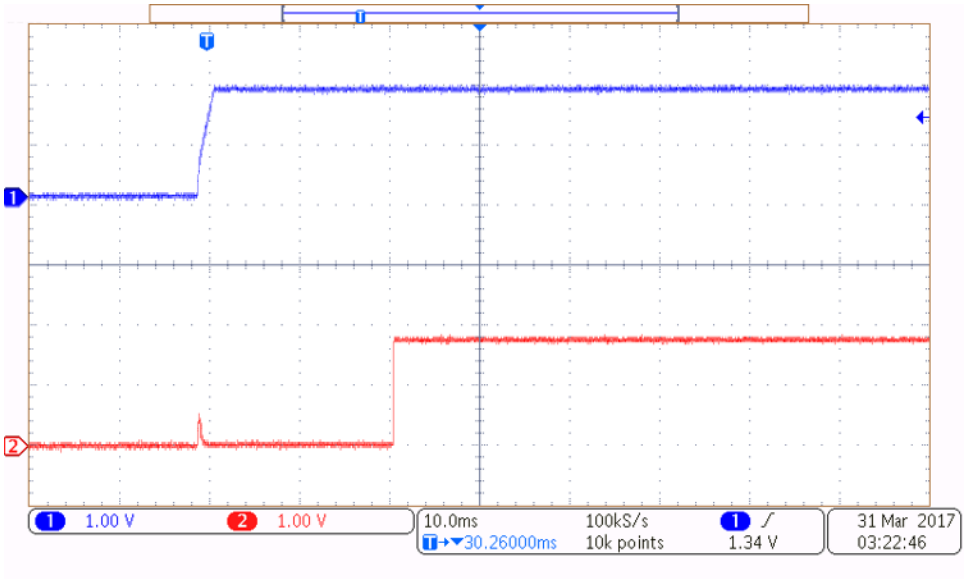

图 **13. Serializer Power-Up Sequence**

注: Channel 1 (blue) 1.8 V; Channel 2 (red) PDB

图 13 shows that PDB comes up roughly 20 ms after the 1.8-V rail has stabilized. This 20-ms delay is due to having the CT pin of the TPS3808G18 floating. If less delay is needed for the serializer to come out of reset after 1.8 V has reached regulation, the TPS3808 allows for adjustable delay with a capacitor tied from the CT pin to ground.

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4.2.3 I²C Communications

Now that the power supplies are up and running, the I²C communication between the processor and AR0140AT over the FPD-Link III backchannel can be confirmed. 图 14 shows the initial I²C communication from the Demo3 board to the AR0140AT on the TIDA-01004 when the sensor data file is loaded. This communication occurs after all the deserializer and serializer initialization is complete and the Demo3 microprocessor writes to the AR0140AT to get the imager ready for video output.

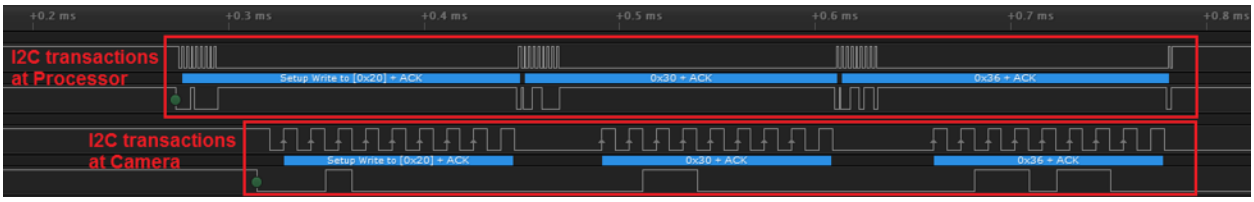

图 **14. I²C Transactions**

The top box labeled "I²C transactions at Processor" is measured at the deserializer side between the host microprocessor and the DS90UB934. The write is to the imager, which is at slave alias address 0x20. The write to the imager is for its register 0x30 with data 0x36.

The bottom box labeled "I²C transactions at Camera" is measured on the TIDA-01004 on the SCL and SDA lines connecting the DS90UB933 and the AR0140AT. This box shows that the write measured at the deserializer is writing across the FPD-Link III connection and being successfully written to the imager on the camera module.

By acknowledging the I²C write, the imager has confirmed that it is present and alive. Reading the status registers can confirm the status of the imager as well as verify that the correct imager was installed during assembly.

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5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01004.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01004.

5.3 PCB Layout Recommendations

5.3.1 Switching DC-DC Converters

During part placement and routing, it is helpful to always consider the path current will be taking through the circuit. The green line in 图 15 shows the current path from the coax in through the POC filter, inductor L5, and capacitors C1 and C2, and then out to the ferrite bead, L1, input capacitor, Cin1, to U1, or the TPS62170-Q1. The yellow line follows the 2.8-V output of the switcher to the output inductor L2 and output capacitor Cout1. Any return currents from the input capacitor Cin1 or the output capacitor Cout1 are joined together at the top left of U1 before they are connected to the ground plane. This is shown inside the blue lines. This will reduce the amount of return currents, and thereby, voltage gradients in the ground plane. This may not be noticeable in the performance of the converter, but it will reduce its coupled noise into other devices.

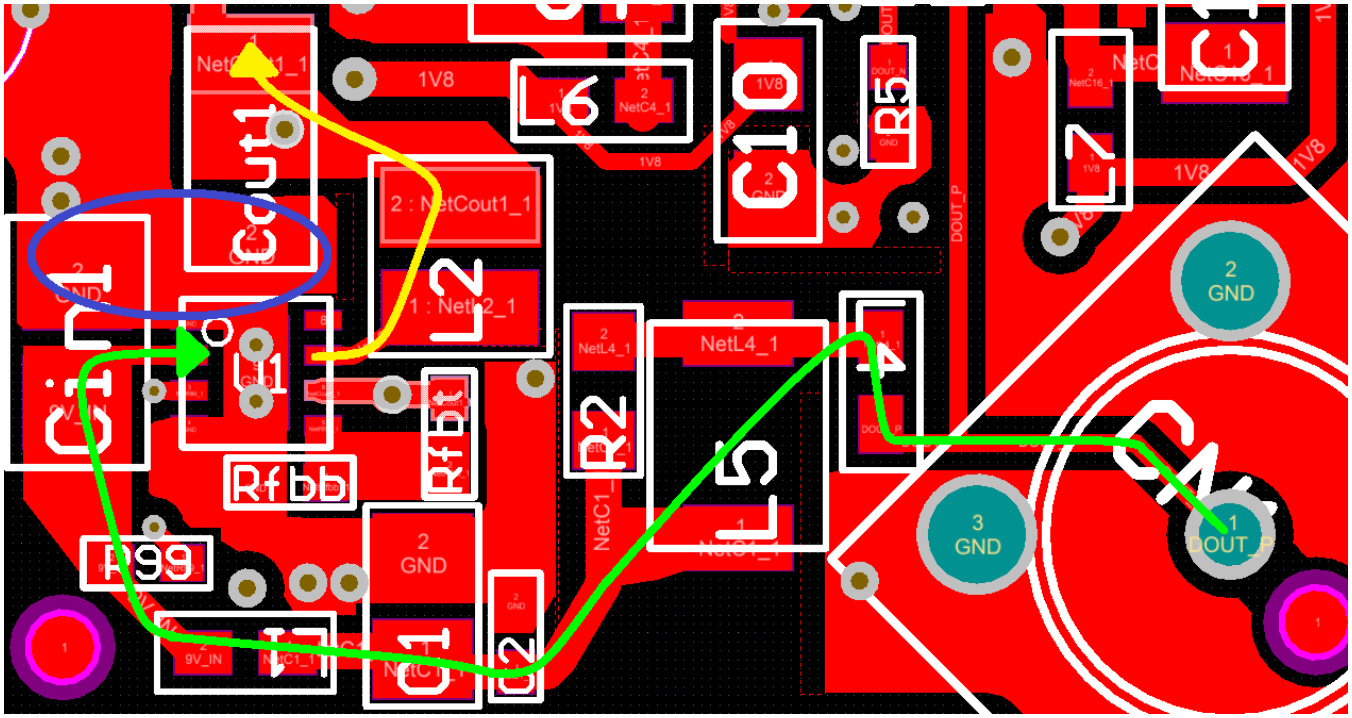

图 15. Routing FB Traces Around SW Nodes

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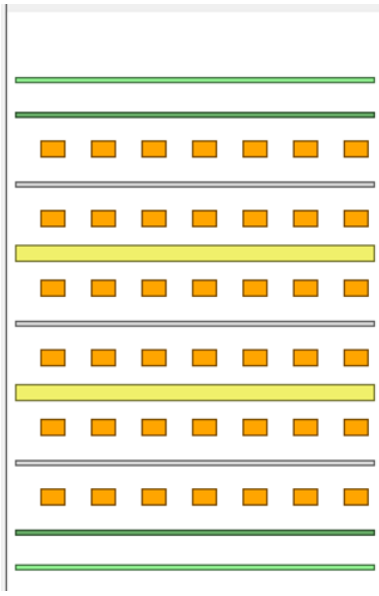
5.3.2 PCB Layer Stackup Recommendations

The following are PCB layer stackup recommendations. Because automotive is the target space, there are a few extra measures and considerations to take, especially when dealing with high-speed signals and small PCBs:

- Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines
- If using a four-layer board, layer 2 must be a ground plane. Because most of the components and switching currents are on the top layer, this reduces the inductive effect of the vias when currents are returned through the plane.
- An additional two layers were used in this board to simplify BGA fan out and routing. 图 16 shows the stackup used in this board:



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant
Top Overlay	Overlay				
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Layer 1 - Top Lay...	Signal	Copper	1.4		
Dielectric 1	Dielectric	Prepreg	12.6	370HR	4.2
Layer 2 - GND	Signal	Copper	1.4		
Dielectric 2	Dielectric	Core	8	370HR	4.2
Layer 3 - Signal	Signal	Copper	1.417		
Dielectric 3	Dielectric	Prepreg	16.6	370HR	4.2
Layer 4 - Signal	Signal	Copper	1.417		
Dielectric 4	Dielectric	Core	8	370HR	4.2
Layer 5 - PWR	Signal	Copper	1.4		
Dielectric 5	Dielectric	Prepreg	12.6	370HR	4.2
Layer 6 - Bottom...	Signal	Copper	1.4		
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Bottom Overlay	Overlay				

图 16. Layer Stackup

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5.3.3 Serializer Layout Recommendations

Decoupling capacitors need to be located very close to the supply pin on the serializer. Again, this requires that the user consider the path of the supply current and the return current. Keeping the loop area of this connection small reduces the parasitic inductance associated with the connection of the capacitor. Due to space constraints, ideal placement is not always possible. Smaller value capacitors that provide higher frequency decoupling must be placed closest to the device.

图 17 shows the supply current from C18 in yellow. The green line is the return path. The cross sectional area of this loop is very small. A similar sketch for C16 or C17 would show a larger loop.

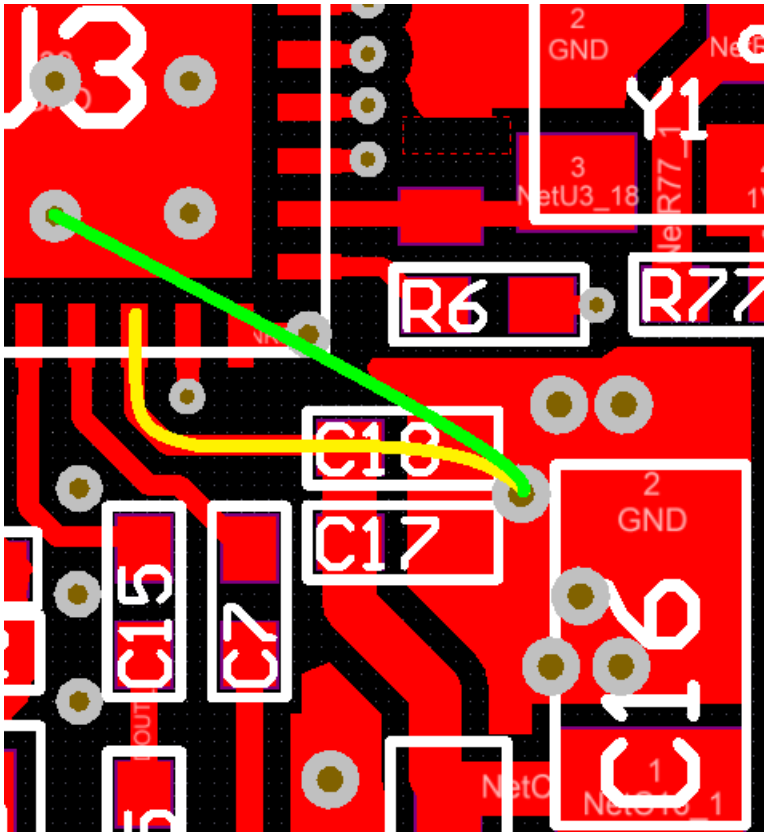

图 **17. Decoupling Current Loop**

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For this application, a single-ended impedance of 50 Ω is required for the coax interconnect. Whenever possible, this connection must also be kept short. The routing of the high-speed serial line is shown in 图 18. It is highlighted by the yellow line. The total length of the yellow line is about ½ inch.

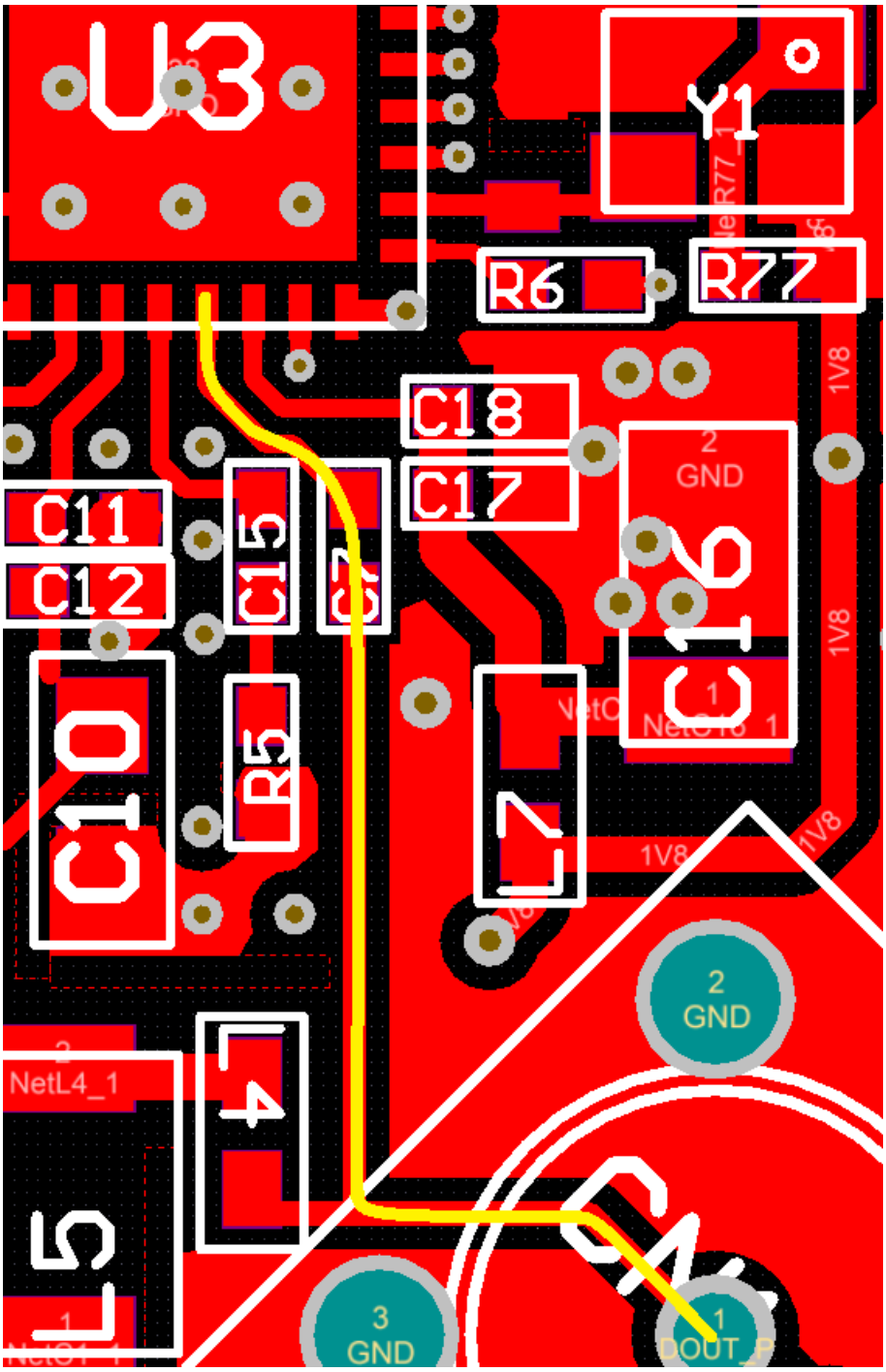

图 **18. High-Speed Serial Trace**

5.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-01004.

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5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01004.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01004.

6 Related Documentation

1. Texas Instruments, *DS90UB933-Q1 FPD-Link III Serializer for 1-MP/60-fps Cameras 10/12 Bits,100 MHz*, DS90UB933-Q1 Datasheet (SNLS546)
2. Texas Instruments, *TPS6217x-Q1 3-V to17-V 0.5-A Step-Down Converters with DCS-Control™*, TPS62170-Q1 Datasheet (SLVSCK7)
3. Texas Instruments, *3-MHz Ultrasmall Stepdown Converter in 1x1.5 SON Package*, TPS62231-Q1 Datasheet (SLVSBV0)
4. Texas Instruments, *Sending Power Over Coax in DS90UB913A Designs*, Application Report (SNLA224)
5. Texas Instruments, *Cable Requirements for the DS90UB913A and DS90UB914A*, Application Report (SNLA229)
6. Texas Instruments, *Optimizing the TPS62130/40/50/60/70 Output Filter*, Application Report (SLVA463)

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