

AFE5832 32-Channel Analog Front-End Evaluation Module (EVM Rev. A)

This user's guide gives a general overview of the AFE5832 evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module. This manual is applicable to the AFE5832 analog front-end, and to the Rev. A version of the EVM hardware. The AFE5832 EVM provides a platform for evaluating the AFE under various signal, clock, reference, and ADC output formats. In addition, the EVM supports the testing of the low-voltage differential signaling (LVDS) interface using the TSW1400EVM capture card.

This user's guide refers to software AFE5832 GUI v.1.0.0 or higher, and *High-Speed Data Converter Pro* (HSDC Pro) Software v.4.7 and requires Microsoft Windows 7[®] or Windows 10[®] to function.

For any further questions regarding the EVM, GUI or device, contact TI support.

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1 EVM Hardware Overview



Figure 1. AFE5832 EVM Hardware Overview

The EVM received should resemble Figure 1. For more hardware details and the default jumper map, see Appendix C.



- The AFE5832 EVM kit contains the following items:
- 1. AFE5832 EVM
- 2. 1 mini-USB cable
- 3. Power cable with barrel connector



Figure 2. Provided Power Cable for J1 Connector

2 GUI Software Installation

The AFE5832 EVM and the TSW capture card EVM have individual software and both require software installations. Ensure that no USB connections are made to the EVMs until after the installations are complete. This user's guide refers to software AFE5832 GUI v.1.0.0, and HSDC Pro Software v.4.7.

See the *HSDCPro Installation* section for information on the installation of the TSW EVM Software GUI (HSDC Pro). For information on the installation of the AFE5832 EVM Software GUI, see the *AFE5832 EVM GUI Installation* section.



3 Quick Views of Evaluation Setups for LVDS Interface

The AFE5832 EVM is tested using the TSW1400EVM for LVDS data interface.

3.1 Equipment Setup Overview

As shown in Figure 3, mating the AFE5832 EVM with a TSW EVM allows for testing using the data interface.





TSW Capture Card EVM: The TSW1400 EVM is required for capturing data from the AFE5832 EVM and its analysis using the graphical user interface (GUI), called High Speed Data Converter Pro (HSDC Pro).

For more information on the TSW1400EVM, see: TSW1400EVM.

Power Supply: A barrel connector power cable is provided with the EVM and is connected at J61, but does not support the –5 V needed for the CW mode. This requires an additional cable, not provided.

This 5-V power supply must be able to source up to 2 A, and –5-V supply must provide up to 1 A. The –5-V supply is used for the negative supply of amplifiers in the CW output external circuitry. The TSW1400 EVM is powered through a power cable similar to Figure 2 that is provided with its own EVM kit.

USB Interface to PC: The USB connections from the AFE5832 EVM and TSW EVM to the PC are used for communication from the GUIs to the boards. USB 2.0 or 3.0 ports are both acceptable.



Equipment: Signal generators (with low-phase noise) must be used as source of the input signal for optimal performance. An onboard crystal oscillator option is provided so that an external clock source is not needed for basic capture. Additionally, for best performance a band-pass filter (BPF) is recommended on the analog input signal to attenuate the harmonics and noise from the signal. For coherent sampling or custom sample rate, an external clock is provided to J39 or J56 (GUI configuration is required for the external clock configuration). For more information on clock configuration, see Section C.1.3.



4 Testing the EVM Data Capture with LVDS Interface

This section outlines (1) the external connections required to test the AFE5832 EVM using the LVDS interface, (2) how to setup the GUIs for testing, and (3) how to capture an analog input signal.

4.1 EVM Hardware Setup

Make the connections shown in Figure 4 for proper hardware setup.



Figure 4. TSW1400EVM and AFE5832 EVM Hardware Setup for LVDS Capture

- 1. **Board Mating:** For LVDS data, mate the TSW1400 EVM at connector **J3** to the AFE5832 EVM at connector **J48** through the high-speed ADC interface connector.
- Power Supply: Connect a 5-V (2-A) power supply using the provided power cable to J12 (+5V_IN) of the TSW1400 EVM or J11 (+5V_IN) of the TSW14J50 EVM. See the TSW manual for more information, if needed.

Next, connect a 5-V (2-A) power supply using the provided power cable to **J61** of the AFE5832 EVM. **Connect the white-striped side of this cable to the positive side of the 5-V power supply.** Optionally, connect a –5-V (1-A) supply at **J63** or TP54 if using the CW circuit. No cable is provided for this.

Turn on the TSW1400 at the SW7 switch.

USB: After installing the GUIs as shown in Appendix A, connect the USB cable from the PC to J65 (USB) located on the top side of the AFE5832 EVM. Connect the USB cable from PC to J5 (USB_IF) of the TSW1400 EVM.

NOTE: TI recommends that the PC USB port be able to support USB2.0. If unsure, always choose the USB ports at the back of the PC chassis over ones located on the front or sides.

- 4. Equipment: Connect a sine wave generator to SMA J1, INP1. Set the frequency to 5 MHz and the amplitude to -20 dBm. For best performance, a 5-MHz band-pass filter (BPF) is recommended on the analog input signal to attenuate the harmonics and noise from the signal.
- 5. CPLD Switches: Ensure that all 4 switches in S5 are in the 'off' position. LEDs D5–D8 should be lit up.



S4 should be 'off' immediately after powering up the board for LVDS capture, but can be manipulated for other modes. For more information on the Complex Programmable Logic Device (CPLD), refer to Section C.1.4.



4.2 Capturing an Analog Input Signal With the LVDS Interface

This section describes the software setup for capturing an analog input using the AFE5832 EVM. If there is any issue with a data capture, refer to the troubleshooting section.

Data capture is confirmed by using only the *Quick Setup* page of the AFE5832 GUI. Assuming the hardware is connected correctly as in Section 4.1, follow these steps to acquire data:

4.2.1 HSDC Pro Actions

- 1. Connect both EVMs to the PC using two USB cables as instructed in Section 4.1.
- 2. Open the HSDC Pro GUI using *Run as Administrator*. Do not open the AFE5832 GUI before this step because it opens automatically. If it is already open, close it.
- 3. If the TSW Hardware is already connected to the USB, then a pop-up window should appear to connect the HSDC Pro GUI to the EVM Hardware.

🚺 Select Board		\times
Select The Serial number	of the Device	
	Serial Numbers	^
	TIYQPZG8-TSW1400	
		_
		_
		×
	Select/Enter IP Address - Port Number	
Connect to KCU105	~	
	Cancel	
V		

Figure 5. Connect to TSW EVM (TSW1400 Shown)

- 4. A pop-up window prompts the user to choose a firmware to download to the TSW EVM FPGA.
- 5. Select firmware: In the upper left-hand corner "Select ADC" box, type the name of your device and the drop-down list will automatically filter based on your input. Then, from the drop-down, choose your desired format. Be sure to choose the correct device to match the AFE5832 EVM hardware or the AFE5832 GUI will show an error when launching.

TEXAS INSTRUME	NTS
AFE5832	V
Capture	
Test Selection	
Single Tone	-

Figure 6. Choose Firmware

- 6. When prompted to update the firmware, click the Yes button.
- 7. The firmware begins downloading to the FPGA on the TSW EVM.
- 8. When the firmware has finished downloading, several Green LEDs are lit on the TSW EVM. For the TSW1400, D5 (USER_LED3) is usually off when the EVM is not configured, and D6 is off.





Figure 7. TSW1400 EVM LEDs Turn On After Firmware Download

9. The AFE5832 EVM GUI opens automatically. Wait until this is finished before continuing. If any errors arise at this time, contact TI support.



Figure 8. AFE5832 GUI Launches

4.2.2 AFE5832 GUI Actions

1. Verify the clock configuration by matching J42, J40, and J54 to Figure 9. Provide a 160-MHz, +13-dBm clock to J56.



Figure 9. Clock Configuration on AFE EVM for LVDS Capture

- 2. Press the DUT RESET button on the AFE5832 GUI.
- 3. Press the *Initialize Device* button on the AFE5832 EVM GUI (Figure 10). These buttons are located close to the upper left-hand corner of the GUI window.
 - Alternatively, there is an option to use the hardware reset. Press the AFE_RST button on the AFE EVM, located above the AFE device (S1), as shown in Figure 11. Hold for 1 second. Then, press the *Initialize Device* button on the AFE5832 EVM GUI.



Figure 10. Software Reset and Initialize Buttons on AFE5832 EVM GUI



Figure 11. AFE_RST Hardware Reset Button



- 4. Ensure there is no SMA cable connected to J37 TX_Trig on the AFE5832EVM.
- 5. Turn switch 4 contained in **S5** on the AFE EVM 'off' for LVDS only. The red LED, D8 should light up. For more information on the *Complex Programmable Logic Device* (CPLD), refer to Section C.1.4.
- 6. Choose the Data Formats and the Analog Configuration for each category as shown in Figure 12:
 - OUTPUT FORMAT: Select 'LVDS: 12x 12b'
 - ADC FORMAT: Select 'Analog Input'
 - VCA GAIN: Select 'Mid Gain'
 - DTGC Modes: Select 'Programmable Fixed-Gain Mode'

NOTE: Ensure the right CPLD switches are configured on S5 as detailed for each capture mode.

ap Configuration related Parameters 20MHz get Frequency 6MHz
related Parameters 20MHz get Frequency 6MHz
20MHz get Frequency 5MHz
get Frequency 5MHz
gorrioquono)
on of Coherent Frequencies 📃
tus
0.00
Status
LVDS interface is enabled
LVDS interface is enabled VTE 12x
LVDS interface is enabled TE 12x 12 bit
LVDS interface is enabled TE 12x 12 bit Analog input
LVDS interface is enabled TE 12x 12 bit Analog input
LVDS interface is enabled ATE 12x 12 bit Analog input
LVDS Interface is enabled TVDS Interface is enabled NTE 12x 12 bit Analog Input

Figure 12. AFE5832 EVM GUI Data Format and Analog Configuration (LVDS)

7. At this point, D5 on the TSW1400 EVM should turn on. If this is not the case, consult Appendix G. There is most likely an ADC clock issue.



Figure 13. LED D5 on the TSW1400 EVM Turns On When ADC is Ready

8. Return to HSDC Pro, and press the *Capture* button in the upper left-hand corner (as shown in Figure 14). A capture similar to that shown in Figure 14 appears for a successful capture. The quality of the output spectrum depends heavily on the coherency and the purity of the input signal and clock.



Figure 14. Analog Input Capture for LVDS

5 Testing the EVM in Digital Time Gain Compensation (DTGC) Mode

Use the following steps to test the EVM in DTGC mode:

- a. Input a 5-MHz, -20-dBm signal to any SMA input on the AFE EVM. Connect a 5-MHz filter to the input signal. Connect a single SMA-SMA cable from J11 (TSW EVM) to J37 (AFE EVM).
- b. Change the jumper configurations as outlined in Section C.1.3 and apply a 160-MHz, 10-dBm external LMK input clock to J56 or clock at 4× the desired ADC sample rate.
- c. Set the switches of the AFE5832 EVM at S5 for 'Up-Down Ramp Mode' as Figure 15 illustrates. LEDs D6-D8 should be lit and LED D5 should be off.



Figure 15. DTGC Mode Test: AFE5832 EVM Switches (S5)

- d. Choose AFE5832.ini as firmware on HSDC Pro.
- e. Change the DTGC Mode on the AFE5832 EVM GUI to 'Up-Down Ramp Mode' and configure the other formats as shown in Figure 16:

act octup	₩ VCA		ADC	Register Map Confi	guration
Reset and Initialize the dev.	ice			HSDC Pro related	d Parameters
DUT Reset Initialize D	Device			fsamp	20MHz
.Choose Data Format				ADC Input Target Frequ	ency 5MHz
OUTPUT FORMAT	ADC FORMAT	*		Auto Calculation of Coh	erent Frequencies 📰
Z LVDS: 10× 10b Z LVDS: 12× 12b ≡	 Ramp Test Pattern Analog Input 				
UVDS: 14x 12b					
CW: 16x 1.953MHz +		+			
CW: 16x 1.953MHz	ion	×			
Choose Analog Configurati	ON DTGC FIXED-GAIN	*			
Choose Analog Configurati	DTGC FIXED-GAIN	*			
CW: 16x 1.953MHz	ON DTGC FDXED-GAIN Max Gain Min Gain	*		Device Status	
CW: 16x 1353MHz	ON DTGC FIXED-GAIN Max Gain Min Gain Win Gain	*		Device Status Parameters	Status
CW: 16x 1.953MHz Choose Analog Configurati DIGC MODES External Non-Uniform Mode VDp-Down Ramp Mode Programmable Fixed-Gain Mode Internal Non-Uniform Mode	DTGC FDKED-GAIN DTGC FDKED-GAIN Max Gain Min Gain Min Gain Min Gain			Device Status Parameters DIS LVDS	Status LVDS interface is enabled
CW: 16: 1353MHz Choose Analog Configurati DTGC MODES External Non-Uniform Mode Programmable Fixed-Gain Mode Internal Non-Uniform Mode	DTGC FIXED-GAIN Max Gain Min Gain V Mid Gain	*		Device Status Parameters DIS_LVDS SER. DATA. RATE	Status LVDS Interface Is enabled 12x
CW: 16x 1353MHz Choose Analog Configurati DTGC MODES External Non-Uniform Mode Up-Down Ramp Mode Programmable Fixed-Gain Mode Internal Non-Uniform Mode	DTGC FIXED-GAIN Max Gain Min Gain Min Gain	*		Device Status Parameters DIS_LVDS SER_DATA_RATE ADC_RES	Status LVDS Interface is enabled 12x 12 bit
CW: 16x 1353MHz Choose Analog Configurati DTGC MODES External Non-Uniform Mode Programmable Fixed-Gain Mode Internal Non-Uniform Mode	OT DTGC FIXED-GAIN Max Gain Min Gain I Min Gain	*		Device Status Parameters DIS_VOS SER_DATA_RATE ADC_RES PAT_MODES	Status LVDS Interface is enabled 12x 12 bit Analog input
CW: 16: 1353MHz Choose Analog Configurati DTGC MODES External Non-Uniform Mode Programmable Fixed-Gain Mode Internal Non-Uniform Mode	OT DTGC FIXED-GAIN Max Gain Min Gain ✓ Mid Gain	*		Device Status Parameters DIS_LVDS SER_DATA_RATE ADC_RES PAT_MODES	Status LVDS interface is enabled 12x 12 bit 12 bit Analog input
CW: 16x 1.353MHz Choose Analog Configurati DIGC MODES External Non-Uniform Mode Programmable Fixed-Gain Mode Internal Non-Uniform Mode	ON DTGC FIXED-GAIN Max Gain Min Gain V Mid Gain	•		Device Status Parameters DIS_LVDS SER_DATA_RATE ADC_RES PAT_MODES	Status LVDS Interface is enabled 12x 12 bit Analog Input
CW: 16x 1.953MHz Choose Analog Configurati Choose Analog Configuration Choose Analog Configu	OT DTGC FIXED-GAIN Max Gain Min Gain I Min Gain	*		Device Status Parameters DIS_LVDS SER_DATA_PATE ADC_RES PAT_MODES	Status LVDS interface is enabled 12x 12 bit Analog Input
CW: 16x 1.353MHz Choose Analog Configurati DTGC MODES External Non-Uniform Mode Up=Down Ramp Mode Programmable Fixed-Gain Mode Internal Non-Uniform Mode	ON DTGC FIXED-GAIN Max Gain Min Gain ✓ Mid Gain			Device Status Parameters DIS_LVDS SER_DATA_RATE ADC_RES PAT_MODES	Status LVDS interface is enabled 12x 12 bit Analog input

Figure 16. DTGC Mode Test: Change GUI Configuration

f. In HSDC Pro, navigate to the *Trigger Option* menu. Choose "Trigger mode enable" and "Arm on next capture button press" as shown in Figure 17.



Testing the EVM in Digital Time Gain Compensation (DTGC) Mode

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Figure 17. DTGC Mode Test: Trigger Options

g. Change the ADC Output Data Rate to '20M' and the ADC Input Target Frequency to '5M'. Set the view display to 'Codes'.



Figure 18. DTGC Mode Test: HSDC Pro Test Parameter Settings

- h. Press the Capture button on HSDC Pro.
- i. The Up-Down Ramp DTGC waveform should appear similar to Figure 19.



Figure 19. DTGC Mode Test: Waveform



6 Using the EVM in CW Mode

Demonstrating the CW mixer in the AFE is done by following these steps:

- 1. In the AFE5832 GUI, reset and initialize the device by referring to Figure 10 and Figure 11. Remember to connect a –5-V and a 5-V source to the device.
- 2. Connect a sine wave generator to any SMA channel. Set the frequency to 1.963125 MHz and the amplitude to –23 dBm.
- 3. Provide a 125-MHz, +10-dBm clock input to J56 of the AFE EVM (LMK external clock). Refer to Section C.1.3 for jumper configurations.
- 4. Turn *Switch 4* contained in **S5** on the AFE EVM to 'on'. The red LED, D8 should not light up. For more information on the CPLD, refer to Section C.1.4.
- 5. Connect two cables to an oscilloscope with timebase of 40 μs and 500 mV / div. Input resistance should be 1 M Ω on each scope channel. DC couple the oscilloscope.
- 6. Connect those two cables to SMAs, J66 and J68 on the AFE EVM.
- 7. Choose the following data format on the AFE5832 EVM GUI:

HSDC Pro related Parameters fsamp 20MHz ADC Input Target Frequency 5MHz Auto Calculation of Coherent Frequencies
fsamp 20MHz ADC Input Target Frequency 5MHz Auto Calculation of Coherent Frequencies
ADC Input Target Frequency 5MHz Auto Calculation of Coherent Frequencies
Auto Calculation of Coherent Frequencies
*
*
Device Status
Parameters Status
, a diloto
DIS LVDS LVDS LVDS interface is enabled
DIS_LVDS LVDS interface is enabled SER_DATA_RATE 16x
DIS_LVDS LVDS Interface is enabled SER_DATA_RATE 16x ADC_RES 12 bit
DIS_LVDS LVDS interface is enabled SER_DATA_RATE 16x ADC_RES 12 bit PAT_MODES Analog Input
DIS_LVDS LVDS Interface is enabled SRE_DATA_PATE 15x ADC_RES 12 bit PAT_MODES Analog input
DIS_LVDS LVDS Interface is enabled SRE_DATA_RATE 16x ADC_RES 12 bit PAT_MODES Analog input
DIS_LVDS LVDS Interface is enabled SIRE_DATA_FATE 15k ADC_RES 12 bit PAT_MODES Analog Input
DIS_LVDS LVDS Interface is enabled SRE_DATA_PATE 15x ADC_RES 12 bit PAT_MODES Analog Input
DIS_LVDS LVDS Interface is en SER_DAT_RATE 16x ADC_RES 12 bit PAT_MODES Analog Input
DIS LVDS LVDS inte

Figure 20. CW Mode Preset

- 8. Trigger the oscilloscope on either channel.
- 9. The oscilloscope displays the frequency I and Q signals at 10 kHz as shown in Figure 21. The amplitude should be around 1.5 Vpp ±300 mVpp, though this amplitude may change. The frequency should be 10 kHz and the I and Q signals should be 90 degrees out of phase.





Figure 21. CW Output



Appendix A SLOU489–August 2017

Software Installation

Section A.1 provides detailed procedures for installing High Speed Data Converter Pro (HSDC Pro), the software GUI used to control a suite of FPGA capture solutions including the TSW1400. Section A.2 provides details for installing the AFE5832 EVM GUI.

A.1 High Speed Data Converter Pro (HSDC Pro) GUI Installation

Download HSDC Pro v.4.7 from the mySecureSoftware folder at https://www.ti.com/securesoftware/docs/securesoftwarehome.tsp.

- 1. Unzip the saved file and run the installer executable (*Run as Administrator*) to obtain the menu shown in Figure 22.
- 2. Click the Next button.



Figure 22. HSDC Pro Install (Begin)



High Speed Data Converter Pro (HSDC Pro) GUI Installation

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3. Read the License Agreement from Texas Instruments and select *I accept the License Agreement*, then press the *Next* button as shown in Figure 23.

🚺 Setup		_		<	
License Agreement			1	01010	
Please read the following License Agreement. You must accept the terms of this agreement before continuing with the installation.					
IMPORTANT -	READ BI	EFORE C	OPYING,	^	
Do not copy install c	listribute put	olic display	or use the		
Materials provided	under this	license a	agreement		
("Agreement"), until vo	ou have care	fully read the	e following	~	
Do you accept 💿 l accep	t the agreeme	nt			
this license? O I do no	ot accept the ag	greement			
instandunuer	< Back	Next >	Cancel		

Figure 23. HSDC Pro Install (TI License Agreement)

4. Read the License Agreement from Texas Instruments and select *I accept the agreement*, then press the *Next* button as shown in Figure 24.

🚺 Setup		—		×
License Agreement				101010
Please read the following Li terms of this agreement be	cense Agree fore continu	ement. You mi ing with the i	ust accept nstallatior	t the n.
Source and Binary A	Code Inte greement	ernal Use Li	cense	<
<				>
Do you accept ® I accept this license? O I do not a	he agreeme accept the ag	nt greement		
	< Back	Next >	Cano	

Figure 24. HSDC Pro Install (TI License Agreement)



5. Allow the installation to be placed in the default directory by clicking Next, as in Figure 25.

🚺 Setup		—	
Installation Directory			101010
Please specify the directo will be installed.	ory where High	n Speed Data C	onverter Pro
Installation Directory	Program Files	(x86)\Texas Ins	truments\Higł
InstallBuilder			
	< Back	Next >	Cancel

Figure 25. HSDC Pro Install (Install Directory)

6. Click *Next* to begin the installation, as in Figure 26.

🚺 Setup	_		Х
Ready to Install			101010
Setup is now ready to begin installing Pro on your computer.	J High Speed Da	ıta Conv	erter
InstallBuilder	Next >	Car	ncel

Figure 26. HSDC Pro Install (Installation Ready)

7. The Cypress Driver begins installing as shown in Figure 27.

🚺 Setup		_	\square ×	
Installing			101010	Ì
Please wait while Setup i your computer.	nstalls High Sp	eed Data Conv	verter Pro on	
	Installing			
Unpacking C:\Users\a0[.]ypress Driver	\wxp\x86\Wdf0	Colnstaller010	
InstallBuilder	< Back	Next >	Cancel	

Figure 27. HSDC Pro Install (Cypress Driver Install)

8. Click *Finish* to continue installation, as shown in Figure 28.

Device Driver Installation Wizar	rd
	Welcome to the Device Driver Installation Wizard! This wizard helps you install the software drivers that some computers devices need in order to work.
	< Back Next > Cancel

Figure 28. HSDC Pro Install (Continue Installation)



9. Click Finish to continue installation, as shown in Figure 29.

Device Driver Installation Wiza	ď	
	Completing the De Installation Wizard	vice Driver 1
	The drivers were successfully in:	stalled on this computer.
	You can now connect your devi came with instructions, please re	ce to this computer. If your device ad them first.
	Driver Name	Status
	✓ Cypress (CYUSB3) USB	Ready to use
	< Back	Finish Cancel

Figure 29. HSDC Pro Install (Continue Driver Installation)

10. Finish HSDC Pro installation by choosing the appropriate installation options and pressing *Finish*, as in Figure 30.



Figure 30. HSDC Pro Install (Finish Installation)

A.2 AFE5832 GUI Installation

Download the AFE5832 EVM GUI from the mySecureSoftware folder at https://www.ti.com/securesoftware/docs/securesoftwarehome.tsp.

1. Unzip the saved file and run the installer executable as administrator by right clicking on the file and selecting *Run as Administrator*. Press the *Next* button once the graphic in Figure 31 appears.



Figure 31. AFE5832 GUI Install (Begin Installation)

2. Read the Texas Instruments License Agreement and select *I accept the agreement* followed by the *Next* button, as in Figure 32.



octop	
License Agreement	
Please read the following Lic agreement before continuin	cense Agreement. You must accept the terms of this ng with the installation.
Source and Binary Code IMPORTANT PLEASE CARE WHICH IS LEGALLY BINDI WHETHER YOU ACCEPT ANI READ AND AGREE UNLESS: YOUR OWN BENEFIT AND F	EFULLY READ THE FOLLOWING LICENSE AGREEMENT, ING. AFTER YOU READ IT, YOU WILL BE ASKED D AGREE TO ITS TERMS. DO NOT CLICK I HAVE : (1) YOU WILL USE THE LICENSED MATERIALS FOR PERSONALLY ACCEPT, AGREE TO AND INTEND TO BE
BOUND BY THESE TERMS:	OR (2) YOU ARE AUTHORIZED TO. AND INTEND TO Iaccept the agreement
Do you accept this license?	I do not accept the agreement
Do you accept this license? InstallBuilder	I do not accept the agreement

Figure 32. AFE5832 GUI Install (TI License Agreement)



AFE5832 GUI Installation

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3. Read the National Instruments[®] License Agreement and select *I accept the agreement* followed by the *Next* button, as in Figure 33.

Magazara Setup	
License Agreement	ų.
Please read the following License Agreement. You must accept agreement before continuing with the installation.	the terms of this
NATIONAL INSTRUMENTS SOFTWA AGREEMENT	
INSTALLATION NOTICE: THIS IS A CONTRACT. BEFORE Y SOFTWARE AND/OR COMPLETE THE INSTALLATION PR	OU DOWNLOAD THE ROCESS, CAREFULLY
Do you accept this license? I accept the agreement I do not accept the agreemen InstallBuilder	t
Sack	Next > Cancel

Figure 33. AFE5832 GUI Install (National Instruments® License Agreement)

4. Read the PSF License Agreement for Python[®] 2.7 and select *I accept the agreement* followed by the *Next* button, as in Figure 34.



🐠 Setup				
License Agreement				- U
Please read the following Lic agreement before continuin	cense Agreement. You g with the installation	u must acce n.	pt the terms of	this
PSF LI	CENSE AGREEMEN	T FOR P	YTHON 2.7	^
This LICENSE AGR Foundation ("PSF' ("Licensee") acces software in source	EEMENT is betwee "), and the Individ ssing and otherwis e or binary form ar	en the Pytual or Org se using P nd its asso	hon Software anization ython 2.7 ociated	e 🗸
۲ ۲	T			÷.
Do you accept this license? InstallBuilder	 I accept the agr I do not accept 	eement the agreem	ent	
37.59%8.5%%A		< Back	Next >	Cancel

Figure 34. AFE5832 GUI Install (PSF License Agreement)

AFE5832 GUI Installation

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5. Allow the software to be installed in the default location by pressing the *Next* button, as in Figure 35.

🐠 Setup	
Installation Directory	-ų
Please specify the directory where AFE5832 EVM will be installed.	
Installation Directory C:\Program Files (x86)\Texas Instruments	
InstallBuilder	
< Back Ne	xt > Cancel

Figure 35. AFE5832 GUI Install (Install Directory)

6. Select the components to install and press Next.

Select Components	
The following components which are modify the selections. AFE5832 EVM LabVIEW Run Time Engine Microsoft .Net Python FTDI Driver	checked will be installed. We recommend not to Click on a component to get a detailed description
stallBuilder	

Figure 36. AFE5832 GUI Install (Select Components)



7. Pressing the *Next* button begins installation, as shown in Figure 37.



Figure 37. AFE5832 GUI Install (Installation Ready)

8. The window shown in Figure 38 appears showing that the installation is in progress.



Figure 38. AFE5832 GUI Install (Installation Progress)

9. A window for the Python 2.7 Setup comes up. Select Install for all users as in Figure 39.



Figure 39. AFE5832 GUI Install (Installation for Users)

If Python is already installed, select the option for *Repair Python 2.7*. Proceed to step 13 and click the *Finish* button.



Figure 40. AFE5832 GUI Install (Python® is Already Installed)



10. Allow the software to be installed in the default destination directory as in Figure 41.

Select Destination Di	rectory
Please select a directory for	• the Python 2.7 files.
	Select Destination Di Please select a directory for Please Python27

Figure 41. AFE5832 GUI Install (Destination Directory)

11. Click Next on the screen displayed in Figure 42.

Python 2.7 Setup		×
	Customize Python 2.7	
	Select the way you want features to be insta Click on the icons in the tree below to chang way features will be installed.	alled. e the
ę	Python Python Provention Provention Tc/Tk Documentation Utility Scripts Test suite	
	Python Interpreter and Libraries]
python windows	This feature requires 22MB on your hard driv has 5 of 5 subfeatures selected. The subfea require 29MB on your hard drive.	ve. It tures
Disk Usage Adva	nced < Back Next > (Cancel

Figure 42. AFE5832 GUI Install (Customize Python®)



AFE5832 GUI Installation

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12. The window shown in Figure 43 appears showing that the installation is in progress.

Python 2.7 3	secup			1
Install Pyth	10n 2.7			
Please v minutes	wait while the Insta s.	aller installs Python 2.7. 1	This may take severa	al
Status:	Copying new files			
		_		



13. Press the *Finish* button, as in Figure 44.



Figure 44. AFE5832 GUI Install: (Python® Finished)



14. Press the *Finish* button, as in Figure 45.



Figure 45. AFE5832 GUI Install (Finished)

The AFE5832 GUI is launched automatically from HSDC Pro, once a device has been selected. Therefore, there is no need to launch AFE5832 GUI manually and there is no need for a desktop shortcut.



Appendix B SLOU489–August 2017

Overview of the AFE5832 EVM GUI Features

This section provides a quick overview of the features and functions of the AFE5832 EVM GUI. The GUI allows the user to easily configure the various functions of the AFE such as receiver gain, bandwidth settings, and timing or clocking control settings.

Operations in the GUI should only be performed after the status at the bottom left-hand corner of the GUI reads **Idle**.

Furthermore, hovering over a control within any of the GUI subtabs provides a description of what the specific control does and shows what register fields would be updated using this control. For example, in Figure 46, hovering over 'LNA_HPF_PROG' or its corresponding drop-down menu brings up a light yellow box describing what this control is responsible for and what register it corresponds to.

OB AFE5832 EVM	
File Script Debug Help	
Eo Quick Setup	
VCA and CW Mixer	
GLOBAL VCA SETTINGS GENERAL SETUP	
LNA_HPF_PROG 75 kHz 🔻	
Select the LPF HPF Corner frequency LNA_HPF_PROG - 0xC7[11:10]	

Figure 46. AFE5832: Hovering Over Controls

The 5 main tabs and their subtabs are as follows:

- Quick Setup
 - HSDC Pro Related Parameters
 - fsamp
 - ADC Input Target Frequency
 - DUT Reset and Initialize Device
 - Data Format
 - Output Format



- ADC Format
- Analog Configuration
 - VCA Gain
 - DTGC Modes

• VCA

- VCA and CW Mixer
 - General Setup
 - VCA PDN Setup
 - TR DIS Setup
 - PD Channel
 - CW Mixer Setup
- DTGC
 - DTGC Modes
 - Test Modes
 - Profile Parameters
 - Attenuator Setup
- ADC
 - Top Level
 - General Setup
 - PDN Setup
 - PLL Setup
 - Test Pattern
 - Global Test Pattern Setup
 - PAT_LVDS
 - PAT_PRBS_LVDS
 - Digital Signal Processing
 - Digital_Offset
 - Digital_Gain
 - Invert_LVDS
 - Misc DSP Setup
 - DIG_HPF
- Register Map Configuration



B.1 Quick Setup Tab

The Quick Setup tab has the following features:

- 1. DUT Reset and Initialize Device buttons
- 2. Data Format 'check-box' menus to select the appropriate *OUTPUT* and *ADC* formats for running various tests
- 3. Choice of Analog Configuration for how VCA gain and DTGC modes need to be configured
- 4. Information boxes on the right-hand side that display the HSDC Pro related Parameters and Device Status

Figure 47 illustrates the AFE5832 Quick Setup tab.

uick Setup	VCA	ADC	Register Map Configu	uration
1.Reset and Initialize the devi	ice		HSDC Pro related I	Parameters
DUT Reset Initialize D	Device		fsamp	20MHz
2 Choose Data Format			ADC Input Target Frequen	cv 2MHz
OUTPUT FORMAT	ADC FORMAT		Auto Colculation of Cohorr	ont Fraguancias
VDS: 10x 10b	Ramp Test Pattern		Auto Calculation of Conero	
UVDS: 12x 12b =	Analog Input	-		
UVDS: 14x 12b				
UVDS: 16x 12b				
LVD3, 10A 12D				
CW: 16x1953MHz - 3.Choose Analog Configuratio	ON DTGC FIXED-GAIN	•		
CW: 16x1933MHz CW: 16x1933MHz 3.Choose Analog Configuration DTGC MODES External Non-Uniform Mode Up-Down Ramp Mode	ON DTGC FIXED-GAIN Max Gain Min Gain		Device Status	
CW:164:1953MHz CW:164:1953MHz CW:164:1953MHz COV:164:1953MHz CUV:164:1953MHz CUV:164:1	ON DTGC FIXED-GAIN Max Gain Min Gain Mid Gain		Device Status	Status
CW: 16:1939MHz - 3. Choose Analog Configuration DTGC MODES - External Non-Uniform Mode Up-Down Ramp Mode Programmable Fixed-Gain Mode Internal Non-Uniform Mode	ON DTGC FIXED-GAIN Max Gain Min Gain Mid Gain		Device Status Parameters Dis LVDS	Status
CW: 16X 1933MHz CW: 16X 1933MH	ON DTGC FIXED-GAIN Max Gain Min Gain Mid Gain		Device Status Parameters DIS_LVDS SFR DATA RATE	Status LVDS interface is enabled fitx
CW: 161 195MH± CW: 161 195MH± CW: 161 195MH± CW: 161 195MH± CHICK CODES External Non-Uniform Mode Up-Down Ramp Mode Programmable Fixed-Gain Mode Internal Non-Uniform Mode	ON DTGC FIXED-GAIN Max Gain Min Gain Mid Gain		Device Status Parameters DIS_LVDS SER_DATA_RATE ADC RES	Status LVDS interface is enabled 16x 12 bit
CW: 16X 1393MHz CW: 16	ON DTGC FIXED-GAIN Max Gain Min Gain Mid Gain		Device Status Parameters DIS_LVDS SER_DATA_RATE ADC_RES PAT_MODES	Status LVDS interface is enabled 16x 12 bit Analoo Inout
CW: 16: 1933MHz CW: 16: 1933MHz CW: 16: 1933MHz CW: 16: 1933MHz CW: 16: 1933MHz CHORE External Non-Uniform Mode UP-Down Ramp Mode Programmable Fixed-5ain Mode Internal Non-Uniform Mode	ON DTGC FIXED-GAIN Max Gain Min Gain Mid Gain		Device Status Parameters DIS_LVDS SER_DATA_RATE ADC_RES PAT_MODES	Status LVDS interface is enabled 16x 12 bit Analog input
CW: 16:1393MH: CW: 16:1393MH: CW: 16:1393MH: CW: 16:1393MH: CHOOSE Analog Configuration DTGC MODES External Non-Uniform Mode Up-Down Ramp Mode Programmable Fixed-Gain Mode Internal Non-Uniform Mode	ON DTGC FIXED-GAIN Max Gain Min Gain Mid Gain		Device Status Parameters DIS_LVDS SER_DATA_RATE ADC_RES PAT_MODES	Status LVOS interface is enabled 16x 12 bit Analog input
CW: 16:1393MH: CW: 16:1393MH: CW: 16:1393MH: CW: 16:1393MH: CHORES	ON DTGC FIXED-GAIN Mac Gain Min Gain Mid Gain		Device Status Parameters DIS_LVDS SER_DATA_RATE ADC_RES PAT_MODES	Status LVDS interface is enabled 16x 12 bit Analog input

Figure 47. AFE5832: Quick Setup Tab


B.1.1 HSDC Pro Related Parameters

The *Quick Setup* tab includes advanced features under the *HSDC Pro related Parameters* section on the right side of the GUI. The feature explanations follow and are shown in Figure 48.

- *fsamp*: Displays the sampling frequency
- ADC Input Target Frequency: This frequency should closely match the input signal that is being supplied

HSDC Pro related Parameters

fsamp	20MHz
ADC Input Target Frequency	5MHz
Auto Calculation of Coherent Frequen	cies 🔳

Figure 48. AFE5832: Quick Setup: HSDC Pro Related Parameters



VCA Tab

B.2 VCA Tab

The VCA tab contains two subtabs: Global VCA Settings and CW Mixer.

B.2.1 VCA and CW Mixer Subtab

The VCA and CW Mixer subtab for the AFE5832 has the following features:

- 1. Settings for configuring LNA high-pass filter and setting corner and cut-off frequencies
- 2. Enable or disable LNA HPF at certain channel inputs
- 3. Fully or partially powering down entire blocks or individual channels in the VCA block
- 4. Configuring the device in CW mode
- 5. Controls for setting the corresponding CW mixer channel phases

Quick Setup	VCA	ADC	Register M	ap Configuration	
and CW Mixer		DTGC			
GLOBAL VCA SETTINGS		CW MIXER SETUP			
GENERAL SETUP	VCA PDN SETUP	1X_CLK_BUF_MODE			
LNA_HPF_DIS	HIGH_POWER Low power mode	16X_CLK_BUF_MODE			
LNA_HPF_PROG 75 kHz	GBL_PDWN 🕅 FAST_PDWN	CW_TGC_SEL	TGC Mode 🔻		
LPF_PROG 15 MHz	PDWN_LNA PDWN_FILTER [CW MIXER PHASE			
		CW_MIX_PH_CH1	0	CW_MIX_PH_CH9	0
TR DIS SETUP	PD CHANNEL	CW_MIX_PH_CH2	0 🔻	CW_MIX_PH_CH10	0 🔻
TR_EXT_DIS External Pins V	PDCH1 PDCH9				
TR DIS1	PDCH2 PDCH10	CW_MIX_PH_CH3	U	CW_MIX_PH_CH11	U
	PDCH3 PDCH11	CW_MIX_PH_CH4	0	CW_MIX_PH_CH12	0
TR_DIS2	PDCH4 PDCH12	CW_MIX_PH_CH5	0	CW_MIX_PH_CH13	0 🔻
TR_DIS3	PDCH5 PDCH13				
TR_DIS4	PDCH6 PDCH14	CW_MIX_PH_CH6	0	CW_MDC_PH_CH14	U V
	PDCH7 PDCH15	CW_MIX_PH_CH7	0 🔻	CW_MIX_PH_CH15	0
	PDCH8 PDCH16	CW_MIX_PH_CH8	0	CW_MIX_PH_CH16	0 🔻

Figure 49. AFE5832: VCA: VCA and CW Mixer

B.2.2 **DTGC Subtab**

The DTGC subtab for the AFE5832 has the following features:

- 1. Options for selecting different DTGC modes and setting parameters within these modes
- 2. Enable interrupts and provide pulses on the TGC pin
- 3. Configure specific parameters for different profiles by setting gains, start and stop indices, and attenuation factors
- 4. Enable and disable the attenuator

uick Setup		CA VCA	3	ADC			Register Map Co	onfiguration	
and CW Mixer			Maria		DTGC				
DTGC MODES									
	Principal		PROFILE PARA	METERS (app	blicable to Up Down	n Ramp, E	cternal and Internal Non-Unife	orm Modes)	_
MODE_SEL	External	non-uniform		E_EXI_DIS	TGC_PROF PINS		PROFILE_REG_SEL	Profile U	
PROGRAMMABLE FIXED-GA	IN MODE		Profile 0		Profile 1		Profile 2	Profile 3	
MANUAL_GAIN_DTGC	0	\$	START	_GAIN_0	0	\$	STOP_GAIN_0	159	\$
INTERNAL NON-UNIFORM M	ODE (specific pa	rameters)	POS_S	TEP_0	0	\$	NEG_STEP_0	255	\$
SLOPE FAC	ō	4	START	_INDEX_0	0	\$	STOP_INDEX_0	159	*
MEM BANK SEL	Bank 0	-	START	_GAIN_TIME_0	0	\$	HOLD_GAIN_TIME_0	0	*
LOAD DTGC MEMORY	Load Memory Br	ank	FIX_AT	TEN_EN_0			ATTENUATION_0	0	\$
TEST MODES			ATTENUATOR	SETUP					
ENABLE_INT_START	External TGC st	art	DIS ATTEN	4 E					
NEXT_CYCLE_WAIT_TIME	0	\$	FLIP_ATTE	N					
MANUAL START	No Operation	1	INP RES S	EL 5	0 ohm 🔍				

Figure 50. AFE5832: VCA: DTGC



ADC Tab

B.3 ADC Tab

The ADC tab contains three subtabs: Top Level, Test Pattern, and Digital Signal Processing.

B.3.1 Top Level Subtab

The Top Level subtab for the AFE5832 has the following features:

- 1. Enabling and disabling the LVDS interface and selecting data rates, delays, and resolutions
- 2. Powering down individual LVDS output lines
- 3. Software and PLL resets

Quick Setup	🗘 VCA			}		Register Map Configur	ation
) Level	Test Pattern				Digital Signal	l Processing	
	GENERAL SETUP			PDN SETUP			
	SOFTWARE_RESET	Click to Reset		GLC	BAL_PDN 🔲		
	LVDS_RATE_2X	1X Rate		PDN_LVDS			
	LVDS_DCLK_DELAY_ PROG	0	\$	PDN_LVDS1	PDN_LVE	DS9 🕅	
	DIS_LVDS	Disabled	•	PDN_LVDS2		DS10	
	LOW_LATENCY_EN	Default Latency	•	PDN_LVDS3	PDN_LVE	DS11 🕅	
	DATA_FORMAT	2's Complement		PDN_LVDS4	PDN_LVE	DS12	
	MSB_FIRST	LSB First	•	PDN_LVDSS	PDN_LVE	DS13	
	SER_DATA_RATE	16x	•	PDN_LVDS6		DS14	
	AUC_RES	12-00		PDN_LVDS7	PDN_LVE	DS15	
				PDN_LVDS8 E	PDN_LVI	DS16	
	PLL SETUP						
	PLLRST1	Click to Init PLL	1				
	PLLRST2	Click to Init PLL	2				

Figure 51. AFE5832: ADC: Top Level



B.3.2 Test Pattern Subtab

The Test Pattern subtab for the AFE5832 has the following feature:

· Selecting preset or custom test patterns to be generated by ADC for LVDS or on certain clock lines

Quick Setup	\$V	/CA		ADC		Register Map Co	nfiguration
Level		Test Patte	ern		Digi	tal Signal Processing	
	GLOBA	L TEST PATTER	N SETUP				
	PAT	SELECT_IND	1	PRBS_EN	PRBS_SYNC	PRBS_MODE	
	PAT	_MODES_FCLK	Normal Oper	ation	SEL_PRBS_PAT_FCL	CUSTOM_PATTERN	
		PAT_MODES	Normal Oper	ation 🔻	SEL_PRBS_PAT_GBL		
PAT_LVDS						PAT_PRBS_LVDS	
PAT_LVDS1	Normal Operation	•	PAT_LVDS9	Normal Operation	*	PAT_PRBS_LVDS1	PAT_PRBS_LVDS9
PAT_LVDS2	Normal Operation		PAT_LVDS10	Normal Operation		PAT_PRBS_LVDS2	PAT_PRBS_LVDS10
PAT_LVDS3	Normal Operation		PAT_LVDS11	Normal Operation		PAT_PRBS_LVDS3	PAT_PRBS_LVDS11
PAT_LVDS4	Normal Operation		PAT_LVDS12	Normal Operation		PAT_PRBS_LVDS4	PAT_PRBS_LVDS12
PAT_LVDS5	Normal Operation	V	PAT_LVDS13	Normal Operation	V	PAT_PRBS_LVDS5	PAT_PRBS_LVDS13
PAT_LVDS6	Normal Operation	V	PAT_LVDS14	Normal Operation	W	PAT_PRBS_LVDS6	PAT_PRBS_LVDS14
PAT_LV0S7	Normal Operation	V	PAT_LVDS15	Normal Operation	V	PAT_PRBS_LVDS7	PAT_PRBS_LVDS15
PAT_LVDS8	Normal Operation	v	PAT_LVDS16	Normal Operation	W	PAT_PRBS_LVDS8	PAT_PRBS_LVDS16

Figure 52. AFE5832: ADC: Test Pattern

ADC Tab



ADC Tab

B.3.3 Digital Signal Processing Subtab

The Digital Signal Processing subtab for the AFE5832 has the following features:

- 1. Setting the digital gain and digital offset or automatically calculating a channel offset for each of the 16 ADC channels, individually
- 2. Inverting the digital outputs on various LVDS output lines
- 3. Enabling or disabling the digital high pass filter for groups of channels

Quick Setup	VCA	\$	ADC	Register Map Configuration	
evel	Test Pa	ttern		Digital Signal Processing	
DIGITAL_OFFSET				INVERT_LVDS	
DIG_OFFSET_EN		OFFSET_REMOVAL_SELF		INVERT_LVDS1	INVERT_LVDS9
Manual Offset - Odd Channels	Manual Offset - E	en Channels	Auto Offset	NVERT_LVDS2	INVERT_LVDS10
				INVERT_LVDS3	INVERT_LVDS11
OFFSET_ADC10 OFFSET_ADC20 OFFSET_ADC	30 OFFSET_ADC40 C	FFSET_ADC50 OFFSET_ADC6	60 OFFSET_ADC70 OFFSET_AD	NVERT_LVDS4	INVERT_LVDS12
	0	0	0 🔷 0	INVERT LVDS5	INVERT_LVDS13
OFFSET_ADC90 OFFSET_ADC100 OFFSET_ADC	110 OFFSET_ADC120 C	FFSET_ADC130 OFFSET_ADC1	140 OFFSET_ADC150 OFFSET_AD	DC160 INVERT LVDS6	NVERT LVDS14
0 0 0 4	0 💠	0 💠 0 💠	0 🌲 0		
Note: OFFSET_CH is a 10- bit signed valu	e. Enter unsigned value in	the control. E.g1 should be en	ntered as 1023	INVERT_LVDS8	INVERT_LVDS16
DIGITAL GAIN				MISC DSP SETUP	
DIG_GAIN_EN				AVG_EN CHOPPER_EN	EN_DITHER
Odd Channels		Even Channels		DIG HDF	
GAIN ADC10 GAIN ADC20 GAIN ADC30	GAIN ADC40 G	AIN ADC50 GAIN ADC50	GAIN ADC70 GAIN ADC8	DIG_HPF_EN_ADC1-4 HPF_COP	RNER_ADC1-4 0
0 💠 0 💠 0	0	0 💠 0 💠	0 💠 0	DIG_HPF_EN_ADC5-8 HPF_COF	RNER_ADC5-8 0
GAIN_ADC86 GAIN_ADC106 GAIN_ADC11	GAIN_ADC120 G	AIN_ADC130 GAIN_ADC140	GAIN_ADC150 GAIN_ADC1	80 DIG_HPF_EN_ADC9-12 HPF_COF	RNER_ADC9-12 0

Figure 53. AFE5832: ADC: Digital Signal Processing



B.4 Register Map Configuration Tab

The *Register Map Configuration* tab is a tool to write to and read from specific registers using SPI. The tab contains multiple useful subsections and features that allow the user to interact with the register map, select update modes, and manipulate register values.

B.4.1 Tab Subsections

The following key words are useful in navigating the map:

- *Register Map*: Displays all the details for each of the registers in the device as well as the fields and bits contained within that register
- Field View: Displays all the Field Names and Field Values corresponding to those names
- *Register Description*: Describes each of the fields within the registers and what writing a certain sequence of '0s' and '1s' indicates in that particular field
- Update Mode: Allows the user to choose an Immediate or Deferred method of updating the content of the registers
- *Export HSDC Parameters*: Updates HSDC Pro GUI with the register-level changes made to the AFE5832EVM.

B.4.2 Register Map Interaction

Clicking on a register name produces a list of the fields within that specific register. Clicking on a field name highlights the bits within the register that correspond to that field. In Figure 54, *Register 3* has been clicked. All the fields within Register 3 come up on the right-hand side of the GUI. Clicking on any one of these field names highlights the corresponding bits for this field in the *Register Map*.

Quick Setup			\$	VCA							-	Q A	DC								Register Map Co	nfigurati	on		
Vrite Selected VVrite Mo	dified Rea	d Selected	F	Read	All			1	Jpd	ate Mi	ode	In	nme	diate	•										
Register Map																					Field View				
Register Name	Address	Default	Mode	Size	Value	15	14	13	12	11 1	0 1	9 8	7	6	5	4	3	2	1	0 🔺	Field Name	Fi	eld Value		
AFE5832_ADC																				10	Register 3 Reserved	Di	sabled		_
Register 0	0x00	0x0000	RM	16	0x0000	0	0	0	0	0 1	0 1	0 0	0	0	0	0	0	0	0	0	RESERVED, REGISTER	R3 0x	1		_
Register 1	0x01	0x0000	RM	16	0x0000	0	0	0	0	0 1	0 1	0 0	0	0	0	0	0	0	0	0	Register 2 Received	Di	cobled		
Register 2	0x02	0x0000	RM	16	0x0000	0	0	0	0	0 1	0 1	0 0	0	0	0	0	0	0	0	0	Register 5_Reserved	DI	sauleu		17.03
Register 3	UxU3	00000	RAW	16	0x8010	1	U	U	0	0 1			U	U	0	1	U	U	ų	0	DIG_OFFSET_EN	DI	gital offset sub	traction disab	nea
Register 4	0x04	0x0000	FOVV DAR	10	0x0000	0	0	U	0	0			0	0	0	0	0	0	0	0	OFFSET_CORR_DELA	Y_FR(0x	:0		
Register 5 Register 7	0x05	0x0000	PAN/	10	0x0000	0	0	0	8	0			0	0	0		0	0	0	0	Register 3_Reserved	Di	sabled		
Register 8	0x07	0x0000	RAM	16	0x0000	0	0	0	0	0 1			0	0	0	0	0	0	0	0 0	DIG_GAIN_EN	Di	gital gain disal	bled	
Register 11	0x0B	0x0000	RAM	16	0x0000	n	0	ñ	ň	0 1	ň	n n	l n	0	n	0	n	n	ñ	ñ	SER DATA RATE	16	iX		-
Register 13	Dx0D	0x0000	RM	16	0x0000	ň	ñ	ň	ň	ñ i	ňi	n n	Ĭ	ň	ň	ň	ñ	ň	ň	õ.	oungoini grane				_
Register 14	0x0E	0x0000	RM	16	0x0000	0	0	0	ō	0 1	o i	0 0	0	0	0	0	ō	0	0	0		-			_
Register 15	0x0F	0x0000	RM	16	0x0000	0	0	0	0	0 1	0 1	0 0	0	0	0	0	0	0	0	0					
Register 16	0x10	0x0000	RM	16	0x0000	0	0	0	0	0 1	0 1	0 0	0	0	0	0	0	0	0	0		1			
Register 17	0x11	0x0000	RM	16	0x0000	0	0	0	0	0 1	0 1	0 0	0	0	0	0	0	0	0	0					
Register 18	0x1 2	0x0000	RM	16	0x0000	0	0	0	0	0 1	0 1	0 0	0	0	0	0	0	0	0	0					
Register 19	0x13	0x0000	RM	16	0x0000	0	0	0	0	0 1	0 1	0 0	0	0	0	0	0	0	0	0					_
Register 20	0x1 4	0x0000	R/W	16	0x0000	0	0	0	0	0 1	0 1	0 0	0	0	0	0	0	0	0	0		-			
Register 21	0x15	0x0000	RM	16	0x0000	0	0	0	0	0 1	0 1	0 0	0	0	0	0	0	0	0	0					
Register 23	0x17	0x0000	RM	16	0x0000	0	0	0	0	0 1	0 1	0 0	0	0	0	0	0	0	0	0					
Register 24	0x18	0x0000	RW	16	0x0000	0	0	0	0	0 1	0 1	0 0	0	0	0	0	0	0	0	0					
Register 25	0x1 9	0x0000	RM	16	0x0000	0	0	0	0	0 1	0 1	0 0	0	0	0	0	0	0	0	0					-
Register 26	Ox1A	0x0000	R/W	16	0x0000	0	0	0	0	0 1	0 1	0 0	0	0	0	0	0	0	0	0					_
gister Description																									
gister 3_Reserved[3:0]																E	llock				Address	Va	lue	Read Data	a
st Write 0															=	1	TOCIL	ACC	600	2 ADC				riode bate	-
SERVED_REGISTER3[4:	4]																	-u- E		2_ADC		×	8010	×U	
st be set to 1																									-
gister 3_Reserved[7:5]																						10	vrite Generic	Read Gen	ier

Figure 54. Clicking on Register and Field Names



Register Map Configuration Tab

B.4.3 Update Modes

There are two options to change the *Update Mode* on the GUI as shown in Figure 57: (a) Immediate and (b) Deferred.

Quick Setup			*	VCA				1			*			liata	-							Register Map Config	uration	
ite Selected Write Mo	dified Rea	d Selected	F	Read /	All			(lpda	ate Mo	de	V De	aterre	ed .			/)						
egister Map										-	-	_	_	_	-	-					ğ	Field View		
Register Name	Address	Default	Mode	Size	Value	15	14	13	2	11 10	9	8	7	6	5	4	3	2	1	0 🔺	11	Field Name	Field Value	
AFE5832_ADC			and the second se								T				100-111					1	1 P	RESERVED REGISTER11	Disabled	
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Register 1	0x01	0x0000	R/W	16	0x0000	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0			Disabled	
Register 2	0x02	0x0000	RM	16	0x0000	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0		EN_DITHER	Dimerdisabled	
Register 3	0x03	0x0000	R/W	16	0x8010	1	0	0	0	0 0	0	0	0	0	0	1	0	0	0	0		Register 11_Reserved	Disabled	
Register 4	0x04	UXU000	RIW	16	UXU000	0	U	U	U	0 0	0	0	0	0	U	U	U	U	2	0				
Register 5	0x05	UXUUUU	RIVY	16	0x0000	U	U	U	0	0 0	U	U	U	U	U	U	U I	0	0	0				
Register /	0x07	0x0000	R/W	10	0x0000	0	0	0		0 0	0	0	0	0	0	8	S.	0	8	0.0				
Register 11	DV0B	0x0000	EWW	16	0x0000	0	0	0	0	8 8	0	0	B	0	8	0	6	0	0	0				
Register 13	0x0D	0x0000	RM	16	0x0000	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0			-	
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Register 17	0x11	0x0000	RM	16	0x0000	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0				
Register 18	0x12	0x0000	RAV	16	0x0000	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0				
Register 19	0x1 3	0x0000	R/W	16	0x0000	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0				
 Register 20 	0x14	0x0000	RAV	16	0x0000	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0				
Register 21	0x15	0x0000	R/W	16	0x0000	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0				
Register 23	0x17	0x0000	RAV	16	0x0000	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0				
Register 24	Ox18	0x0000	R/W	16	0x0000	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0				
Register 25	0x19	0x0000	R/W	16	0x0000	0	0	0	0	0 0	0	0	0	0	0	0	0	0	0	0				
Register 26	Ux1A		RW	16	UXUUUO	U	U	U	U I	0 0	1.0	U	U	U	U	U	U	U	0	0 .	11			
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ERVED_REGISTER11[0:0]															в	lock					Address	Value	Read Data
Write 0															-	ΠĒ		AFE	583	2 ADC	2			× 0
ster 11_Reserved[10:1]																-		1995	2005		35	* <u> </u>		0
I WITTLE DI 4-441																							Trade and a survey of	
DURCHILLI	-	higher and																					Write Generic	Read Gene

Figure 55. AFE5832: Register Map Configuration: Update Modes



- 1. The *Immediate* update mode allows the user to change the values of any number of bits or fields within the registers, and these changes are immediately written to the device. Within this update mode, there exists options to (a) *Read Selected* data, (b) *Read All* data, and (c) *Write Selected*.
 - 1. *Read Selected*: Clicking this option in the top left-hand corner displays the value contained in the register in the *Read Data* field in the lower right-hand corner of the GUI. In the same area of the GUI, the *Address* field will display the address of the selected register, and the *Value* field will display the value contained in that register as shown in Figure 56.
 - 2. *Write Selected*: This option indicates that only the values in a **selected** register is written to the device. In order to select a particular register to write to, click on any register under *Register Name* and then choose to write to the selected register.
 - 3. *Read All*: This option reads data from all the registers in the device regardless of whether they are selected or not.

AFE5832 EVM																									- 8 💉
File Script Debug Help						_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_			
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E Quick Setup		_	Ø	VCA	١							₽	AD	С									Register Map Configu	ration	
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Register 1	0x01	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		Register 4_Reserved	Disabled	
Register 2	0x02	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6	DATA_FORMAT	I was complement form	lat for output
Register 3	0x03	0x0000	RAV	16	0x8010	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0		MSB_FIRST	The LSB is transmitted	first on seria
Register 4	0x04	0x0000	RAW	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		PRBS_EN	PRBS sequence generation	ation block d
Register 5	0x05	0x0000	RAV	16	UXUUUU	0	U		0	0	0	0	0	0	U	0	0	U	0	U	0		PRBS_MODE	23-bit PRBS generator	
Register /	0:07	0x0000	DAR	10	0x0000	0	0	U U	S.	8	0	0	0	0	8	S.	0	8	0	0			PRBS_SYNC	Normal operation	
Register 11	0x08	0x0000	RM	16	0x0000	0	0	n i	0	0	0	0	0	0	0	0	0	n.	0	0			PAT SELECT IND	All I VDS output data lin	es have the
Register 13	0x0D	0x0000	RAV	16	0x0000	0	0	n	ñ	n	n	n	0	0	n	ñ	0	n	0	0	l n		NUTO OFFORT DEMOVIE	An EVE C Colpor Cata In	co nave and
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Register 15	0x0F	0x0000	RAV	16	0x0000	Ō	ō	Ō	ō	0	0	ō I	ō	ō	0	ō	ō.	ō.	0	0	0	8	OFFSET_REMOVAL_START_	_ 0x0	
Register 16	0x10	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R I	OFFSET_REMOVAL_START_	Auto offset correction in	itiated when
Register 17	0x11	0x0000	RAW	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6	OFFSET_REMOVAL_SELF	0x0	
Register 18	0x12	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6			
Register 19	0x13	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ř I			
Register 20	0x14	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6			
Register 21	0x15	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6			
Register 23	0x17	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6			
Register 24	0x18	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6			
Register 25	0x19	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8_			
Register 26	0x1A	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				v
Register Description																									
ADC RES[1:0]																			v				Addition	Value Res	
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00 = 12-bit resolution																			AC	200	32_	nuc	× 4	× U ×	U
01 = Do not use																									
10 = Do not use																								Write Generic Re-	ad Generic
11 = 10-bit resolution																्र									
Idle																								ed 🛛 🐺 Texas Ins	STRUMENTS

Figure 56. AFE5832: Register Map Configuration: Immediate Update Mode



Register Map Configuration Tab

2. The *Deferred* update mode allows the user to change the values of any number of bits or fields within the registers, but these changes will not be written to the device instantly. Unless the changes are implemented, data cannot be read from the registers either.

When a user changes the contents of a register in *Deferred* mode, the GUI will turn the changed register font a blue color. These *blue-font registers* indicate that a change has been made but not yet implemented.

Within the *Deferred* update mode, there exist options in the top left-hand corner of the GUI for deciding how the changes should be implemented (shown in Figure 57): (a) *Read Selected* data, (b) *Write Selected* data, and (c) *Write Modified* data, or (d) *Read All* data.

- 1. *Read Selected*: Clicking this option in the top left-hand corner displays the value contained in the register in the *Read Data* field in the lower right-hand corner of the GUI. In the same area of the GUI, the *Address* field will display the address of the selected register, and the *Value* field will display the value contained in that register as shown in Figure 57.
- 2. *Write Selected*: This option indicates that only the values in a **selected** register is written to the device. In order to select a particular register to write to, click on any register under *Register Name* and then choose to write to the selected register.
- Write Modified: If the user has made changes to multiple registers in the register map, this option allows the user to write the changes within all modified registers to the device. Once all changes have been written, there will no longer be any *blue-font registers*, indicating that all the changes have been implemented.
- 4. *Read All*: This option reads data from all the registers in the device regardless of whether they are selected or not.
 - **NOTE:** If any number of registers contains modified values that are not yet written, none of the *Read* options can be used. The user is prompted to either write the modified fields to the device or discard the changes.

Script Debug Help							_		_						_											
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Quick Getup	_		34	YCA	_						×,	S AE	C									Register Map Conf	iguratio	on		
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gister wap			_	-	-																Fie	eld View				
Register Name	Address	Default	Mode	Size	Value	15	14	13 1	2 1	1 10	9	8	7	6	5	4	3	2	1	0 🔺	Fi	ield Name	Fie	ald Value		
AFE5832_ADC																				1	0	FFSET CORR DELAY	FRC 0x	.0		_
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Register 1	0x01	0x0000	R/W	16	0x0000	0	0	0 1		0 0	0	0	0	0	0	0	0	0	0	0	-	AT MODER	De	ofoult		
Register 2	0x02	0x0000	RAW	16	0x0000	0	0	0		0 0	0	0	0	0	0	0	0	0	0	0	F.	AI_MODES		naun	0	_
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Register 4	0x04	0×0000	DAM	16	0x0000	0	0	0			0	0	0	0	0	0	0	0	0	0	A	WG_EN	No) digital averag	ging	
Register 5	0x03	0x0000	DAV	16	0x0000	0	0	0 1			0	0	0	0	0	0	0	0	0	0	L	.0W_LATENCY_EN	De	efault latency w	vith digital fea	itur
Register 9	0x07	0x0000	RM	16	0×0000	0	0				0	0	0	6	i i	n i	8	0	0	0	P.	AT MODES FOLK	De	afault		
Register 11	0x0B	0x0000	RM	16	0x0000	0	0	0	1	0 0	l ő	n.	n.	0	ñ	ň	ñ l	0	ñ	0		- 27				-
Register 13	0x0D	0x0000	RM	16	0x0000	n	ñ	n i	í.	0 0	0	n.	0	ñ	ñ	ň	ň	n	n	ñ						
Register 14	0x0E	0x0000	RAV	16	0x0000	ñ	ň	ň	í I	n n	ň	ň	ň	ň	ň	ň	ň	ñ	ñ	ñ			_			
Register 15	0x0E	0x0000	RM	16	0x0000	n	ñ	n i	i I	0 0	0	n i	0	ñ	ñ	ň	ň	n	ñ	ñ						
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Register 18	0x12	0x0000	RM	16	0x0000	0	Ō	0 1	5	0 0	0	0	0	0	0	ō	0	0	0	0						-
Register 19	0x13	0x0000	RAV	16	0x0000	0	Ō	0 1		0 0	0	0	Ō	ō	0	ō	ō	0	0	0			_			
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Register 21	0x15	0x0000	RAV	16	0x0000	0	ō	0 1	5	0 0	0	0	ō	ō	0	ō	ō	0	0	0						
Register 23	0x17	0x0000	RM	16	0x0000	0	0	0 1	n I.	0 0	0	0	0	0	0	0	0	0	0	0						-
Register 24	0x18	0x0000	RAV	16	0x0000	0	0	0 1	5	0 0	0	0	0	0	0	0	0	0	0	0						-
Register 25	0x19	0x0000	RAV	16	0x0000	0	0	0 1		0 0	0	0	0	0	0	0	0	0	0	0						_
Register 26	0x1A	0x0000	RAW	16	0x0000	0	0	0 1		0 0	0	0	0	0	0	0	0	0	0	0 🔻						
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emaining two MSB bits	are the OFFS	T CORR	DELA	Y ERI	OM TX T	RIG	7.61	hits (h	its 1	(0-9) ii	n rec	ister	3	30	-			AFE	583	2_ADC	2	🔻 🛛 🗙 2	×	0	× 0	
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Figure 57. AFE5832: Register Map Configuration: Deferred Update Mode



B.4.4 Manipulating Register Values

Writing to a register or changing the existing value in a register can be accomplished via (1) GUI controls, or (2) manual data entry:

1. *GUI Controls*: Hovering over the corresponding *Field Value* to a *Field Name* generates a drop-down menu from which a series of options can be picked to populate that field as Figure 58 shows. The change shows up in the register map. The value for a specific bit can also be changed by clicking on the bit in the register map.

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rite Selected Write Mo	dified Rea	d Selected	F	Read	AJI .			į.	Jpd	ate N	lode		Det	ferred	1	2						
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Register Name	Address	Default	Mode	Size	Value	15	14	13	12	11	10	9	8	7 6	3 5	i 4	3	2	1	0 🔺	Field Name	Field Value
AFE5832_ADC												T									Register 3 Reserved	Disabled
Register 0	0x00	0x0000	R₩	16	0x0000	0	0	0	0	0	0	0	0	0 0	0 0	0	0	0	0	0	RESERVED REGISTERS	Dv1
Register 1	0x01	0x0000	R/W	16	0x0000	0	0	0	0	0	0	0	0	0 0	0 0	0	0	0	0	0	Bagister 2. Basarrad	Disphled
Register 2	0x02	0x0000	RM	16	0x0000	0	0	0	0	0	0	0	0	0 0) (0	0	0	0	0	Register 3_Reserved	Disabled
Register 3	0x03	0x0000	RAW	16	0x8010	1	U	U	U	U	0	8	0	0 0			U	U	0	0	DIG_OFFSET_EN	Digital offset subtraction disab
Register 4	0x04	0x0000	RIV	10	000000	0	0	0	0	0	0	0	0			U	U	U	0	0	OFFSET_CORR_DELAY_FF	RC 0x0
Register 5 Periotor 7	0x05	0x0000	DAV	16	0x0000	0	0	0	0	0	0	0	0					0	0	0	Register 3_Reserved	Disabled
Register 9	0x07	0x0000	RM	16	0x0000	0	0		8	n l	0	0	0						0	0	DIG GAIN EN	Digital gain disabled
Register 11	0x08	0x0000	RM	16	0x0000	n l	n	ň	n	ñ.	ñ	n l	ñ	n r	n n	i n	n l	0	0	6	SER DATA RATE	168
Register 13	0×0D	0x0000	RAV	16	0x0000	ñ	n	ñ	ñ	ñ	ñ	ñ	ñ	n n	n r	i n	n.	n.	n	0	Research Constraints of Constraints	1.2%
Register 14	0x0E	0x0000	RAV	16	0x0000	ō	0	ō	0	ō	ō .	0	ō l	0 0		0	0	0	0	0		12A
Register 15	0x0F	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0 0		0	0	0	0	0		14X
Register 16	0x10	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0 0	0 0	0	0	0	0	0		16X
Register 17	0x11	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0 0	0 0	0	0	0	0	0		10X
Register 18	0x12	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0 0	0 0	0	0	0	0	0		Unused
Register 19	0x13	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0 0	0 0	0	0	0	0	0		Unused
Register 20	0x14	0x0000	RM	16	0x0000	0	0	0	0	0	0	0	0	0 0	0 0	0	0	0	0	0		Linused
Register 21	0x15	0x0000	R/₩	16	0x0000	0	0	0	0	0	0	0	0	0 0	0 0	0	0	0	0	0		onased
Register 23	0x17	0x0000	RMV	16	0x0000	0	0	0	0	0	0	0	0	0 0	0 0	0	0	0	0	0		
Register 24	0x18	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0 0	0 0	0	0	0	0	0		
Register 25	0x19	0x0000	RM	16	0x0000	0	0	0	0	0	0	0	0	0 0	0 0	0	0	0	0	0		
Register 26	Ox1A	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0 0	0 0	1 0	0	0	0	0	I; I	
ister Description																						
ister 3_Reserved[3:0]																	Bloc	k			Address	Value Read Data
st Write 0															E		0100	AFF	-683	32 ADC		
SERVED_REGISTER3[4:	4]																-	9.6%				× 0010
st be set to 1																						
jister 3_Reserved[7:5]																						Write Generic Read Gen

Figure 58. AFE5832: Register Map Configuration: Changing Register Value



Register Map Configuration Tab

2. *Manual Data Entry*: The value for a register can also be changed by manually typing in a hexadecimal value under the *Value* field in the bottom right-hand corner of the GUI. After typing in a value, clicking *Write Generic* will write this change to the device. The change will show up in the register map. Clicking *Read Generic* will read the data from that register and the hexadecimal value will show up in the *Read Data* field.

Write Selected Write Modified Read Selected Read Address Default Mode Size Default Update Mode Default I Register Map Register Name Address Default Mode Size Value 15 14 13 12 11 10 9 7 6 5 4 3 2 1 0				Q	VCA	·							\$	ADO	C								Register Map Configu	uration
Register Mame Address Default Mode Size Value 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0	ite Selected Virite M	odified Rea	d Selected		Read	All				Upd	late M	vlode		Det	ferre	d	¥							
Register Name Address Default Mode Size Value 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 A AFE5932_ADC 0x00 0x000 Register Register 0x00 Register Register </th <th>egister Map</th> <th></th> <th>Field View</th> <th></th>	egister Map																						Field View	
AFES32_ADC Register 0 0.00 Register 1 0.00 Register 4 0.00 Register 3 0.00 Register 3 0.00 Register 4 0.00 Register 5 0.00 Register 7 0.00 Register 1 0.00	Register Name	Address	Default	Mode	Size	Value	15	14	13	12	11	10	9	8	7	6	5	4	3	2 1	1	0 🔺	Field Name	Field Value
Fegister 0 0x00 0x000 RAVY 16 0x0000 0	AFE5832_ADC																						ADC RES	12-bit resolution
Register1 0xd1 0xd000 RAV 16 0x0000 0<	Register 0	0x00	0x0000	RAW	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0	Register 4 Reserved	Disabled
Register 3 0.002 0.0000 R/W 16 0.0000 0	Register 1	0x01	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0				0	DATA FORMAT	Twos complement format for output
Register 3 0x000	Register 2	0x02	010000	DAAC	10	0x0000	1	0	0	0	0	0	0	0	0	0		4				0	MOD EIDOT	The LCB is transmitted first on
Register 5 0x06 0x000 RAV 16 0x0000 0 <td>Register 4</td> <td>0x03</td> <td>0x0000</td> <td>RAN</td> <td>16</td> <td>0x0010</td> <td>0</td> <td>10</td> <td>n</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>n</td> <td>ñ</td> <td>6</td> <td></td> <td></td> <td></td> <td>0</td> <td>DDDC FN</td> <td>DDDC appropriate apparation black</td>	Register 4	0x03	0x0000	RAN	16	0x0010	0	10	n	0	0	0	0	0	0	n	ñ	6				0	DDDC FN	DDDC appropriate apparation black
Register 7 bx07 bx0000 RAW 16 bx0000 0 </td <td>Register 5</td> <td>0x05</td> <td>0x0000</td> <td>RAV</td> <td>16</td> <td>0x0000</td> <td>0</td> <td>0 0</td> <td>) (</td> <td>5</td> <td>0</td> <td>PRD2_EN</td> <td>FRBS sequence generation block</td>	Register 5	0x05	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (5	0	PRD2_EN	FRBS sequence generation block
Register 8 0x88 0x0000 RAW 16 0x0000 0	Register 7	0x07	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	PRBS_MODE	23-bit PRBS generator
Register11 0x08 0x0000 RAV 16 0x0000 RVV 16 0x0000 0	Register 8	0x08	0x0000	RAW	16	0x0000	0	0	0	0	Û	0	0	0	0	0	0	0	0 0) (3	0	PRBS_SYNC	Normal operation
Register 13 0x0D 0x0D0 RAW 16 0x0000 R W 16 0x0000 0	Register 11	0x0B	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0 () (וו	0	PAT_SELECT_IND	All LVDS output data lines have the
Hegister14 Odde Doubling RAW 16 Doubling 0 <	Register 13	0x0D	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0			21	0	AUTO_OFFSET_REMOVAL_	A 0x0
register 15 0x00 0x000	Register 14	UXUE	000000	RAV	16	0x0000	0	0	U	0	0	0	0	0	0	0	0	0				0	OFFSET_REMOVAL_START	_ 0x0
Register 17 Dx11 Dx0000 FW 16 Dx0000 0 <td< td=""><td>Register 15 Register 16</td><td>Ox0P</td><td>0x0000</td><td>DAA</td><td>16</td><td>0x0000</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td><td></td><td>51</td><td>0</td><td>OFFSET REMOVAL START</td><td>Auto offset correction initiated whe</td></td<>	Register 15 Register 16	Ox0P	0x0000	DAA	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0			51	0	OFFSET REMOVAL START	Auto offset correction initiated whe
Register 18 0x12 0x0000 RAW 16 0x0000 0	Register 17	0×11	0x0000	RAV	16	0x0000	n	n	ñ	ñ	n	n	ñ	ñ	ñ	ň	ñ	ñ	n	i li	ň I.	ñ	OFFSET REMOVAL SELF	
Register 19 0x13 0x0000 R/W 16 0x0000 0	Register 18	0x12	0x0000	RAV	16	0x0000	ŏ	ŏ	ŏ	ŏ	0	0	õ	õ	õ	ŏ	ŏ	õ	0 0		5	õ	off der_nemonie_deed	one
	Register 19	0x13	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0		-
Register 21 Oxf5 0x0000 R/W 16 0x0000 0<	Register 20	0x14	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (D	0		
- Register 23 0x17 0x0000 RAW 16 0x0000 0 <t< td=""><td>Register 21</td><td>0x15</td><td>0x0000</td><td>RAV</td><td>16</td><td>0x0000</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0 0</td><td>) (</td><td></td><td>0</td><td></td><td></td></t<>	Register 21	0x15	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (0		
Register 24 0xt8 0x0000 R/W 16 0x0000 0	Register 23	0x17	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0		
Register 25 0x19 0x0000 R/W 16 0x0000 0 <th0< th=""> <th0< t<="" td=""><td>Register 24</td><td>0x18</td><td>0x0000</td><td>RAV</td><td>16</td><td>0x0000</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0 0</td><td>) (</td><td>D</td><td>0</td><td></td><td></td></th0<></th0<>	Register 24	0x18	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0 0) (D	0		
Register 26 0x1A 0x0000 R/W 16 0x0000 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Register 25	0x19	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0 () (וו	0		
rgister Description	Register 26	0x1A	0x0000	RAV	16	0x0000	0	0	0	0	0	0	0	0	0	0	0	0	0 () (0	0 💌		
	ister Description																							
DC_RES[1:0] Block Address Value Resolution Block Address Val	C_RES[1:0] ese bits control the ADC	resolution.																Bl	ock A	FE5	832	2_ADC	Address	Value read Cota

Figure 59. AFE5832: Register Map Configuration: Manual Data Entry



Appendix C SLOU489–August 2017

Hardware Configuration

C.1 EVM Headers, Test Points, and Configuration

This section describes the functions of the headers on the EVM. It also provides a list of test points on the EVM that are useful for debug and general-use purposes.

C.1.1 EVM Header Configuration

The AFE5832 EVM is flexible in its configurability through the use of 2- and 3-pin headers. The default configuration of the EVM is set to facilitate initial testing, requiring minimal bench equipment. Figure 60 shows the default positions of all headers.



Figure 60. Default Jumper Positions

 Table 1 lists the default header configurations and descriptions.

Jumper	Circuit	Description	Pin Numbers	Selection
J63	Power Supply	±5V Input Power Connector	-	-
J64	USB/SPI	SPI Signals Probe Point	-	-
J35	PDN	PDN_Global	-	-
J36	PDN	PDN_Fast	-	-
J41	ADC Clock	OSC1 Xtal Power supply +3.3VD	-	3.3V
J42	ADC Clock	Clk source selector for SE Xtal or Diff	2-4,1-3	Differential
J40	ADC Clock	Diff CLK Source selector, Ext Xfmr or LMK	3-5, 4-6	LMK CLK
J44	CW CLK	16x CLK Source Selector	3-5, 4-6	Ext
J45	CW CLK	1x CLK Source Selector	3-5, 4-6	Ext
J50	DTGC	DTGC Digital Input Signals	-	-
J49	DTGC	GND for Dig Input Signals	-	-
J60	DTGC	CPLD JTAG Programming Header	-	-
J58	DTGC	CPLD GPIO	-	-
J55	LMK	LMK Chip Reset	1-2	-
J53	LMK	LMK Supply for 125M Xtal	1-2	-
J57	LMK	Power Supply for 40 MHz VCO	1-2	3.3V
J54	LMK	Input Clk selector for Clkin1	1-2	125 MHz Xtal
J38	LNA TR Enable	TR_EN 1-4	-	-

C.1.2 EVM Testpoints

Table 2 lists all test points on the AFE5832 EVM and their purposes.

Table	2.	EVM	Rev. A	Test	points
	_				

Testpoint	Circuit	Label	Testpoint Description
TP62-65, 69	GND	GND	Digital Ground Reference for EVM
TP31, 32	GND	AGND	Input Signal Ground Reference for EVM
TP66	GND	DGND	USB Ground Reference for EVM
T53	Power Supply	+5V_IN	+5V_IN
T54	Power Supply	-5V_IN	-5-V supply for Op-Amp circuitry
T59	Power Supply	+1.8 VD	AFE 1.8-V supply
TP67	Power Supply	OPAMP-	-5-V Supply for Op Amp circuitry
TP58	Power Supply	3.3 VD	+3.3 VA
TP56	Power Supply	AVDD_3.15	AFE analog supply for 3.15 V
TP68	Power Supply	ODAMP+	+5-V Supply for Op Amp circuitry
TP57	Power Supply	AVDD_1.9	AFE analog supply for 1.9-V
TP60	Power Supply	+5V_SRC	+5-V source for entire EVM
TP61	Power Supply	-5VSS	-5V Supply for CW Op Amp circuitry
TP1-30, 33, 34	Analog Inputs	SMA_INPx	Analog Input Channel 1-32
TP35	External Trigger	TX_TRG	TX_Trig input
TP38	DTGC	None	Ext TGC_Profile2 Input
TP36	DTGC	None	Ext TGC_Profile1 Input
TP37	DTGC	TGC_SLP	Ext TGC_Slope
TP39	DTGC	TGC_UD	Ext TGC_Up/Down
TP40,41	LMK Clock Circuit	CP1,CP2	LMK Output CP1,CP2
TP42	LMK Clock Circuit	None	None
TP43	LMK Clock Circuit	None	None
TP44	LMK Clock Circuit	None	LMK ADC Clock to Dut P/N
TP45	LMK Clock Circuit	None	None
TP47	LMK Clock Circuit	FPGA_CLK_OUT_P	LMK ADC CLK to FPGA P

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Testpoint	Circuit	Label	Testpoint Description
TP48	LMK Clock Circuit	None	LMK VCXO output
TP46	LMK Clock Circuit	None	LMK Clock to CPLD
TP49	IC 0.5-V Source Bias	None	SRC_BIASO
TP50	IC 2.5-V Bias	None	BIAS_2P5E
TP51	IC BandGap Bias	None	BAND_GAPE
TP52	IC LNA Bias	None	LNA_IN_CME

Table 2. EVM Rev. A Testpoints (continued)

C.1.3 ADC Clock Source Configuration

The AFE clock input can be driven differentially (sine wave, LVPECL, or LVDS) or single-ended (LVCMOS). The clock input of the device has an internal buffer and clock amplifier which is enabled or disabled automatically, depending on the type of clock provided (auto-detect feature). Therefore, the EVM allows for multiple clocking options.



Figure 61. EVM ADC Clock Source Configuration





Figure 62. AFE EVM ADC Clock Source Configuration Schematic





Configuration 1: Single-Ended On-Board XTAL OSC (LVDS Only)



Configuration 2: Differential Direct External Clock (LVDS Only)



Configuration 3: Differential Clock from the LMK04821 Clock Device

Figure 63. EVM ADC Clock Source Configuration Examples

Configuration 1: To use the onboard single-ended crystal oscillator as the clock source for the AFE, connect shunt jumpers for configuration 1 (as seen in Figure 63). Note: J41 powers the onboard oscillator with 3.3 V, due to the power limitations of the FXO-HC735-40 low-jitter crystal oscillator. The recommended ADC clock input for new designs is to use low-jitter square signals (LVCMOS levels, 1.8-V amplitude).

Configuration 2 (LVDS Only): To use a direct external clock as the clock source for the AFE, connect shunt jumpers for configuration 2 (as seen in Figure 63). Connect a single-ended external clock generator to SMA J39. Set the clock source to an appropriate frequency, such as 10 MHz to 100 MHz, and +13-dBm amplitude.

Configuration 3: To use the differential outputs from the LMK04821 as the clock source for the AFE, connect shunt jumpers for configuration 3 (as seen in Figure 63). The clock signal can be generated either from the 40-MHz onboard crystal (Y1), the 125-MHz onboard crystal (Y2), or an external clock generator. To use the 125-MHz onboard crystal, connect the J54 jumper as indicated by option 2 (Figure 63). To use the 40-MHz onboard crystal, connect the J54 jumper as indicated by option 1 (Figure 63). For an external source, connect an external clock generator to J56, and set the clock source to 160 MHz, and +13-dBm amplitude. For an external source, leave the J54 jumper as in configuration 2.

C.1.4 Complex Programmable Logic Device (CPLD)

The AFE5832 board has a XilinxTM CPLD, designated by U21 on the schematic. This CPLD is controlled by four switches contained in **S5** on the board. When all of these switches are in the 'off' position, LEDs D5 - D8 should light up on the board as shown in Figure 64.

	-
D100 R116	
D7 7 R117 R117	- S
D6R111 []	- Ci
05 I R110 R118	

Figure 64. CPLD Switches and LEDs

The following describes the function of each of the four switches contained in S5:

Switch 1: In the 'off' position, this switch turns on the TGC signals. In the 'on' position, these signals are turned off.

Switch 2: This switch determines whether the CPLD outputs signals for *Up-Down Ramp Mode* or *External Non-Uniform Mode* when running a DTGC test. In the 'off' position, the CPLD outputs for *Up-Down Ramp Mode*, and in the 'on' position, the CPLD outputs for *External Non-Uniform Mode*.

Switch 3: This switch controls the distance between two consecutive TGC_SLOPE pulses for *Up-Down Ramp Mode*.

Switch 4: This switch controls TX_TRIG. The TX_TRIG pulse resets the phase of the test pattern generator, the odd and even sampling phase selection, and the phase of the frame clock. This phase reset can corrupt the ADC data because the clock dividers will no longer be synchronized. In the 'off' position, *Switch 4* turns on the TX_TRIG pulse, and in the 'on' position, the TX_TRIG pulse is turned off.

The switches controlling the CPLD must be manipulated for some of the modes outlined in this user guide. Switch 4 is the most important to pay attention to as it controls whether or not the phase is reset. As a summary, the modes with their corresponding *Switch 4* settings are outlined in the following list:

- LVDS Capture Switch 4 off and LED D8 on
- DTGC Mode Test Switch 4 off and LED D8 on
- CW Mode Test Switch 4 on and LED D8 off



Appendix D SLOU489–August 2017

Triggering Options

D.1 ADC Synchronization and TX_TRIG

In the analog-front-end, 16 ADCs are being used to convert the 32 inputs. Each ADC converts one oddnumbered input and one even-numbered input. For example, ADC 1 converts inputs 1 and 2; ADC 2 converts inputs 3 and 4, and so forth. As two inputs need to be processed by each ADC, the inputs are alternately converted using two sampling circuits within each ADC.

The device has many PLLs and clock dividers that can synchronize the various test patterns generated. The device has a TX_TRIG input that is used to synchronize the clock dividers inside the device, and this enables multiple parallel devices to be synchronized as well. This TX_TRIG signal provides the means to determine when the odd and even signals should be sampled with respect to the rest of the system and its clock.

Refer to the ADC Synchronization Using TX_TRIG and Input Multiplexer and Sampler sections in the AFE5832 data sheet (SBAS823) for more information.

D.2 Software Trigger

One method of triggering the TSW EVM, AFE EVM as well as other bench equipment such as function generators is to generate the trigger from the TSW EVM itself. This requires a feedback loop from the TSW trigger output to the TSW trigger input using a short SMA cable. Secondly, a second trigger output from the TSW board can be routed to the AFE EVM, if needed, or to external bench equipment such as a function generator. See the TSW or HSDC Pro manual for more information.



Figure 65. HSDC Pro Trigger Configuration for SW





rigg	er Option	
	🔽 Trigger mode en	able
	Software Trigger	enable
	🔲 Arm on next cap	ture button press
	0 Trigger CLK	Delays
-		
2	ок 🍊	Cancel

Figure 66. HSDC Pro Trigger Configuration for SW Trigger

D.3 External Trigger

Another method of triggering the TSW EVM and AFE EVM as well as other bench equipment such as function generators is to generate the trigger from a bench trigger source such as the function generator. This requires feeding the trigger source to the TSW trigger input using an SMA cable. Secondly, a second trigger output from the trigger source can be routed to the AFE EVM, if needed. See the TSW or HSDC Pro manual for more information.



Figure 67. HSDC Pro Trigger Configuration for HW



🚺 Trigger Option	8
Trigger Option	
 Trigger mode ena Software Trigger e Arm on next capte Trigger CLK I 	ble enable ure button press Delays
🔊 ок	Cancel

Figure 68. HSDC Pro Trigger Configuration for HW External Trigger



Appendix E SLOU489–August 2017

Common Hardware Modifications

E.1 External SPI Programming

The AFE EVM allows for external access to the SPI bus for the AFE only, not the LMK device. This is done by connecting SPI signals at J64 and removing R140 near U14 on the bottom side of the board.



Hardware Reference

F.1 AFE5832 EVM Hardware Overview

The following images give an overview illustration of the EVM hardware.



Figure 69. AFE5832 EVM Block Diagram



F.2 AFE5832 EVM Schematic

Figure 70 through Figure 81 illustrate the EVM schematics.



Figure 70. AFE5832 Rev. A EVM Schematic 1 of 12



DTGC CPLD







ADC LVDS OUTPUT 9



Figure 72. AFE5832 Rev. A EVM Schematic 3 of 12



INM11 521

INM2

0.01µF INM1

C6 0.01µF INM3

C10 || 0.01µF ||NM5

C14 0.01µF INM7

C15 0.01µF INM8

C17 0.01µF INM9

C20 0.01µF INM10

C21 0.01µF INM11

C25 0.01µF INM13

C28 0.01µF INM14

C30 0.01µF INM15

C34 0.01µF INM17

C36 0.01µF INM18

C38 0.01µF INM19

C44 0.01µF INM22

C46 0.01µF INM23

C48 0.01µF INM24

C50 0.01µF INM25

C52 0.01µF INM26

C54 0.01µF INM27

C58 0.01µF INM29

C59 0.01µF INM30

C61 0.01µF INM31

C63 0.01µF INM32

C56 0.01µF INM28

C40 0.01µF

C42 0.01µF INM21

INM12

C24 0.01µF

C11 0.01µF INM6

INP[1..32] INP[1..32]

49.9 SMA INP1 C1 0.01µF INP1

49.9 SMA_INP2 C3 1 0.01µF INP2

SMA INP3 C5 || 0.01µF

49.9 SMA INP4 C7 11 0.01µF INP4

49.9 SMA INPS C9 11 0.01µF INPS

49.9 SMA_INP7 C13 0.01µF INP7

49.9 SMA INP8 C16 0.01µF INP8

49.9 SMA_INP9 C18 0.01µF INP9

10 ... 49.9 SMA INP10 C19 1 0.01µF INP10

11 49.9 SMA_INP11 C22 0.01µF INP11

12 49.9 SMA INP12 C23 0.01µF INP12

R13 49.9 SMA INP13 C26 0.01µF INP13

R14 49.9 SMA INP14 C27 0.01µF INP14

R15, 49.9 SMA INP15 C29 0.01µF INP15

R16 49.9 SMA INP16 C31 0.01µF INP16

R17 49.9 SMA INP17 C33 0.01µF INP17

R18 49.9 SMA INP18 C35 0.01µF INP18

R19 49.9 SMA INP19 C37 0.01µF INP19

R20 49.9 SMA_INP20 C39 0.01µF INP20

R21 49.9 SMA INP21 C41 0.01µF INP21

R22 49.9 SMA INP22 C43 0.01µF INP22

 R23
 49.9
 SMA INP23
 C45
 0.01µF
 INP23

 R24
 49.9
 SMA INP24
 C47
 0.01µF
 INP24

R25 49.9 SMA INP25 C49 0.01µF INP25

R26 49.9 SMA_INP26 C51 0.01µF INP26

R27 49.9 SMA INP27 C53 0.01µF INP27

R28 ... 49.9 SMA_INP28 C55 1 0.01µF INP28

R31 49.9 SMA INP31 C62 0.01µF INP31

49.9 SMA_INP32 C64 0.01µF INP32

49.9

INP29 C57 0.01µF

INP30 C60 0.01µF INP30

SMA_INP6_C12_0.01µF_INP6

MHR009 ANALOG INPUTS













CW I/V OUTPUT 3















Figure 76. AFE5832 Rev. A EVM Schematic 7 of 12















Figure 78. AFE5832 Rev. A EVM Schematic 9 of 12



MHR009 pin configuration



Figure 79. AFE5832 Rev. A EVM Schematic 10 of 12





Figure 80. AFE5832 Rev. A EVM Schematic 11 of 12









Figure 81. AFE5832 Rev. A EVM Schematic 12 of 12



F.3 EVM Bill of Materials

Table 3 lists the AFE5832 EVM bill of materials (BOM).

Table 3. AFE5832 EVM Bill of Materials ⁽¹⁾

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
$\begin{array}{c} C1, C2, C3, C4,\\ C5, C6, C7, C8,\\ C9, C10, C11,\\ C12, C13, C14,\\ C15, C16, C17,\\ C18, C19, C20,\\ C21, C22, C23,\\ C24, C25, C26,\\ C27, C28, C29,\\ C30, C31, C32,\\ C33, C34, C35,\\ C36, C37, C38,\\ C39, C40, C41,\\ C42, C43, C44,\\ C45, C46, C47,\\ C48, C49, C50,\\ C51, C52, C53,\\ C54, C55, C56,\\ C57, C58, C59,\\ C60, C61, C62,\\ C63, C64\\ \end{array}$	64	0.01 µF	CAP, CERM, 0.01 μF, 6.3 V, +/- 10%, X7R, 0402	0402	GRM155R70J103K A01D	MuRata		

⁽¹⁾ Unless otherwise noted in the Alternate Part Number or Alternate Manufacturer columns, all parts may be substituted with equivalents.



EVM Bill of Materials

www.ti.com

Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C90, C91, C92, C93, C94, C95, C96, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124, C125, C126, C132, C136, C139, C141, C142, C143, C144, C146, C147, C148, C149, C150, C151, C155, C157, C162, C167, C168, C169, C170, C171, C172, C210, C211, C212, C213, C214, C217, C218, C219, C220, C230, C233, C235, C237, C239, C249, C252, C253, C266, C264, C265, C266	107	0.1µF	CAP, CERM, 0.1 μF, 16 V, +/- 10%, X7R, 0402	0402	GRM155R71C104 KA88D	MuRata		
C75	1	10µF	CAP, CERM, 10 μF, 6.3 V, +80/- 20%, Y5V, 0805_140	0805_140	GRM21BF50J106Z E01L	MuRata		
C97	1	10µF	CAP, CERM, 10 µF, 6.3 V, +/- 20%, X5R, 0603	0603	C0603C106M9PA CTU	Kemet		
C98, C231, C232	3	1000pF	CAP, CERM, 1000 pF, 6.3 V,+/- 10%, X5R, 0402	0402	GRM155R60J102K A01D	MuRata		

Table 3. AFE5832 EVM Bill of Materials ⁽¹⁾ (continued)


Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
C127, C129, C159	3	10pF	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0402	0402	GRM1555C1H100J A01D	MuRata		
C131	1	0.68µF	CAP, CERM, 0.68 μF, 10 V, +/- 10%, X5R, 0603	0603	C0603C684K8PAC TU	Kemet		
C133	1	47pF	CAP, CERM, 47 pF, 100 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C2A470J A01D	MuRata		
C134	1	3900pF	CAP, CERM, 3900 pF, 50 V, +/- 10%, X7R, 0402	0402	GRM155R71H392 KA01D	MuRata		
C135, C138, C145, C153	4	10µF	CAP, CERM, 10 μF, 6.3 V, +/- 20%, X5R, 0603	0603	GRM188R60J106 ME47D	MuRata		
C137, C140, C154, C161	4	100pF	CAP, CERM, 100 pF, 50 V, +/- 10%, X7R, 0402	0402	CC0402KRX7R9B B101	Yageo America		
C152	1	0.1µF	CAP, CERM, 0.1 μF, 25 V, +/- 5%, X7R, 0603	0603	06033C104JAT2A	AVX		
C158	1	0.01µF	CAP, CERM, 0.01 μF, 16 V,+/- 10%, X5R, 0402	0402	GRM155R61C103 KA01D	MuRata		
C160	1	2200pF	CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R, 0402	0402	GRM155R71H222 KA01D	MuRata		
C173, C174, C175, C176, C177, C178, C179, C180	8	1µF	CAP, CERM, 1 μF, 6.3 V, +/- 20%, X5R, 0402	0402	GRM152R60J105 ME15D	MuRata		
C181, C182, C184, C186, C189, C190, C192, C195, C198, C200, C201, C205, C208	13	0.1µF	CAP, CERM, 0.1µF, 16V, +/- 10%, X5R, 0603	0603	GRM188R61C104 KA01D	MuRata		
C183, C187, C191, C196, C202, C206	6	22µF	CAP, CERM, 22 μF, 10 V,+/- 20%, X5R, 0603	0603	GRM187R61A226 ME15D	MuRata		
C185, C188, C194, C197, C199, C204, C207	7	22µF	CAP, CERM, 22 μF, 16 V, +/- 20%, X5R, 1206	1206	1206YD226MAT2A	AVX		



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Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
C193	1	470pF	CAP, CERM, 470pF, 50V, +/-5%, C0G/NP0, 0603	0603	06035A471JAT2A	AVX		
C203	1	15pF	CAP, CERM, 15 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	06035A150JAT2A	AVX		
C209	1	270pF	CAP, CERM, 270 pF, 50 V, +/- 10%, X7R, 0603	0603	GRM188R71H271 KA01D	MuRata		
C215, C216	2	47pF	CAP, CERM, 47 pF, 50 V, +/- 1%, C0G/NP0, 0402	0402	GRM1555C1H470 FA01D	MuRata		
C221, C222, C226, C228, C240, C241, C245, C246	8	0.015µF	CAP, CERM, 0.015 μF, 16 V,+/- 5%, X7R, 0402	0402	GRM155R71C153J A01D	MuRata		
C223, C224, C225, C242, C243, C244	6	4.7µF	CAP, CERM, 4.7 μF, 10 V, +/- 10%, X5R, 0603	0603	C0603C475K8PAC TU	Kemet		
C229, C234, C236, C238, C250, C251, C254, C255	8	1µF	CAP, CERM, 1 μF, 16 V, +/- 10%, X5R, 0603	0603	C0603C105K4PAC TU	Kemet		
D1, D2, D3, D4	4	Green	LED, Green, SMD	1.6x0.8x0.8mm	LTST-C190KGKT	Lite-On		
D5, D6, D7, D8, D11, D12	6	Red	LED, Red, SMD	Red LED, 1.6x0.8x0.8mm	LTST-C190CKT	Lite-On		
D9, D10	2	Orange	LED, Orange, SMD	1.6x0.8x0.8mm	LTST-C190KFKT	Lite-On		
D13, D14	2	Blue	LED, Blue, SMD	BLUE 0603 LED	LB Q39G-L2N2-35- 1	OSRAM		
FB3	1	1000 Ω	Ferrite Bead, 1000 Ω @ 100 MHz, 0.3 A, 0402	0402	BLM15AG102SN1 D	MuRata		
FB4, FB5, FB6, FB7, FB8, FB9, FB12, FB14, FB15, FB16, FB17, FB18, FB19, FB20, FB21, FB22, FB23, FB24, FB25, FB26, FB27, FB28, FB29, FB30, FB31, FB32	26	120 Ω	Ferrite Bead, 120 Ω @ 100 MHz, 0.8 A, 0805	0805	BLM21AG121SN1 D	MuRata		
FB10, FB11	2	120 Ω	Ferrite Bead, 120 Ω @ 100 MHz, 4 A, 1206	1206	HI1206P121R-10	Laird-Signal Integrity Products		



Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
H1, H5, H8, H13, H16	5		HEX STANDOFF 4-40 ALUMINUM 1/2"	HEX STANDOFF 4-40 ALUMINUM 1/2"	2203	Keystone		
H2, H6, H9, H12, H15	5		HEX, M-F STANDOFF 4-40 ALUMINUM 5/8"	HEX, M-F STANDOFF 4-40 ALUMINUM 5/8"	8402	Keystone		
H3, H7, H10, H11, H14	5		MACHINE SCREW PAN PHILLIPS 4- 40	Machine Screw, 4- 40, 1/4"	PMSSS 440 0025 PH	B&F Fastener Supply		
H4	1		CABLE ASSY STR 2.1MM 6' 24 AWG		CA-2185	Tensility		
J1, J4, J8, J11, J14, J17, J21, J24, J27, J30	10		Connector, End launch SMA, 50 Ω , SMT	End Launch SMA	142-0701-801	Johnson		
J2, J3, J5, J6, J9, J10, J12, J13, J15, J16, J19, J20, J22, J23, J25, J26, J28, J29, J31, J32, J33, J34, J37, J39, J43, J46, J51, J52, J56, J59, J66, J68	32		SMA Straight PCB Socket Die Cast, 50 Ω, TH	SMA Straight PCB Socket Die Cast, TH	5-1814832-1	TE Connectivity		
J7, J18, J48	3		Socket, 0.5MM, 60x2, Gold, SMT	Socket, Female, 0.5MM, 60x2, SMT	QTH-060-01-L-D-A	Samtec		
J35, J36, J41, J53, J57	5		Header, 100mil, 2x1, Gold, TH	2x1 Header	TSW-102-07-G-S	Samtec		
J38, J60	2		Header, 100mil, 4x2, Gold, TH	4x2 Header	TSW-104-07-G-D	Samtec		
J40, J42, J44, J45	4		Header, TH, 100mil, 3x2, Gold plated, 230 mil above insulator	3x2 Header	TSW-103-07-G-D	Samtec		
J49, J50	2		Header, TH, 100mil, 4x1, Gold plated, 230 mil above insulator	4x1 Header	TSW-104-07-G-S	Samtec		
J54, J55, J63	3		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec		
J58	1		Header, 100mil, 6x1, Gold, TH	6x1 Header	TSW-106-07-G-S	Samtec		



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Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
J61	1		Power Jack, mini, 2.1mm OD, R/A, TH	Jack, 14.5x11x9mm	RAPC722X	Switchcraft		
J62	1		Terminal Block, 3.5mm Pitch, 3x1, TH	10.5x8.2x6.5mm	ED555/3DS	On-Shore Technology		
J65	1		Connector, Receptacle, USB - mini AB, R/A, SMD	Receptacle, 5- Leads, Body 9.9x9mm, R/A	67803-8020	Molex		
J67	1		Audio Jack, 3.5 mm, Stereo, R/A, TH	Connector, 3- Leads, 3.5mm Stereo Jack R/A, TH	STX-3000	Kycon Inc		
LBL1	1		Printed Circuit Board		MHR009	Any		
LBL2	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650≈ x 0.200"W	THT-14-423-10	Brady	-	-
R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R34, R38, R41, R43, R46, R47, R48, R52, R53, R87, R91, R143, R144, R145, R152, R153, R154	49	49.9	RES, 49.9, 1%, 0.063 W, 0402	0402	CRCW040249R9F KED	Vishay-Dale		
R36, R40, R50, R51, R60, R61, R70, R71, R72, R73, R88, R100, R103, R112, R139, R140, R158, R159, R164, R165, R167, R172, R175, R177	24	0	RES, 0, 5%, 0.063 W, 0402	0402	CRCW04020000Z0 ED	Vishay-Dale		



Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
R44, R45, R56, R57, R58, R59, R84, R105, R106, R107, R108, R109, R110, R111	14	100	RES, 100, 1%, 0.1 W, 0402	0402	ERJ-2RKF1000X	Panasonic		
R49	1	60.4k	RES, 60.4k Ω, 1%, 0.063W, 0402	0402	CRCW040260K4F KED	Vishay-Dale		
R62, R65	2	100	RES, 100, 1%, 0.1 W, 0603	0603	CRCW0603100RF KEA	Vishay-Dale		
R76	1	39k	RES, 39 k, 5%, 0.063 W, 0402	0402	CRCW040239K0J NED	Vishay-Dale		
R77	1	620	RES, 620, 5%, 0.063 W, 0402	0402	CRCW0402620RJ NED	Vishay-Dale		
R83	1	11	RES, 11, 5%, 0.063 W, 0402	0402	CRCW040211R0J NED	Vishay-Dale		
R85, R86	2	1.8k	RES, 1.8 k, 5%, 0.063 W, 0402	0402	CRCW04021K80J NED	Vishay-Dale		
R92, R93, R95, R97	4	750	RES, 750, 5%, 0.063 W, 0402	0402	CRCW0402750RJ NED	Vishay-Dale		
R114, R115, R116, R117, R118, R119, R120	7	10.0k	RES, 10.0 k, 1%, 0.1 W, 0603	0603	ERJ-3EKF1002V	Panasonic		
R121	1	0	RES, 0 Ω, 5%, 0.125W, 0805	0805	CRCW08050000Z0 EA	Vishay-Dale		
R122	1	30k	RES, 30k Ω, 5%, 0.125W, 0805	0805	CRCW080530K0J NEA	Vishay-Dale		
R123	1	47k	RES, 47 k, 5%, 0.1 W, 0603	0603	CRCW060347K0J NEA	Vishay-Dale		
R124	1	30.1k	RES, 30.1 k, 1%, 0.1 W, 0603	0603	CRCW060330K1F KEA	Vishay-Dale		
R125, R126, R127, R128, R129, R130	6	332	RES, 332, 1%, 0.063 W, 0402	0402	CRCW0402332RF KED	Vishay-Dale		
R131	1	1.65k	RES, 1.65 k, 1%, 0.1 W, 0603	0603	CRCW06031K65F KEA	Vishay-Dale		
R132	1	3.01k	RES, 3.01k Ω, 1%, 0.1W, 0603	0603	CRCW06033K01F KEA	Vishay-Dale		
R141, R142, R146, R147, R150, R151, R155, R156	8	499	RES, 499, 1%, 0.063 W, 0402	0402	CRCW0402499RF KED	Vishay-Dale		



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Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
R148, R171	2	3.30k	RES, 3.30 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF3301X	Panasonic		
R149, R174	2	4.70k	RES, 4.70 k, 1%, 0.1 W, 0402	0402	ERJ-2RKF4701X	Panasonic		
R161, R162, R169, R170	4	140k	RES, 140 k, 1%, 0.063 W, 0402	0402	CRCW0402140KF KED	Vishay-Dale		
R188, R189	2	0	RES, 0, 5%, 0.125 W, 0805	0805	MCR10EZPJ000	RΩ		
S1, S2, S3, S4, S6	5		Switch, push- button, SMD	2.9x2x3.9mm SMD	SKRKAEE010	Alps		
S5	1		Switch, SPST, 4 Pos, Top Actuated, SMD	SMD, 8-Leads, Pitch 1.27mm	1571983-5	TE Connectivity		
SH-1, SH-2, SH-3, SH-4, SH-5, SH-6	6	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec	969102-0000-DA	ЗМ
T1, T2, T3, T4, T5	5		RF Transformer, 50 Ω , 2 to 775 MHz, SMT	CD542	ADT4-1WT+	Minicircuits		
TP31, TP32, TP55, TP62, TP63, TP64, TP65, TP66, TP69	9	Black	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone		
TP35	1	Yellow	Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone		
TP36, TP37, TP38, TP39, TP49, TP50, TP51, TP52	8	Orange	Test Point, Miniature, Orange, TH	Orange Miniature Testpoint	5003	Keystone		
TP48	1	Blue	Test Point, Miniature, Blue, TH	Blue Miniature Testpoint	5117	Keystone		
TP53, TP56, TP57, TP58, TP59, TP60, TP68	7	Red	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone		
TP54, TP61, TP67	3	White	Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone		



Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
U1	1		32-Channel Ultrasound AFE with 41.5- mW/Channel Power, 1.5nV/vHz Noise, 12-Bit, 40- MSPS or 10-Bit, 50-MSPS output and Passive CW Mixer, ZBV0289A (NFBGA-289)	ZBV0289A	AFE5832ZBV	Texas Instruments		Texas Instruments
U2	1		CLOCK BUFFER WITH PROGRAMMABLE DIVIDER, LVPECL I/O + ADDITIONAL LVCMOS OUTPUT, RGT0016A	RGT0016A	CDCM1802RGTR	Texas Instruments	CDCM1802RGTT	Texas Instruments
U3	1		64K I2C Smart Serial EEPROM, SOIC-8	SOIC-8, 208mil wide	24LC65-I/SM	Microchip		
U4	1		Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner with Dual Loop PLLs, NKD0064A (WQFN-64)	NKD0064A	LMK04821NKDR	Texas Instruments	LMK04821NKDT	Texas Instruments
U5	1		Ultralow-Noise, High PSRR, Fast, RF, 1A Low- Dropout Linear Regulator, DCQ0006A	DCQ0006A	TPS79618DCQR	Texas Instruments		Texas Instruments
U6, U9	2		Single Output High PSRR LDO, 1 A, Fixed 3.3 V Output, 2.7 to 5.5 V Input, 6-pin SOT-223 (DCQ), -40 to 125 degC, Green (RoHS and no Sb/Br)	DCQ0006A	TPS79633DCQR	Texas Instruments	Equivalent	None



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Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
U7, U8, U10	3		Ultralow-Noise, High PSRR, Fast, RF, 1A, Low- Dropout Linear Regulator, DCQ0006A	DCQ0006A	TPS79601DCQR	Texas Instruments		Texas Instruments
U11	1		USB FIFO IC, 28SSOP	SSOP28	FT245RL	FTDI		
U12	1		4242-VPK Small- Footprint and Low- Power Quad Channels Digital Isolators, DBQ0016A	DBQ0016A	ISO7140CCDBQR	Texas Instruments	ISO7140CCDBQ	Texas Instruments
U13	1		6-BIT BIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR WITH AUTO- DIRECTION SENSING AND ±15-KV ESD PROTECTION, PW0016A	PW0016A	TXB0106PWR	Texas Instruments		Texas Instruments
U14	1		4242-VPK Small- Footprint and Low- Power Quad Channels Digital Isolators, DBQ0016A	DBQ0016A	ISO7141CCDBQR	Texas Instruments	ISO7141CCDBQ	Texas Instruments
U15, U16	2		HIGH-SPEED, LOW-NOISE, FULLY- DIFFERENTIAL I/O AMPLIFIERS, DGN0008D	DGN0008D	THS4131CDGNR	Texas Instruments	THS4131CDGN	Texas Instruments



Designator	Quantity	Value	Description	Package Reference	PartNumber	Manufacturer	Alternate Part Number	Alternate Manufacturer
U17, U18, U19, U20	4		Dual, High Gain Bandwidth, High Output Current, Operational Amplifier with Current Limit, 5 to 12 V, -40 to 85 degC, 8-pin SOIC (D8), Green (RoHS and no Sb/Br)	D0008A	OPA2614ID	Texas Instruments	Equivalent	Texas Instruments
U21	1		XC2C64A CoolRunner-II CPLD, QFG48	QFN-48	XC2C64A- 5QFG48C	Xilinx		
Y1	1		OSC, 3.3 V, 40 MHz, SMD	SMD, 4-Leads, Body 7x5mm	FXO-HC735-40	Fox Electronics		
Y2	1		OSC, 3.3 V, 125 MHz, 15 pF, SMD	7x5mm	VCC1-B3B- 125M000000	Vectron		
Y3	1		OSC, 40 MHz, 3.3V, SMD	7x5mm	ASVV-40.000MHZ- N102-T	Abracon Corportation		



Appendix G SLOU489–August 2017

FAQ and Troubleshooting

G.1 Common Issues

The following section illustrates some of the common problems seen when attempting to use the EVM hardware and software.

G.1.1 Issues

- Other Versions of Windows: Officially, the EVM software supports Windows 7 and Windows 10.
- Power supply capacity: It is likely that both the AFE EVM and the TSW EVM do not have a wall power supply. Instead, they include the ability to connect to a bench-top supply via the provided cable. It is critical that each of these EVMs has access to 2 A of current capacity.
- No Capture in HSDC Pro: It is possible that once the GUIs and EVMs are configured for capture, and the capture button in HSDC Pro is pressed, that nothing seems to happen and eventually the GUI will timeout and a pop-up an error appears as seen in Figure 82. Reasons for this can include the following:
 - Incorrect firmware loaded
 - Current starvation on at least one EVM, 2 A is sufficient
 - Missing Data output clock from the AFE to the FPGA. With LVDS, this could be the FCLK or DCLK.
 D5 of the TSW1400 should turn on, and if not, this is probably the reason.
 - · Verify that the EVMs are mechanically mated correctly
 - Verify power supply to both EVMs
 - Verify jumper settings on the AFE EVM. Particularly inspect J54, J53, J57, J41, J40 and J42.
 - Use an oscilloscope to test the frequency of the clock at header J40 or J42. This should be 40-MHz.
- Even-odd channel swap observed with LVDS capture: Make sure that Switch 4 in S5 is in the "off" position with LED D8 on. Ensure that there is no SMA cable connected to J37 on the AFE5832EVM before retrying capture in HSDC Pro.



Figure 82. Read DDR Error for No Capture

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