

**Buttons, Switches,
LEDs**
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DDR III
SHEET 3

FMC CONN
SHEET 4

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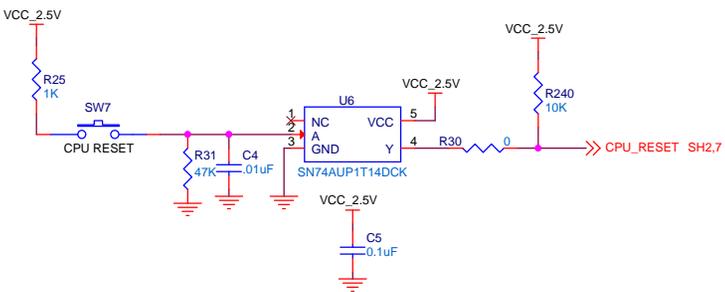
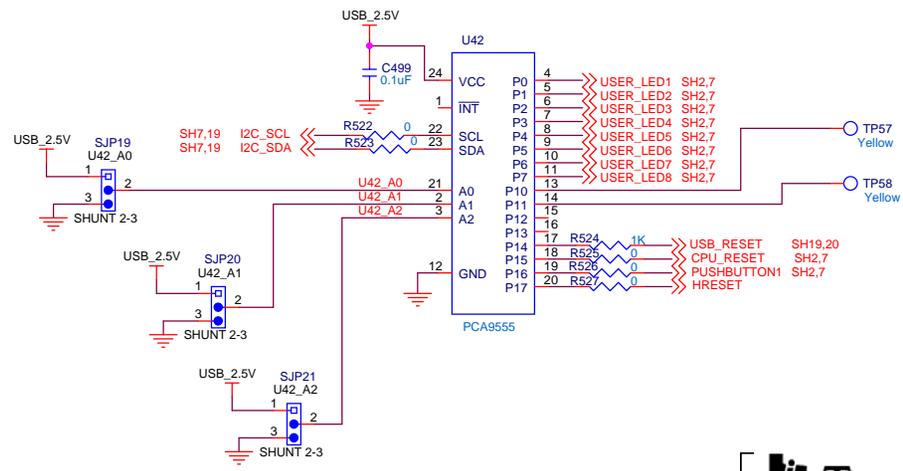
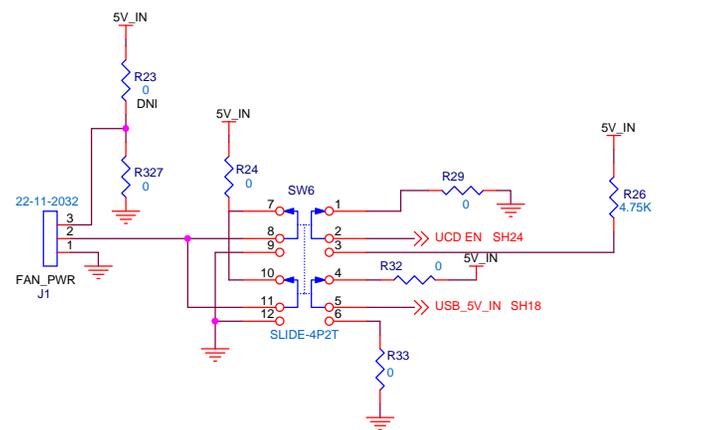
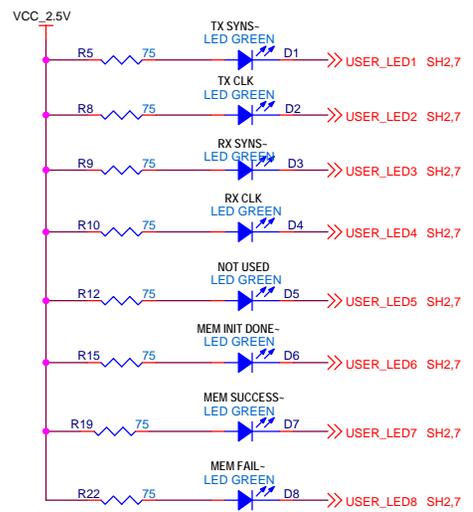
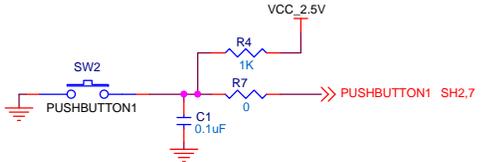
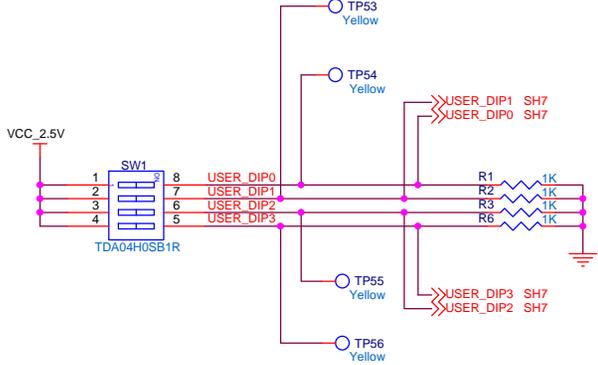
NOTE: DNI = DO NOT INSTALL COMPONENT.



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Engineer: J. SETON / E. DWOBENG	Date: Friday, March 11, 2016	Rev E

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Buttons, Switches, LEDs

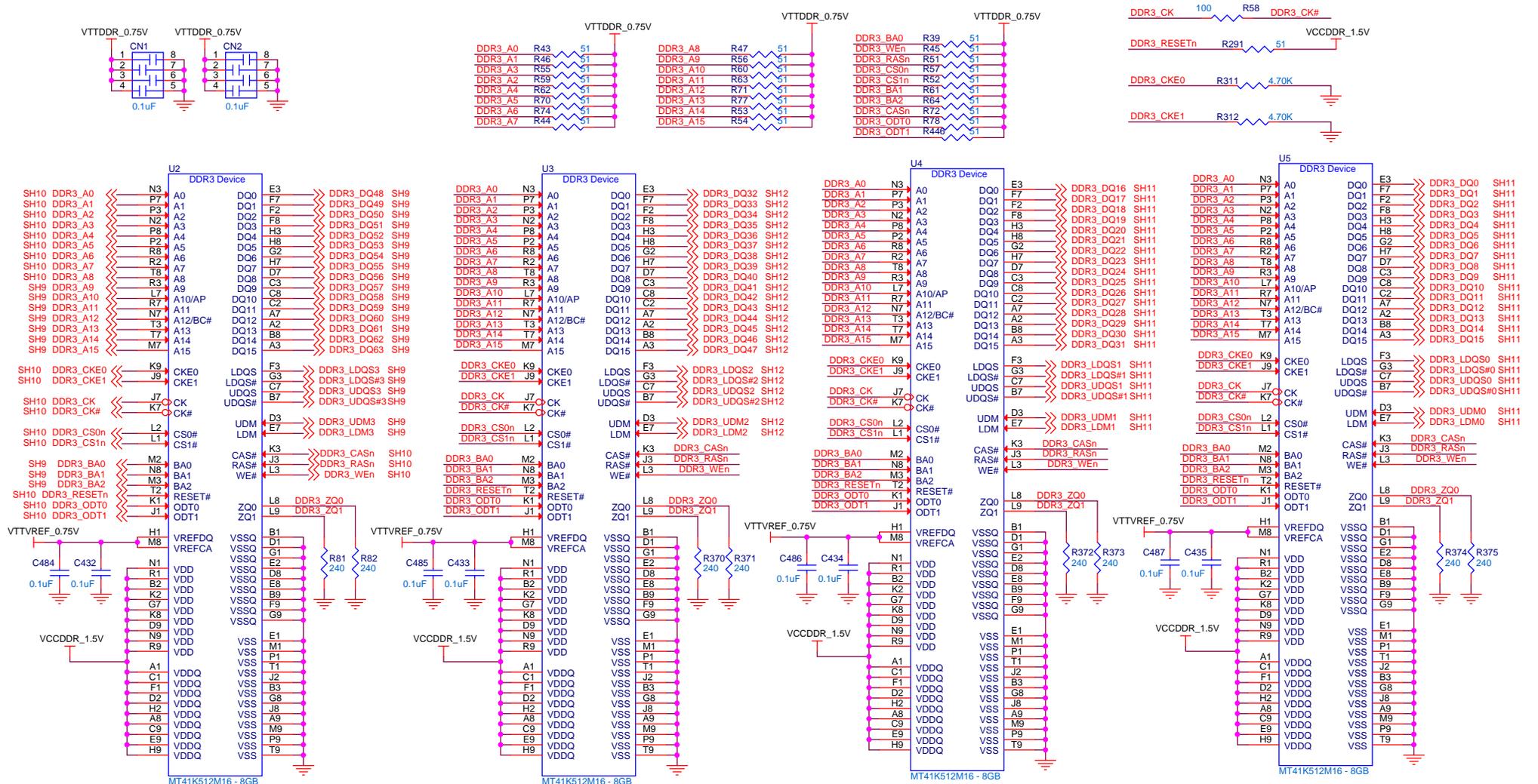


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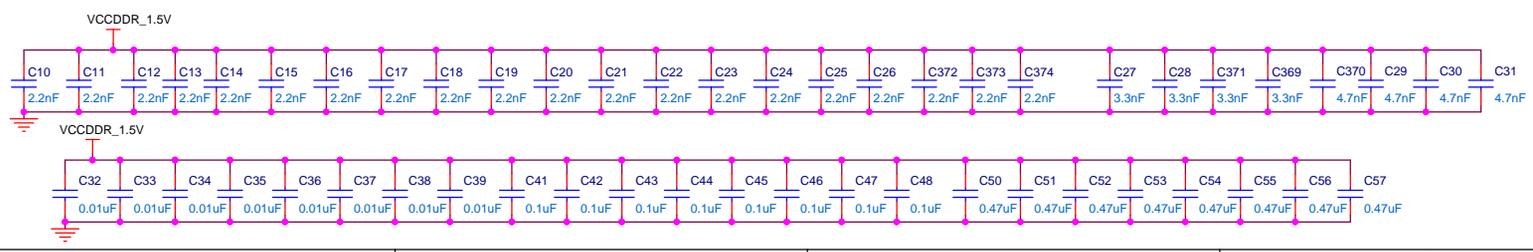
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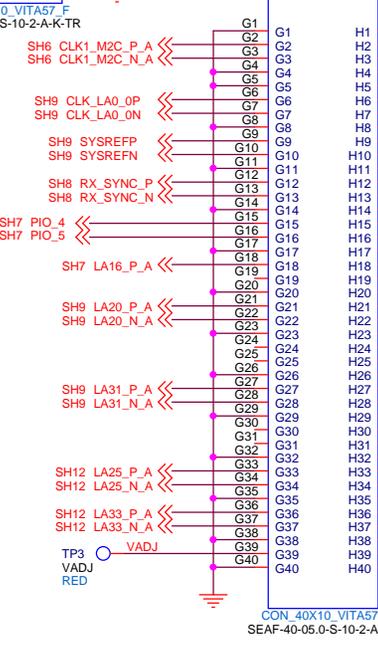
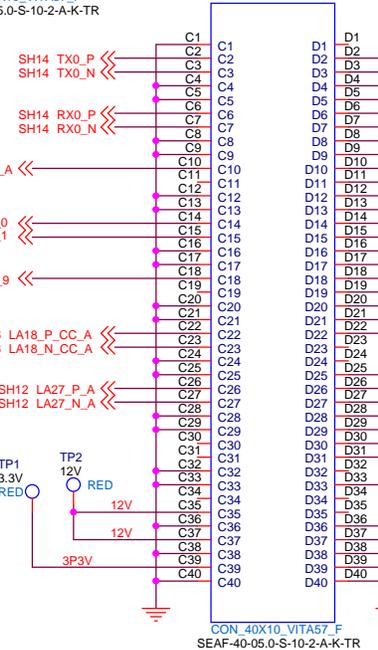
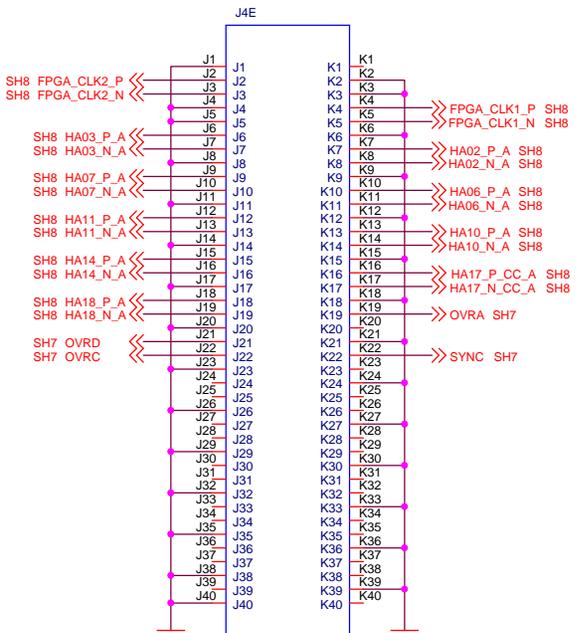
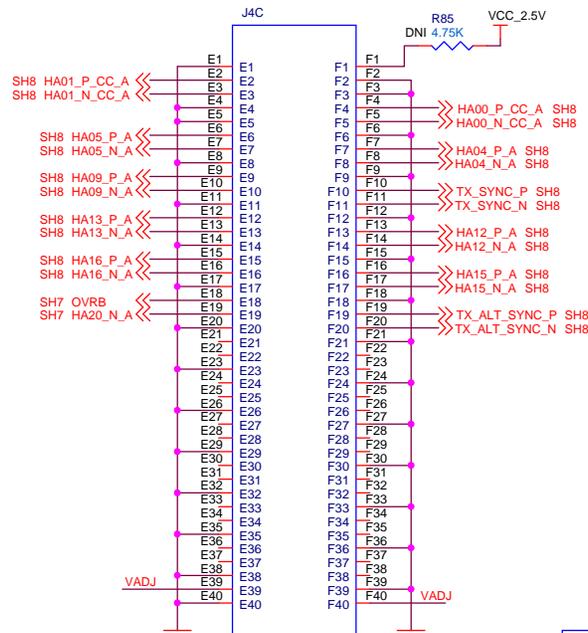
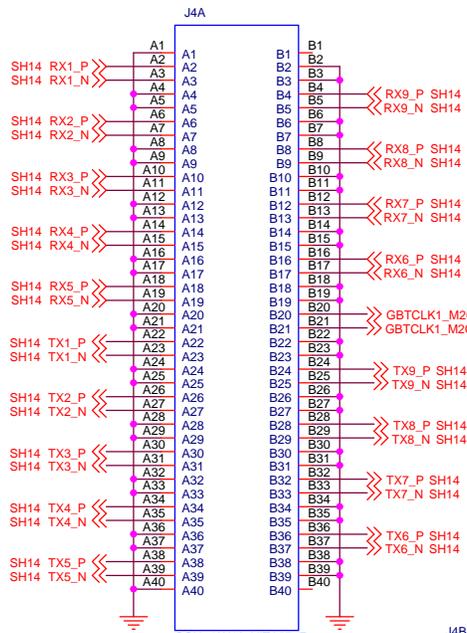


DDR III
Uses Soft Controller

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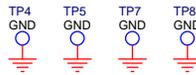
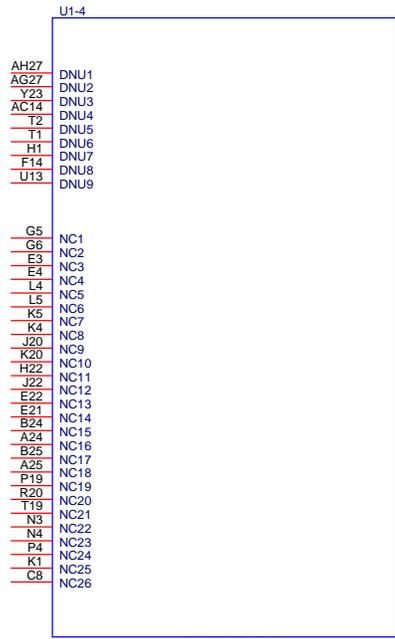


FPGA=CARRIER
DUT=MEZ
M2C - ADC
C2M - DAC

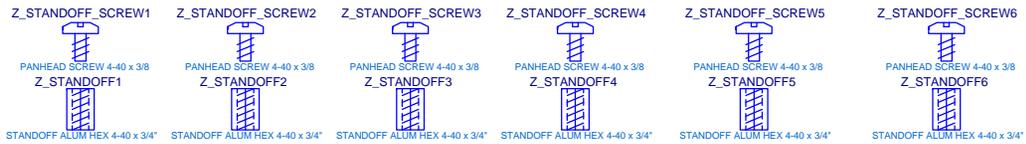
FMC HPC CONNECTOR



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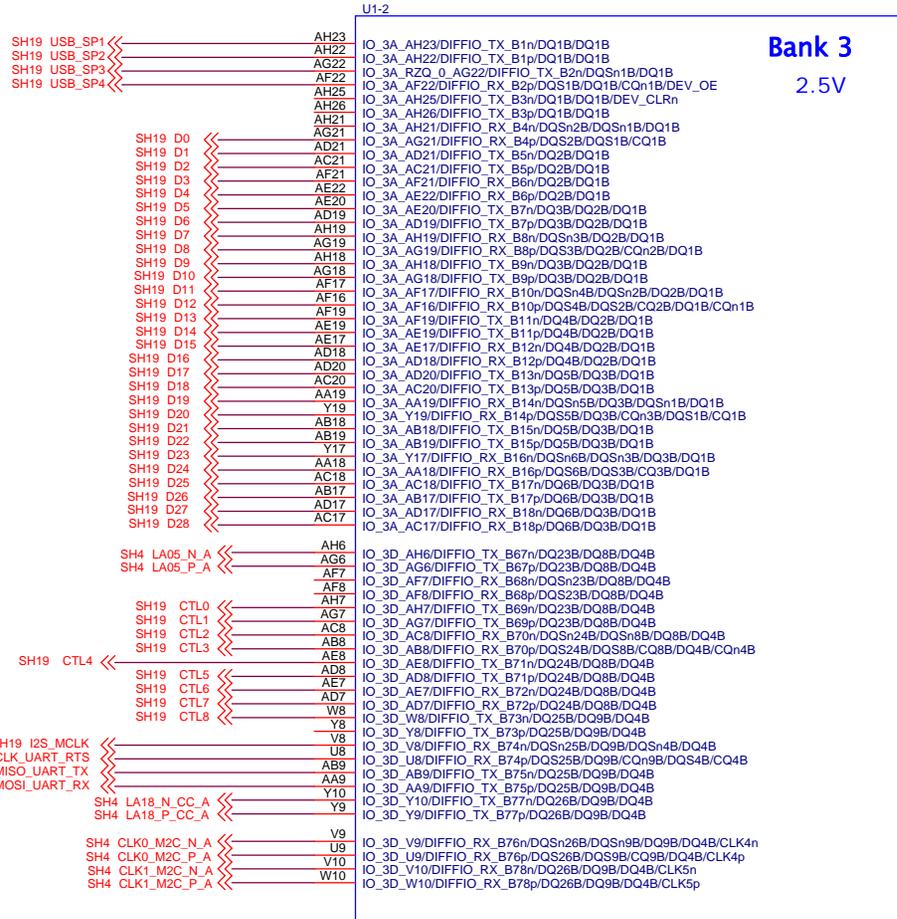
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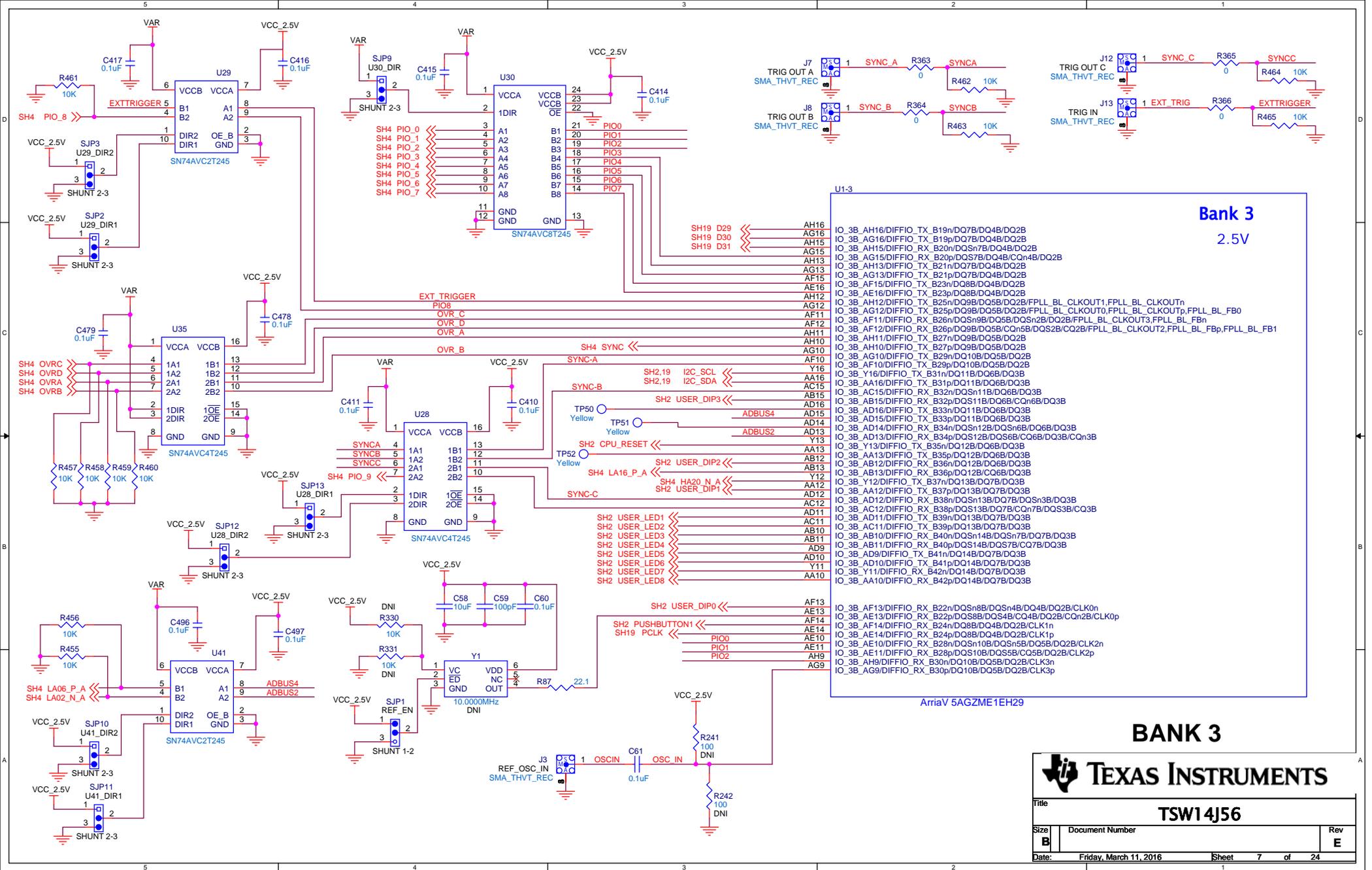
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BANK 3



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Bank 3
2.5V

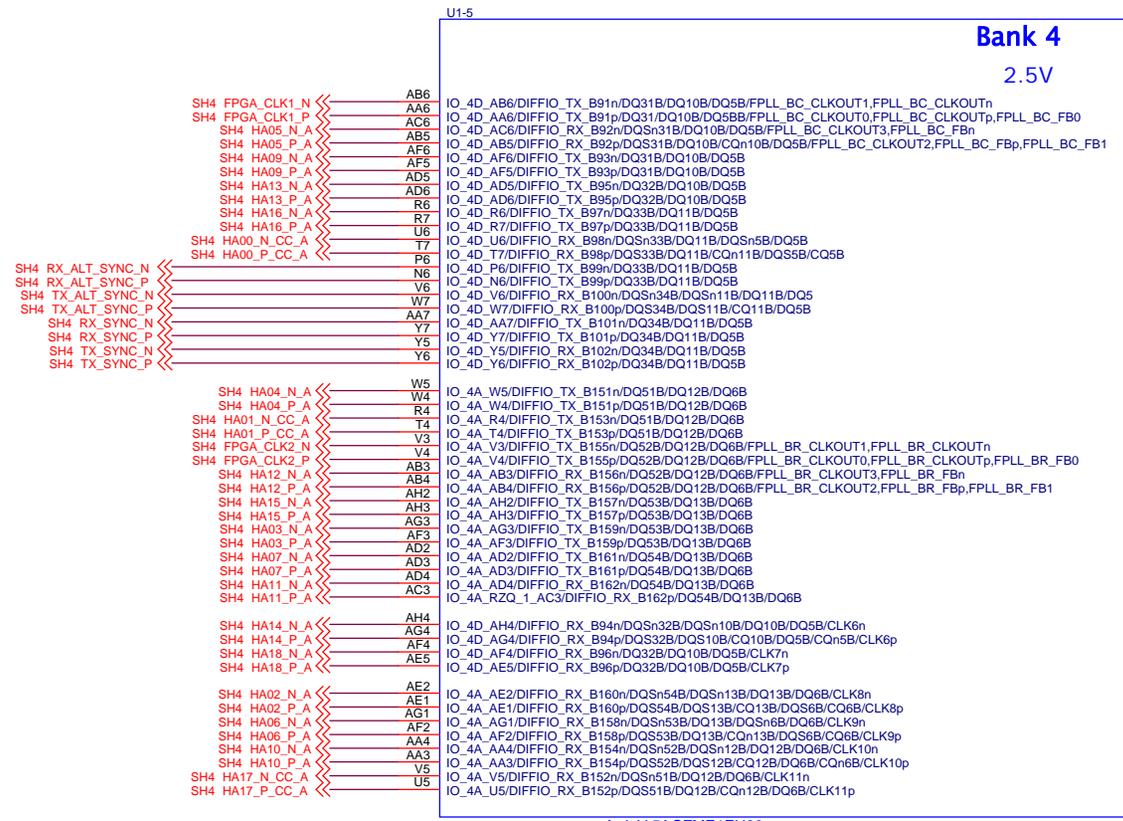
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BANK 3

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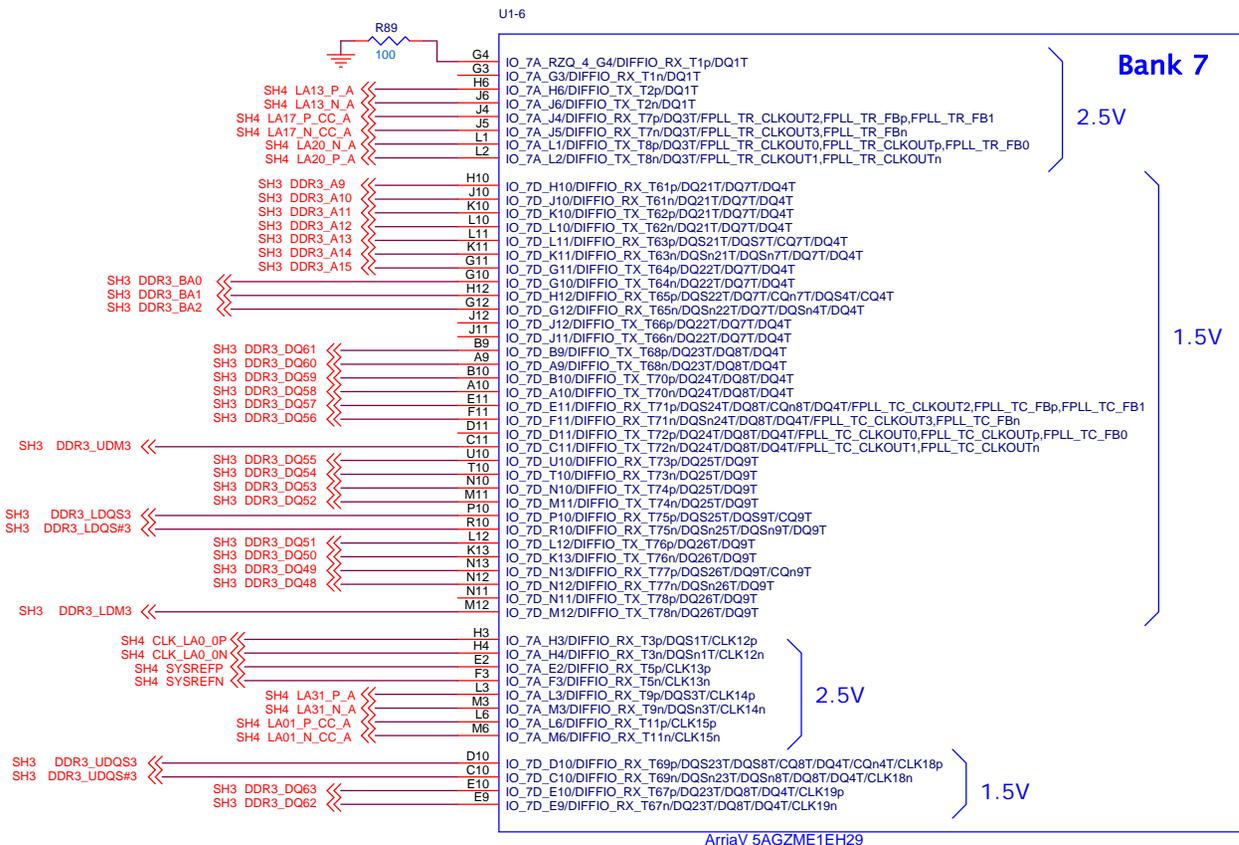


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FPGA Bank 4

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FPGA Bank 7

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1.5V

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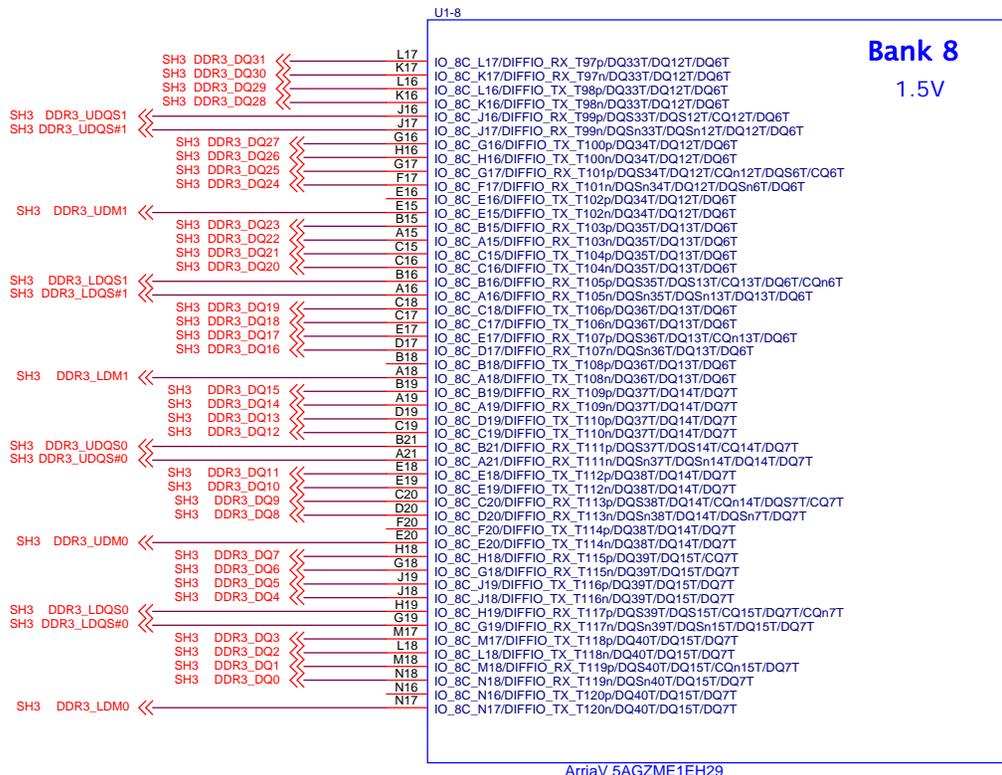
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SH3	DDR3_ODT1	<<	E7
SH3	DDR3_CKE0	<<	E6
SH3	DDR3_CKE1	<<	D7
SH3	DDR3_CK	<<	D8
SH3	DDR3_CK#	<<	M8
SH3	DDR3_CS0n	<<	L8
SH3	DDR3_CS1n	<<	M9
SH3	DDR3_RESEtN	<<	L9
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SH3	DDR3_A2	<<	R8
SH3	DDR3_A3	<<	P7
SH3	DDR3_A4	<<	P9
SH3	DDR3_A5	<<	N9
SH3	DDR3_A6	<<	T8
SH3	DDR3_A7	<<	R9
SH3	DDR3_A8	<<	R9

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BANK 7



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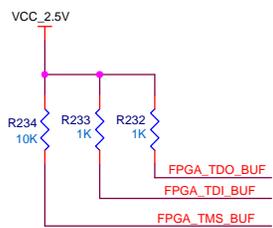
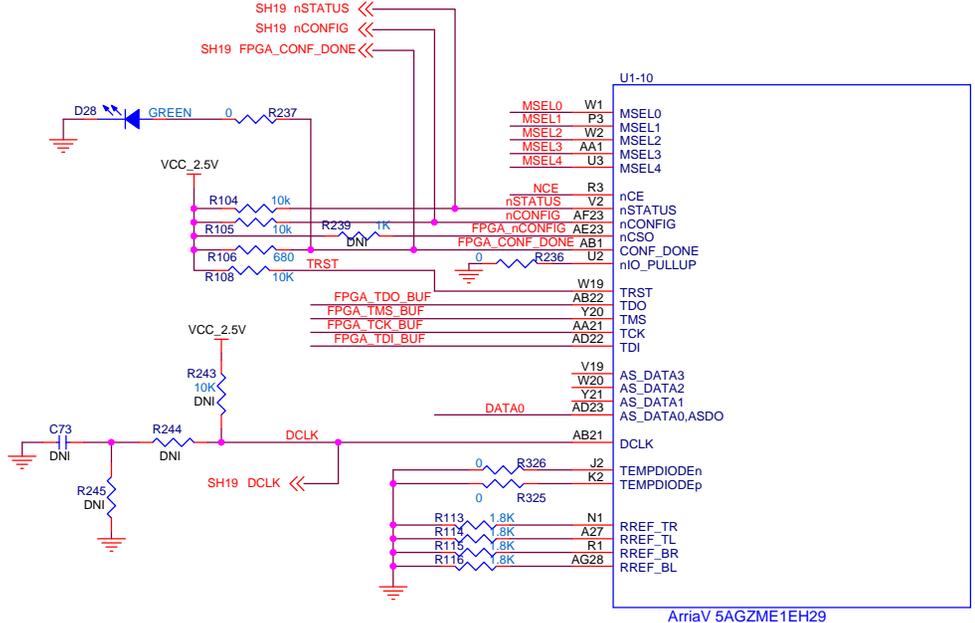
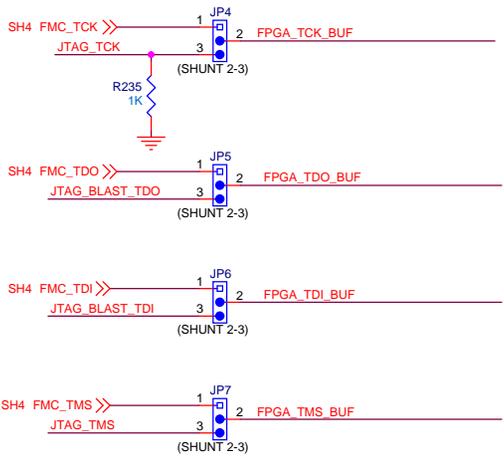
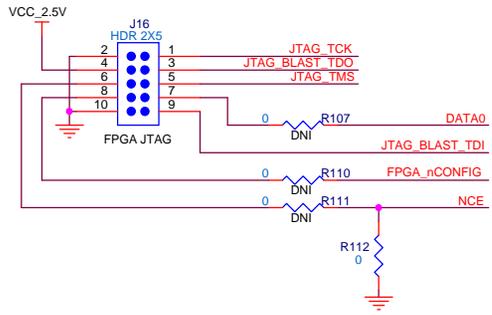
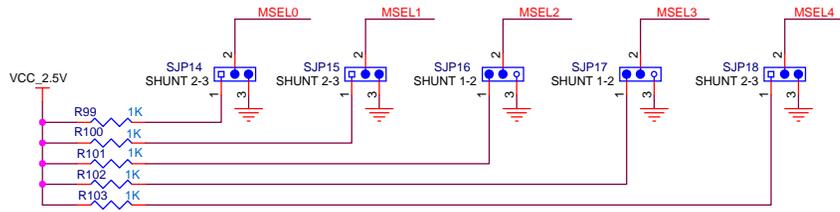


BANK 8

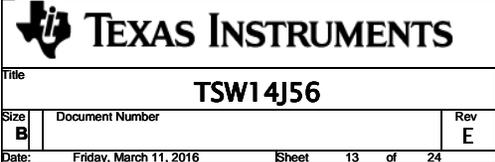
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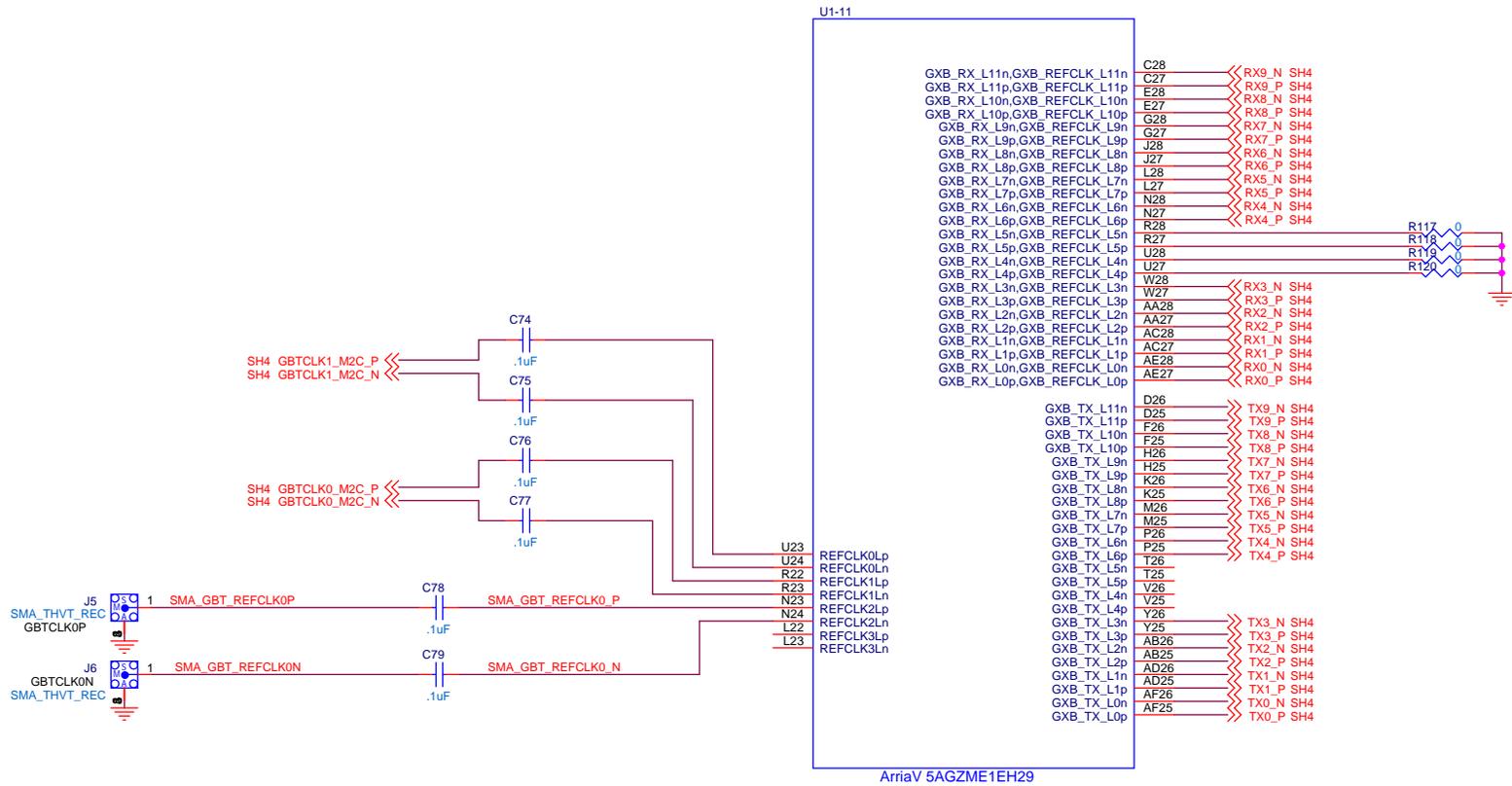
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FPGA CONFIGURATION



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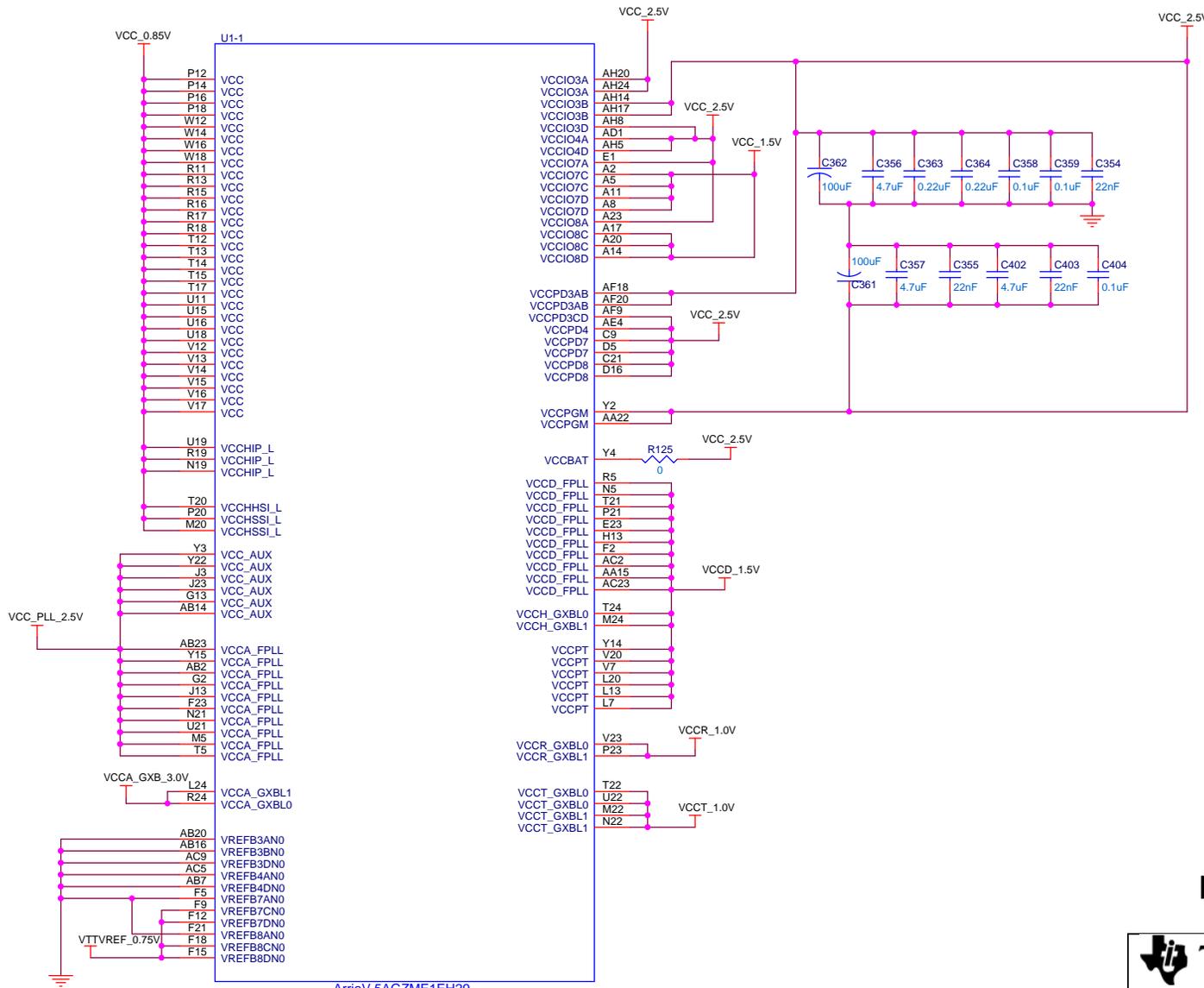
HIGH SPEED BANK

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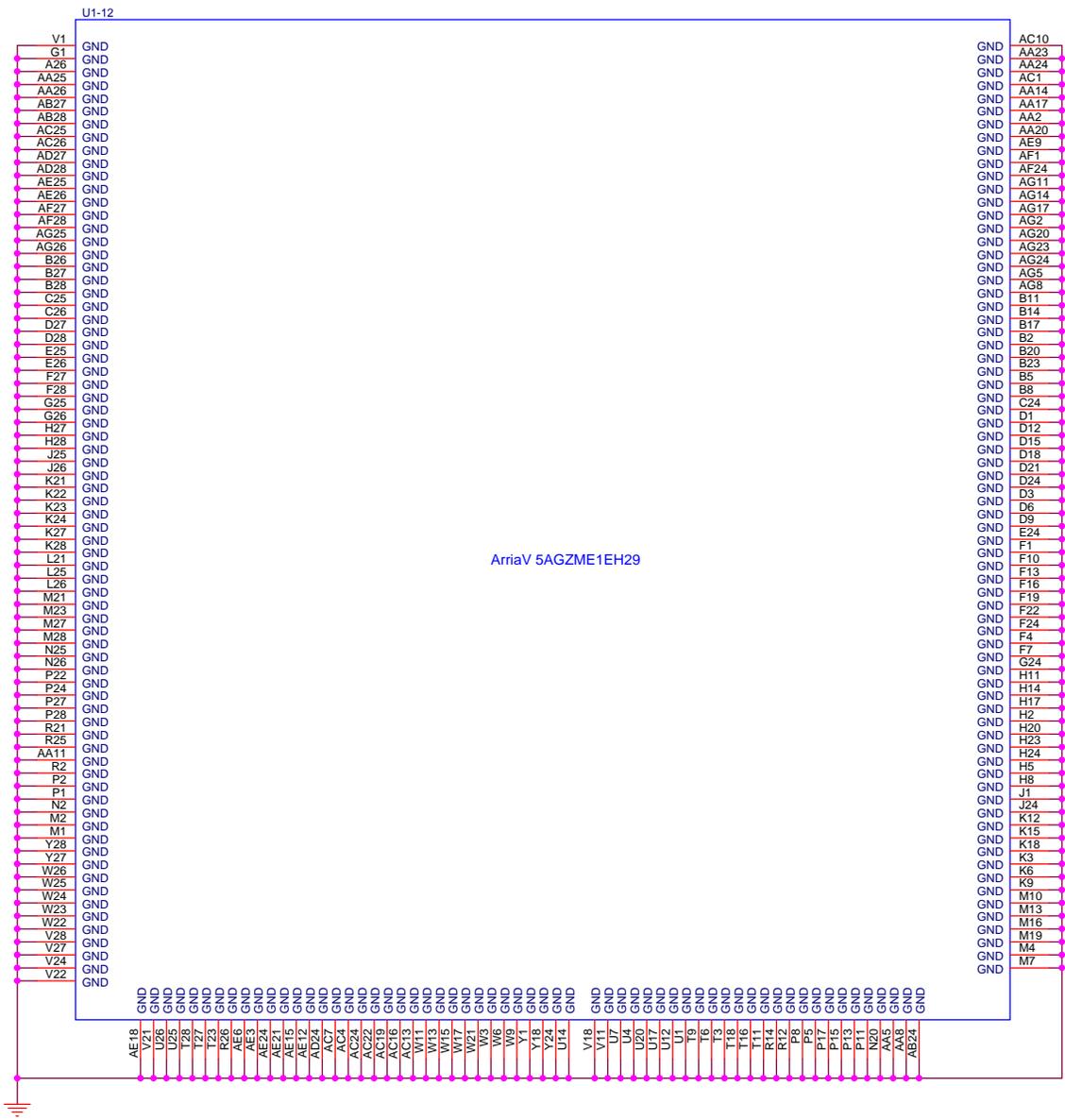


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FPGA POWER



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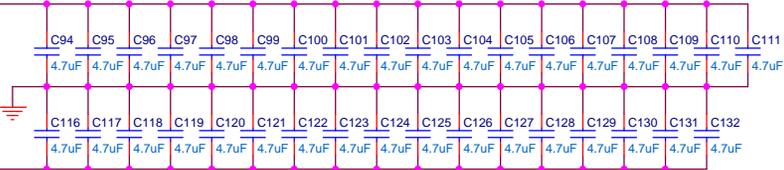
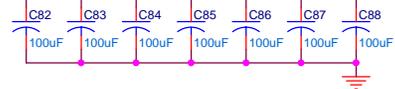
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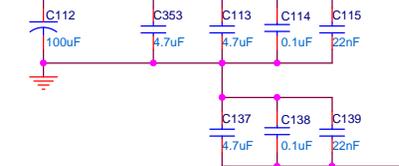
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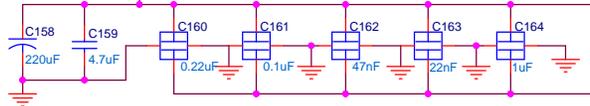
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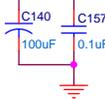
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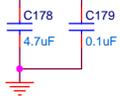
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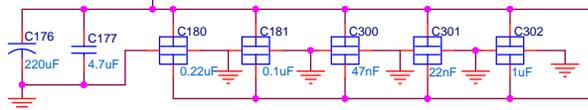
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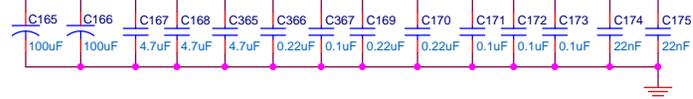
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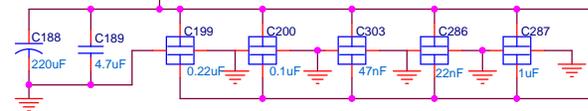
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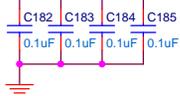
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VCCT_1.0V



VTTVREF_0.75V



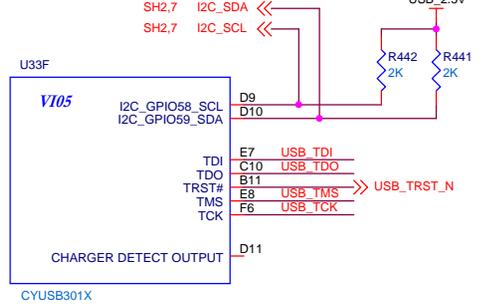
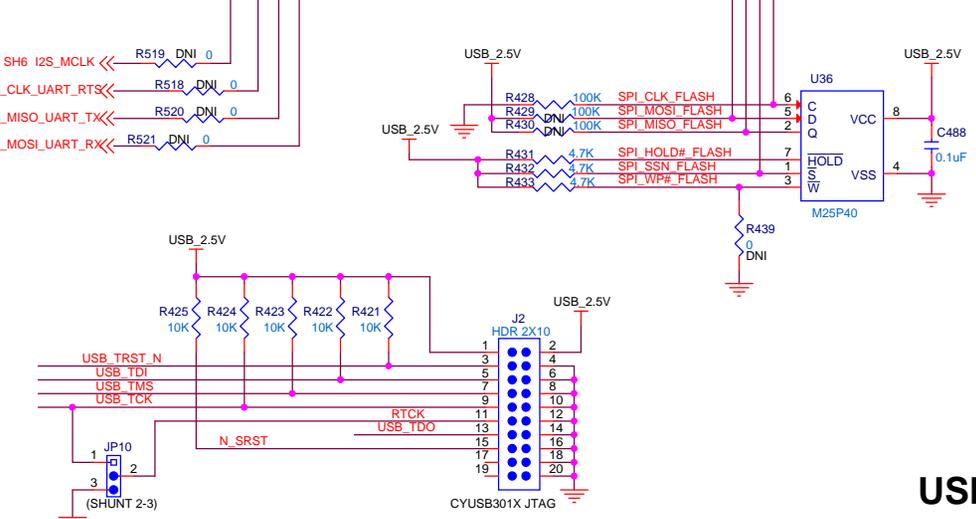
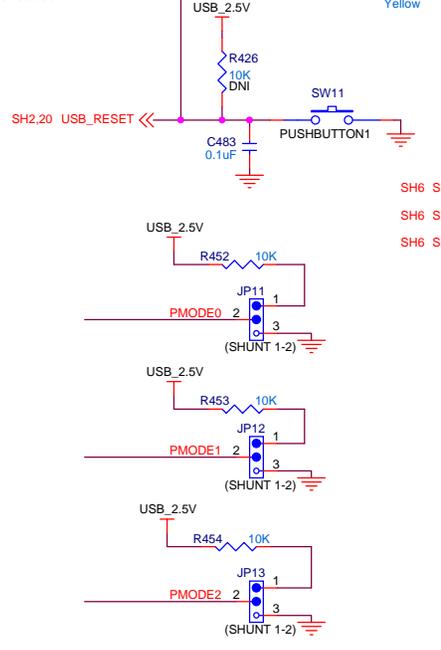
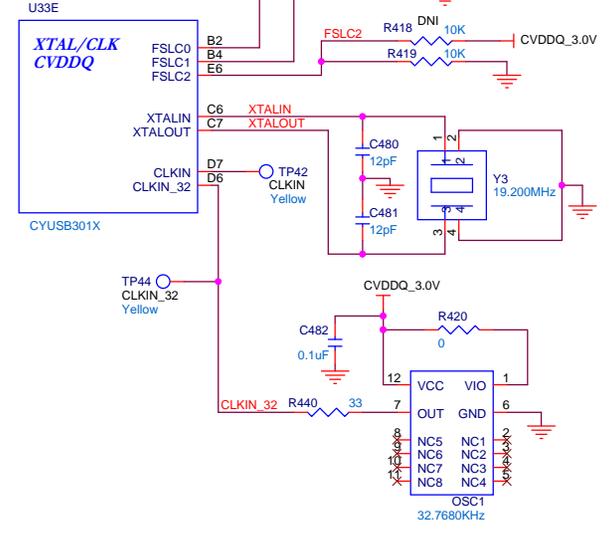
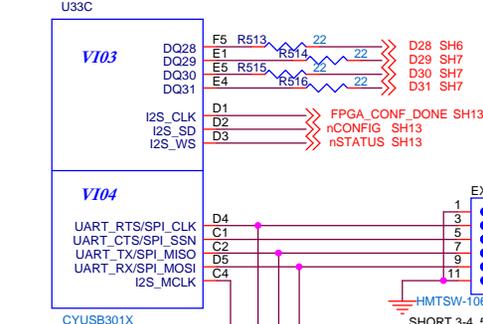
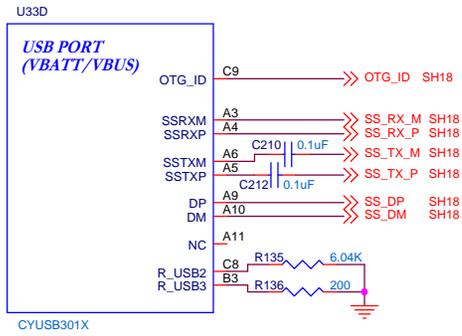
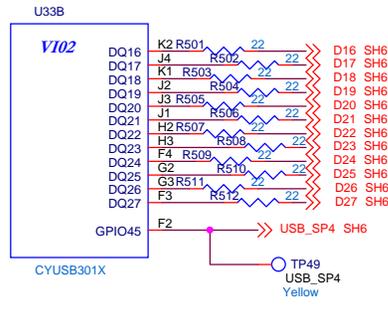
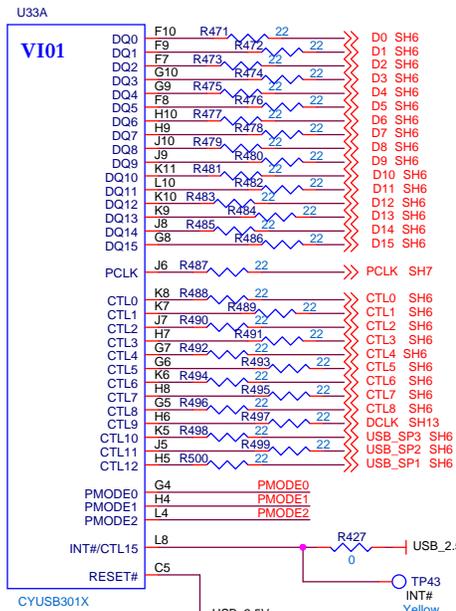
FPGA Decoupling

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USB

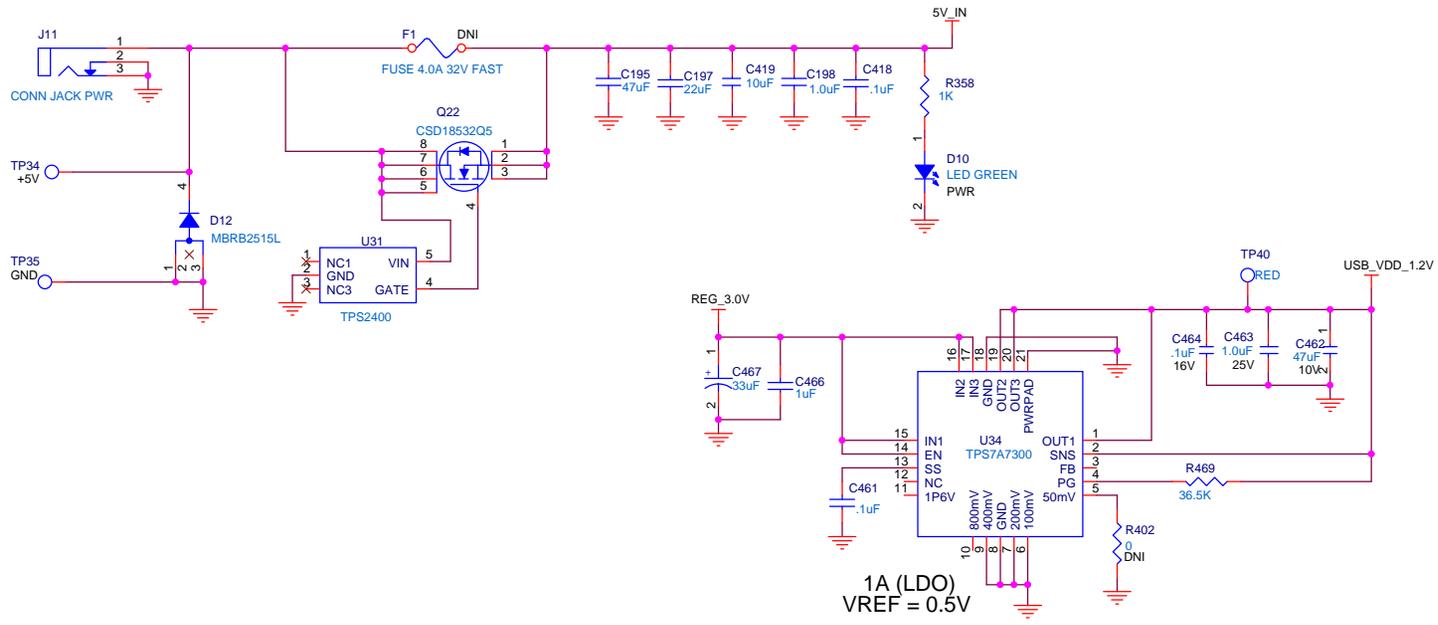
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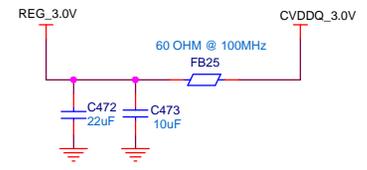
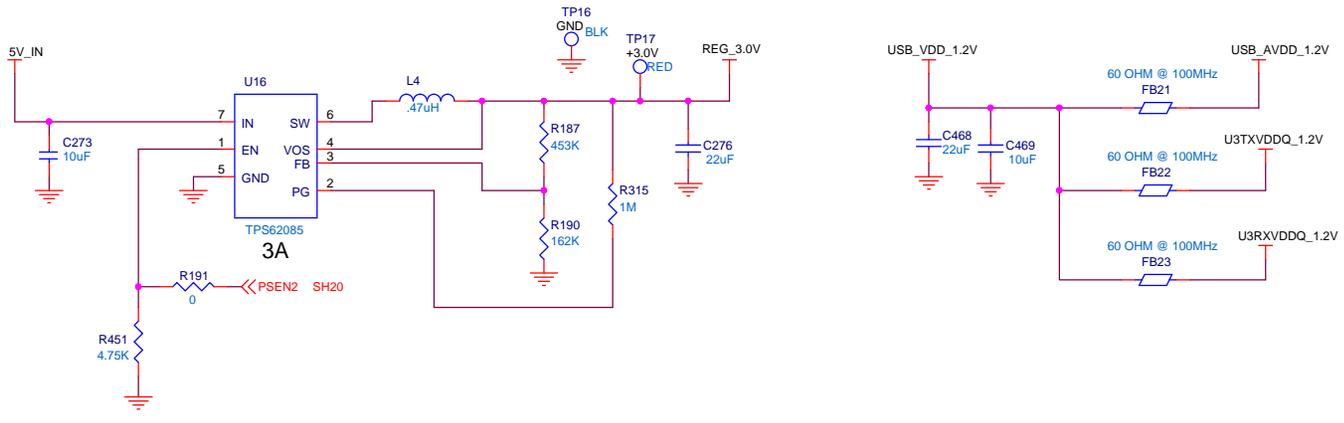
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5V DC INPUT



1A (LDO)
VREF = 0.5V

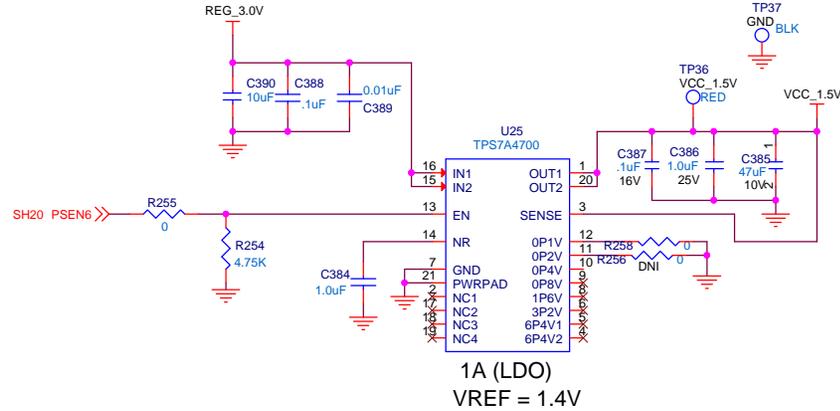
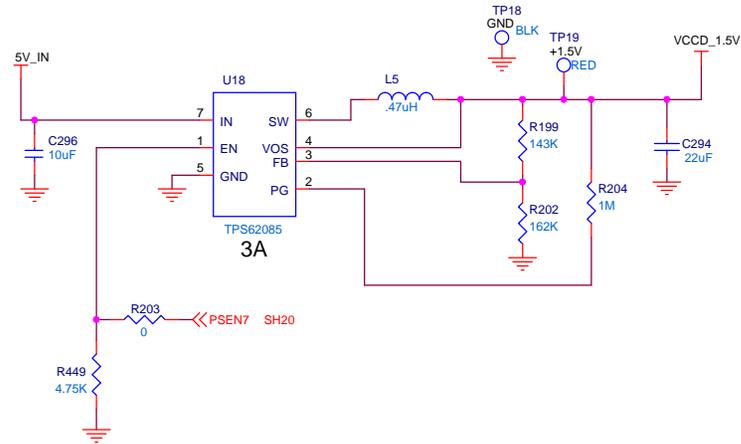
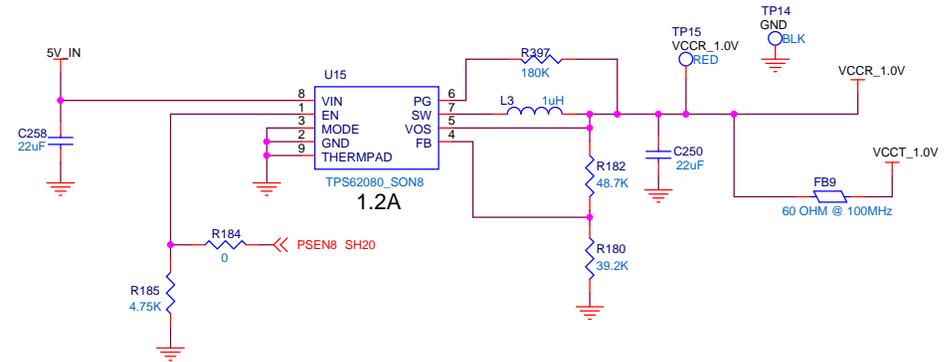
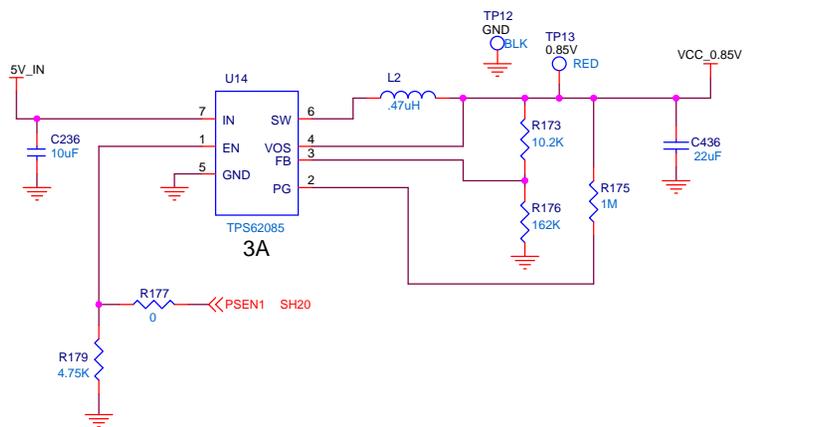


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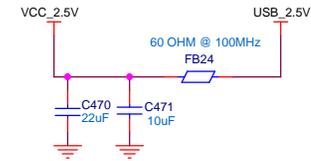
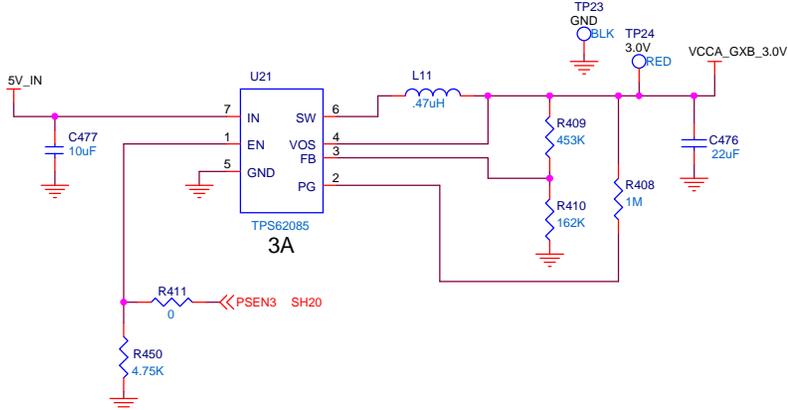
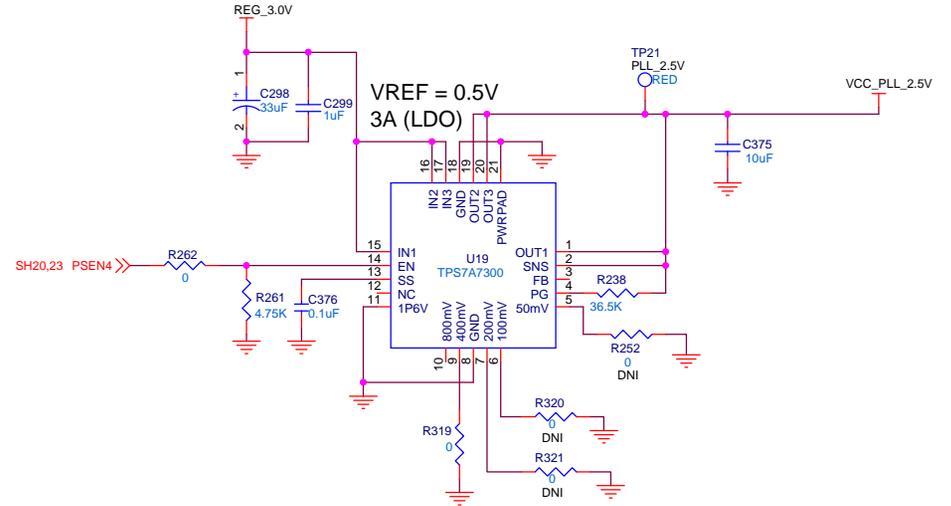
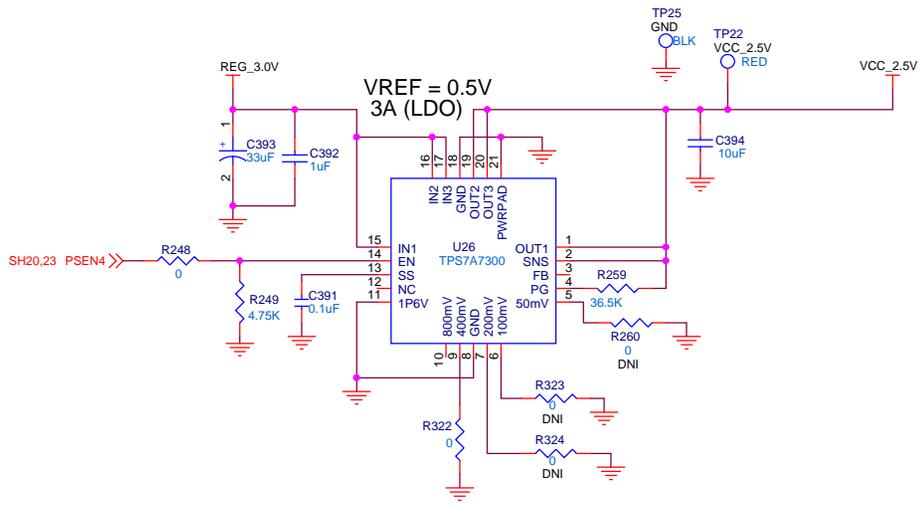
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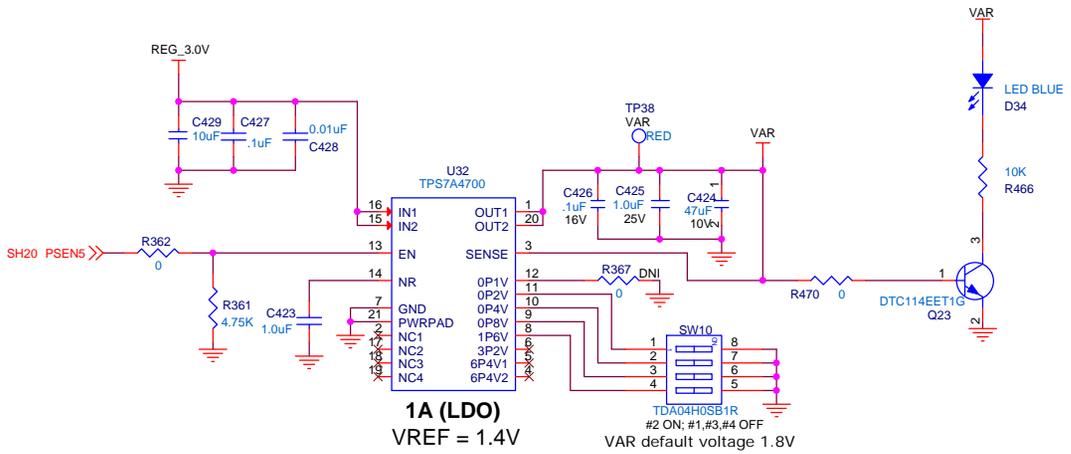
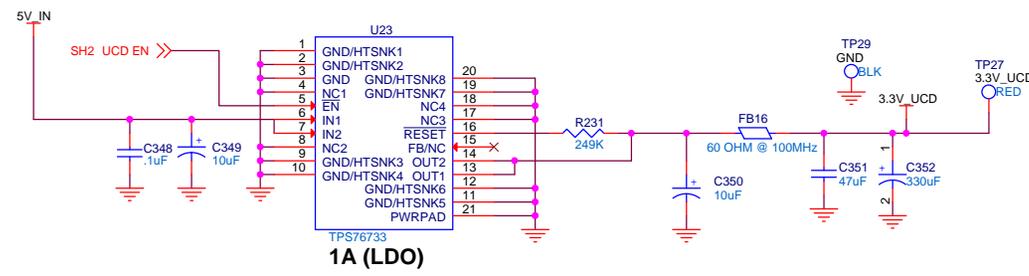
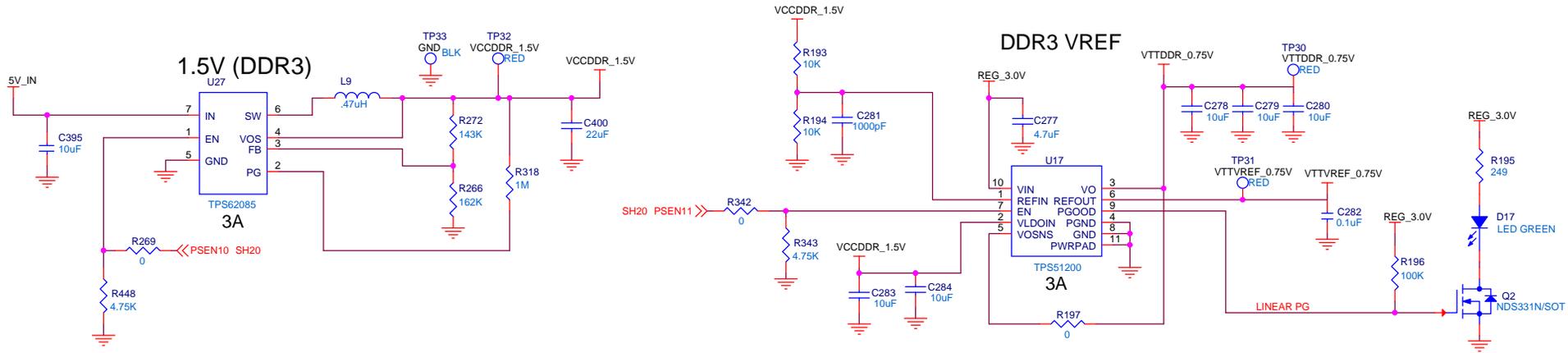
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