Application Report

SNLA056D–October 2002–Revised April 2013

# AN-1263 DP83865 Gig PHYTER V 10/100/1000 Ethernet Physical Layer Design Guide


**ABSTRACT**

This application report discusses the design for the 10/100/1000 DP83865 Gigabit Ethernet physical layer transceiver.


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# 1 Introduction

This design guide is intended to assist in the circuit design and board layout of the DP83865 Gigabit Ethernet physical layer transceiver. This design guide covers the following subjects:

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# 2 Hardware Reset and Start Up

There is no on-chip internal power-on reset and the DP83865 requires an external reset signal applied to the $\overline{\text{RESET}}$ input. The active low $\overline{\text{RESET}}$ should be held low for a minimum of 150 µs to allow power supply voltage and clock input to stabilize before starting internal initialization. The first MDIO access should wait another 500 µs till internal initialization is completed. For timing details see Section 7 of the datasheet.

# 3 Clocks

The CLOCK_IN pin is the 25 MHz clock input to the DP83865 used by the internal PLL to generate various clocks needed internally and externally. This input should come from a 25 MHz clock oscillator or crystal. Check Section 12 for component requirements. When using a crystal, CLOCK_OUT must be connected to the second terminal, and when using with a oscillator the CLOCK_OUT pin should be left floating.

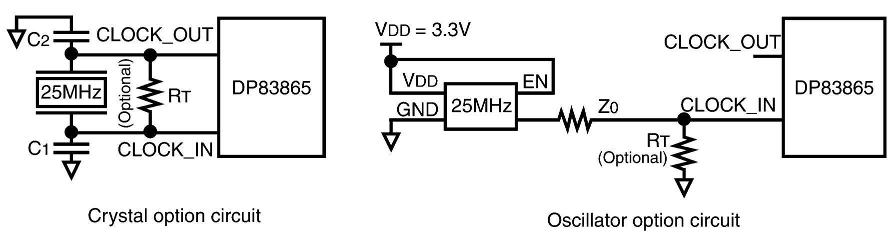


**Figure 1. Clock Input Circuit**

The clock signal requires termination consideration. The termination requirement depends on the trace length of the clock signal. No series or load termination is required for short trace less than 0.5 inch. For longer traces termination resistors are recommended.

There are a number of ways to terminate clock traces. The commonly used types are series and parallel termination. Series termination consumes less power and it is the recommended termination. The value of the series termination resistor is chosen to match the trace characteristics imped-ance. For example, if the clock source has output impedance of 20 Ω and the clock trace has characteristic impedance Zo = 50 Ω then Rs = 50 - 20 = 30 Ω. The series source termination Rs should be placed close to the output of the crystal oscillator.

The parallel termination consumes more power than series termination, but yields faster rise and fall times. The value of the termination is equal to the trace characteristic impedance, $R_T$ = Zo. The parallel termination $R_T$ should be placed close to the PHY CLOCK_IN pin to eliminate reflections.

In cases where multiple PHY's exist on the same board, it may be cost effective to use one oscillator with a high speed PLL clock distribution driver. Connecting multiple clock inputs in a Daisy chained style should be avoided, especially when series termination is applied.

Adequate and proper decoupling is important to the clock oscillator performance. A multilayer ceramic chip capacitor should be placed as close to the oscillator VDD pin as possible to supply the transient switching current.

EMI is another consideration when designing the clock circuitry. The EMI field strength is proportional to the current flow, frequency, and loop area. By applying series termination, the current flow is less than parallel termination and the edge speed is slower, making it better for EMI considerations. Loop area is defined as the trace length times the distance to the ground plane, i.e., the current return path. By keeping the clock trace as short as possible reduces the loop area that reduces EMI.

It is best to place the oscillator toward the center of the PCB rather than at the edge. The radiated magnetic field tends to be stronger when traces are running along the PCB edge. If the trace has to run along the edge of the board, make sure the trace to board edge distance is larger than the trace to ground plane distance. This would make the field around the trace more easily coupled to the ground than radiating off the edge. If the clock trace is placed on the surface layer, by placing parallel ground trace on each side of the clock trace could localize the EMI and also prevent crosstalk to adjacent traces. By burying the clock trace in between the ground and VDD plane could also minimize EMI radiation.

For a through-hole clock oscillator component, mount the oscillator as flat and close to the PCB as possible and, trim excessive leads if necessary. Provide a ground pad equal or larger than the oscillator foot print on the component side of the PCB. Tie this ground pad to the ground plane through multiple vias. This would minimize the distance to the ground plane and provide better coupling of the electro-magnetic fields to the board.

## 4 Power Supply Decoupling

The capacitance between power and ground planes can provide appreciable power supply decoupling for high edge rate circuits. This "plane capacitor" has very low ESR and ESL so that the plane capacitance remains effective at the frequencies so high that chip capacitors become ineffective. It is strongly recommended that the PC board have one solid ground plane, one solid 2.5 V plane, and one solid 1.8 V plane with no breaks. The interplane capacitance between the supply and ground planes may be maximized by reducing the plane spacing. In addition, filling unused board areas on signal planes with copper and connecting them to the proper power plane will also increase the interplane capacitance.

The 2.5 V and the 1.8 V supply pins are paired with their corresponding ground pins. Every other paired supply pins need to be decoupled with Surface Mount Technology (SMT) capacitors. It's recommended that SMT capacitance alternates between 0.01 µF and 0.1 µF so that the resonance frequencies of the capacitors are "dispersed". The decoupling capacitors should be placed as close to the supply pin as possible. For optimal results, connect the decoupling capacitors within 0.010 inch to the power pins. For lowest ESL and best manufacturability, place the plane connecting via within 0.010 inch to the SMT capacitor pads, see Figure 2.

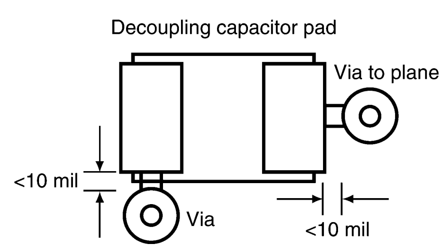


**Figure 2. Place Via Close to Pad**

Bulk capacitance supplies current and maintains the voltage level at frequencies above the rate that the power supply can respond to and below frequencies that chip capacitors are effective. To supply lower speed transient current, a tantalum 10 µF capacitor for each power plane and each port should also be placed near the DP83865.

Lowering the power supply plane and ground plane impedance will also reduce the power supply noise. A 1 oz. copper is recommended for the power and ground planes. Avoid routing power or ground traces to the supply pins that could introduce inductive coupling leading to ground bounce. Connect power and ground pins directly to the planes.

The power supply decoupling recommendations may be perceived conservative. However, for the early prototyping, please follow the guide lines and recommendations to assure first time success. To lower the manufacturing cost, the component count may be reduced by the designer after careful evaluation and extensive tests on EMI and bit-error-rate (BER) performance.

## 5 Sensitive Supply Pins

The Analog PGM_AVDD supply is susceptible to noise and requires special filtering to attenuate high frequencies. A low pass filter formed by a 18 Ω resistor, a 22 µF and a 0.01 µF capacitor is suggested (Figure 3).

A 1% 9.76 kΩ resistor is needed to connect to the BG_REF pin. The connections to this resistor needs to be kept as short as possible (Figure 3).

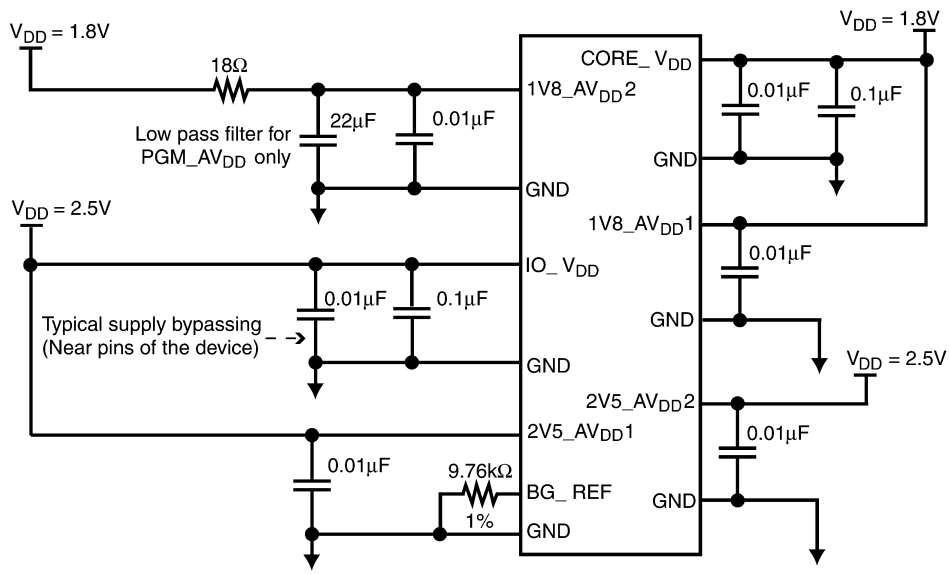


**Figure 3. Power Supply Filtering (One Port)**

Avoid placing noisy digital signal traces near these sensitive pins. It is recommended that the above mentioned components should be placed before other components.

The 1.8 V supplies both the digital core and the analog. The analog power supply is sensitive to noise. To optimize the analog performance, it is best to locate the voltage regulator close to the analog supply pins. Avoid placing the digital core supply and GMAC in the analog return path. An example of voltage regulator placement is shown in Figure 4.

Ferrite beads could be used to isolate noisy VCC pins and preventing noise from coupling into sensitive VCC pins. This bead in conjunction with the bypass capacitors at the VCC pins form a low pass filter that prevents the high frequency noise from coupling into the quiet VCC. However, the use of ferrite beads may yield mixed results when the inductance resonates with the capacitance. To decrease the likelihood of resonance, a resistor in parallel with the ferrite bead may be used. The noise characteristics vary from design to design. Ferrite beads may not be effective in all cases. The decision is left to the board designer based on the evaluation of a specific case.

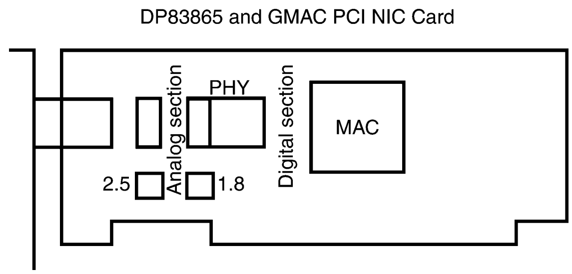


**Figure 4. 1.8 V Voltage Regualtor Placement**

## 6 PCB Layer Stacking

To route traces for the DP83865 PQFP package, a minimum of four PCB layers is necessary. To meet performance requirements, a six -ayer board design is recommended. The following is the layer stacking recommendations for four, six, and eight-layer boards.

**Four-layer board (typical application: NIC card):**

1. Signal 1 (top layer)
2. GND
3. 3.3 Volt power plane
4. Signal 2, planes for 1.8 Volt and 2.5 Volt

**Six-layer board:**(Figure 5)

1. Signal 1 (top layer)
2. Power plane
3. Signal 2 (best for clock and MDI signals)
4. Signal 3 (best for clock and MDI signals)
5. GND
6. Signal 4

**Eight-layer board:**

1. Signal 1 (top layer)
2. GND
3. Signal 2 (best for clock and MDI signals)
4. Power plane 1
5. GND
6. Signal 3 (best for clock and MDI signals)
7. GND or power plane 2
8. Signal 4

**Note** that signal traces crossing a plane split should be avoided (Figure 6). Signal crossing a plane split may cause unpredictable return path currents and would likely to result signal quality failure as well as creating EMI problems.

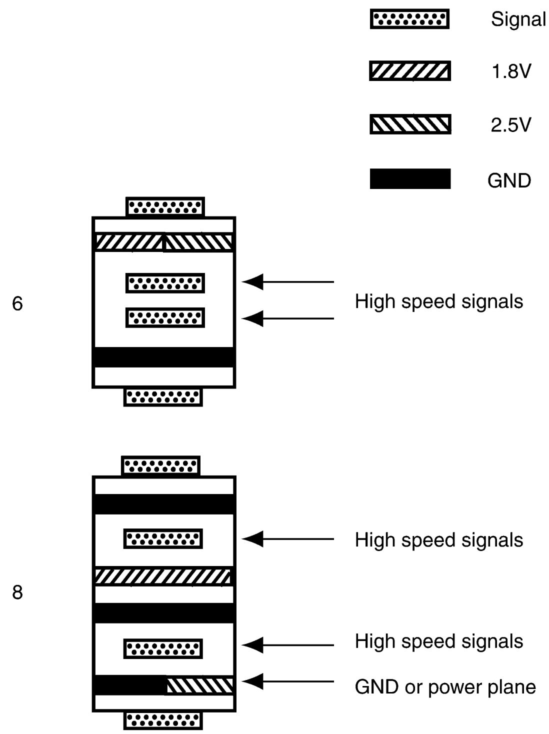


**Figure 5. PCB Layer Stacking, Circuit Side**

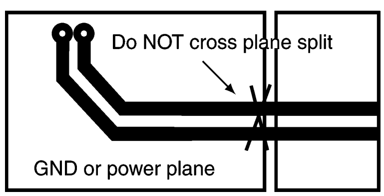


**Figure 6. Signal Crossing a Plane Split**

The layer stacking on the isolated chassis side is shown in Figure 7.

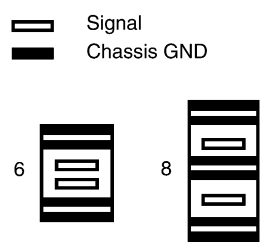


**Figure 7. Layer Stacking, Chassis Side**

# 7 Layout Notes on MAC Interface

## 7.1 Trace Impedance

All the signal traces of MII, and GMII should be impedance controlled. The trace impedance reference to ground is 50 Ohms. Uncontrolled impedance runs and stubs should be kept to minimum.

## 7.2 MII, and GMII Interfaces

MII, GMII, and RGMII are single-ended signals. The output of these signals are capable of driving 35 pF under worst conditions. However, these outputs are not designed to drive multiple loads, connectors, backplanes, or cables.

## 7.3 Termination Requirement

The purpose of the series termination is to reduce reflections and to improve the signal quality. The board designer should evaluate the reflection and signal integrity to determine the need for the termination in each design. As a general rule, if the trace length is less than 1/6 of the equivalent length of the rise and fall times, the series termination is not needed. The following is an example of calculating the signal trace length.

The rise and fall times of GMII are in the order of 500 ps for RX_CLK, and GTX_CLK. Propagation Delay = 170 ps/inch on a FR4 board. Equivalent length of rise time = (1/6) Rise time (ps) / Delay (ps/inch) = (1/6) *(500/ 170) = 0.5 inch. Thus, series termination is not needed for traces less than 0.5 inch long.

The value of the series termination depends on the driver output impedance and the characteristic impedance of the PCB trace. Termination value Rs = characteristic impedance Zo - driver output impedance Ro. For example, if $V_{DDIO}$ = 3.3 V, Ro = 27 Ω, Zo = 50 Ω, and Rs = 50 - 27 = 23 Ω. Check Section 7.0 Electrical Specifications of the DP83865 Data Sheet for Ro value.

## 7.4 Recommended Maximum Trace Length

Although that GMII and RGMII are synchronous bus with clock and data traveling in the same direction, there are a number of factors limiting the trace length. At longer trace, the signal becomes more attenuated at the destination so that it becomes more susceptible to noise interference. The rise time slows down that could be pron to jitter. Longer trace also acts as an antenna if it is on the surface layer that can radiate EMI. If a long trace is running adjacent to a noisy signal, there could be cross talk coupled into the signal path.

It is highly recommended that to keep the trace length as short as possible. Ideally, it is recommended to keep the trace within two inches. If the application requires longer trace length please keep it below six inches and place the trace in the middle layer.

Trace length matching could play a significant role. If the longest and the shortest trace length difference is 4 inches, the delay difference could be 4 x 170 ps = 680 ps. The delay skew may cause timing metastability.

# 8 Twisted Pair Interface

The Twisted Pair Interface consists of four differential media dependent I/O pairs (MDI_A, MDI_B, MDI_C, and MDI_D). Each signal is terminated with a 49.9 Ω resistor. Figure 8 shows a typical connection for channel A. The circuitry of channels A, B, C, and D are identical. The MDI signals are directly connect to 1:1 magnetics. To optimize the performance, the key parameters for the magnetics are specified. Please refer to Section 12.2.

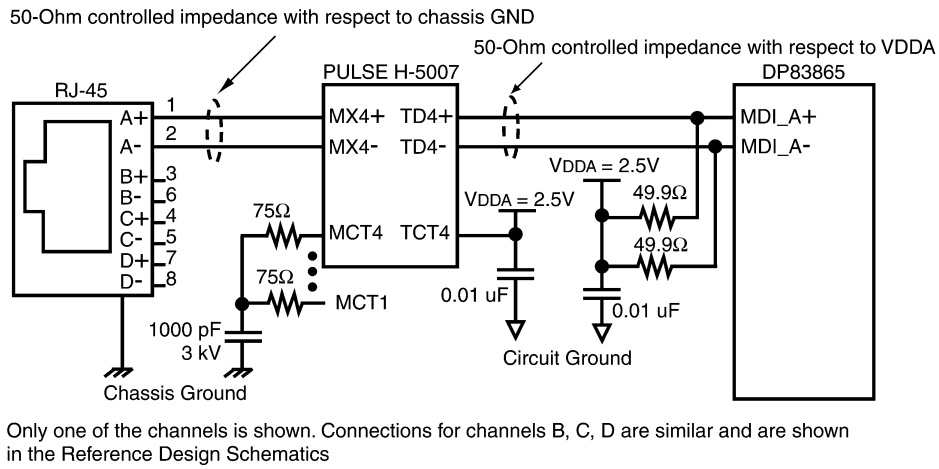


**Figure 8. Twisted Pair/Magnetics Interface (Channel A)**

The following is a layout guide line for the MDI section.

- Place the 49.9 Ω 1% termination resistors as close as possible to the PHY. Place a 0.01 µF decoupling capacitor for each channel between 2.5 V plane and ground close to the termination resistor. Place a 0.01 µF decoupling capacitor for each port at the transformer center tab.
- For microstrip traces, a solid ground plane is needed under the signal traces. The ground plane keeps the EMI localized and the trace impedance continuous. Since the strip-line traces are typically sandwiched between the ground planes, they have the advantage of lower EMI radiation and less noise coupling. The trade off of using strip line is lower propagation speed.
- All the MDI interface traces should have a controlled impedance of 50 Ω to the 2.5 V plane. This is a strict requirement to minimize return loss.
- Each MDI pair should be placed as close as possible in parallel to minimize EMI to the adjacent trace. The spacing between each channel controls the inductive crosstalk and should be at least twice the spacing between the members of each pair.
- Capacitive coupling occurs when traces run directly on top of each other in parallel. A 2.5V power plane should be placed between each trace layer of different channels.
- Each member of a pair should be matched in length to prevent mismatch in delay that would cause common mode noise.
- Ideally there should be no crossover or via on the signal paths.

## 9 RJ-45 Connections

The magnetics isolates local circuitry from other equipment that Ethernet connects to. The IEEE isolation test places stress on the isolated side to test the dielectric strength of the isolation. The center tap of the isolated winding has a "Bob Smith" termination through a 75 Ω resistor and 1000 pF cap to chassis ground. The termination capacitor should have voltage tolerance of 3 kV (Figure 8).

To pass EMI compliance tests, there are a few helpful recommendations to follow.

- The RJ-45 is recommended to have metal shielding that connects to chassis ground to reduce EMI emission.
- The isolated side should have the chassis ground "island" placed. The MDI pairs are placed above a continuous chassis ground plane.
- The MDI pairs are suggested to be routed close together in parallel to reduce EMI emission and common mode noise (Figure 9). The spacing between each channel controls the inductive crosstalk and should be at least twice the spacing between the members of each pair.

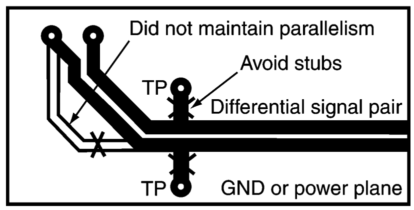


**Figure 9. Differential Signal Pair**

- The EMI can be further reduced by placing the striplines between chassis ground. Note that placing the traces directly on top of each other in parallel may cause capacitive coupling between channels. Use chassis ground to separate channels on different layers.
- Generally, it is a good practice not to overlap the circuit ground plane with the chassis ground that creates coupling. Instead, make chassis ground an isolated island and make a void between the chassis and circuit ground. Place two or three 1206 pads across the chassis and circuit ground void. This would allow experimentally choosing the appropriate inductive, capacitive, or resistive components to pass EMI emission test.

## 10 LED/Strapping Option

When the LED outputs are used to drive LEDs directly, the active state of each output driver depends on the logic level sampled by the corresponding strapping input upon power-up or reset. For example, if a strapping input is pulled low and the corresponding output is configured as an active high LED driver (Figure 11). Conversely, if a strapping input is pulled high and the corresponding output is configured as an active low LED driver. Figure 10 is an example of LED and PHYAD connection with the base address strapped to 00011 (03h).

The internal pull-up and pull-down resistor values are between 50 kΩ to 80 kΩ. It is recommended that an external 2 kΩ pull-up or pull-down resistor is applied to make absolutely certain that the correct level is strapped to.

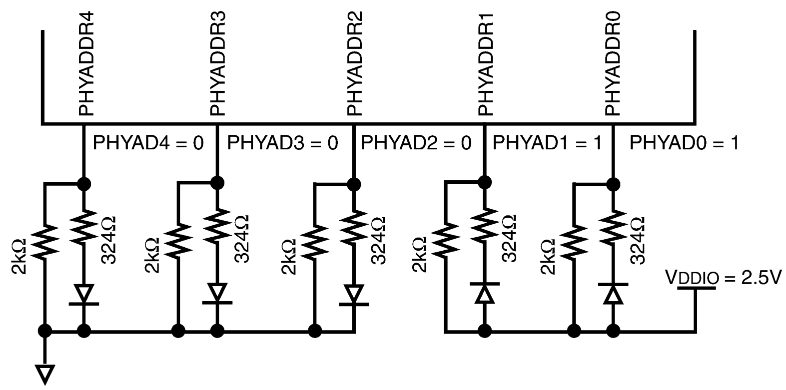


**Figure 10. PHYAD/LED Strap Configuration. (PHY base address = 3)**

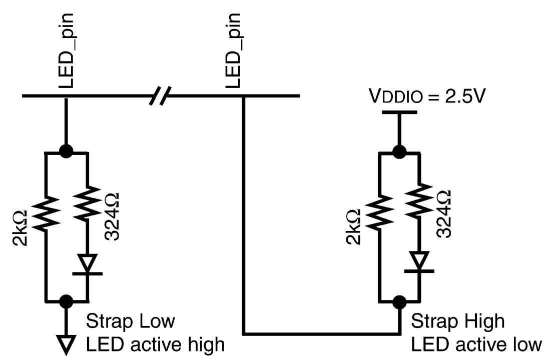


**Figure 11. LED/Strapping Option examples**

## 11 Unused Pins and Reserved Pins

Unused CMOS input pins should not be left floating. Floating inputs could have intermediate voltages halfway between VCC and ground and, as a consequence, turning on both the NMOS and the PMOS transistors resulting in high DC current. Floating inputs could also cause oscillations. Therefore unused inputs should be tied high or low. In theory CMOS inputs can be directly tied to VCC or GND. This method has the advantage of minimizing component count and board space. However, it's safer to pull the unused input pins high or low through a current limiting resistor. This resistor will prevent excessive current drawn at the input pin in case there is a defect in the input structure shorting either VCC or GND to the input. Another advantage of the protection resistor is to reduce the possibility of latch-up. To save component count and board space, the adjacent unused input pins can be grouped and tied together with a single resistor.

The unused input pins on DP83865 are the JTAG TDI, TRST, TMS and TCK that can be all tied together and pulled-down using a 2 kΩ resistor. Other reserved or unused pins may be pulled up/down using a 2 kΩ resistor.

# 12 Component Selection

## 12.1 Oscillator or Crystal

The requirements of 25 Mhz oscillators and crystals are listed in Table 1 and Table 2. Some recommended oscillator manufacturers are listed in Table 3.

Quartz crystals exhibit a unique characteristic when subject to temperature changes. "AT cut" is the most common type of crystal cut that will provide the optimum stability in frequency. AT cut is the recommended type for DP83865.

Note that the jitter specification was derived from maximum capacitance load, worst case supply voltage, and wide temperature range. The actual allowable jitter number may be significantly higher when driving the DP83865 clock input under normal operating conditions. Please consult the respective vendors for specifics.

**Table 1. 25 MHz Crystal Oscillator Requirements**

| Parameter | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|
| Frequency | | 25 | | MHz | |
| Frequency Stability | | | ± 50 | ppm | 0 - 70 deg C, 1 year aging, load change |
| Rise/Fall Time | | | 6 | nS | 20 - 80 % |
| Jitter (short term) | | | 25 | pS | Cycle-to-cycle, driving 10 pF load |
| Jitter (long term) | | | 200 | pS | Accumulative over 10 uS |
| Load Capacitance | 15 | | | pF | |
| Symmetry | 40 | | 60 | % | |
| Logic 0 | | | 10% VDD | V | VDD = 2.5 or 3.3 V nominal |
| Logic 1 | 90% VDD | | | V | VDD = 2.5 or 3.3 V nominal |

**Table 2. 25 MHz Crystal Requirements**

| Parameter | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|
| Frequency | | 25 | | MHz | |
| Frequency Tolerance | | | ± 50 | ppm | 0 °C to 70 °C |
| Frequency Stability | | | ± 50 | ppm | 1 year aging |
| Load Capacitance | 15 | | 40 | pF | Total load capacitance including C1 and C2 |

**Table 3. Recommended Crystal Oscillators**

| Manufacturer | Description | Part Number |
|---|---|---|
| Vite Technology www.viteonline.com | 125 MHz 7.5 x 5 mm Crystal Oscillator | VCC1-B2B-125M000 |
| | 25 MHz 7.5 x 5 mm Crystal Oscillator | VCC1-B2B-25M000 |
| Raltron www.raltron.com | 25 MHz 7.5 x 5 mm Crystal Oscillator | C04305L-25.000MHz |
| Saronix www.saronix.com | Crystal Clock Oscillator, 125MHz | SCS-NS-1132 |
| Valpey Fisher www.valpeyfisher.com | 125 MHz Crystal Oscillator | VFAC570BL |
| | 125 MHz Crystal Oscillator | VFAC38L |
| **Note:** Contact Oscillator manufactures for latest information on part numbers and product specifications. All Oscillators should be thoroughly tested and validated before using them in production. | | |

In the case where multiple clock sources are needed, high speed PLL clock distribution driver is recommended. The drivers may be obtained from vendors such as Texas Instrument, Pericom, and Integrated Device Technology. Note that the jitter specification may be derived from maximum capacitance load, worst case supply voltage, and wide temperature range. The actual jitter number may be significantly lower when driving DP83865 clock input under normal operating conditions. Please consult vendor for specifics.

## 12.2 Magnetics

The magnetics has large impact on the PHY performance. Per IEEE 802.3ab Clause 40.8, the component requirements are listed in Table 4. In addition, it is recommended that the magnetics has an isolation transformer followed by a common mode choke to reduce EMI (Figure 12). There is an additional autotransformer which is center tapped. To save board space and reduce component count, RJ-45 with integrated magnetics may be used (Table 5).

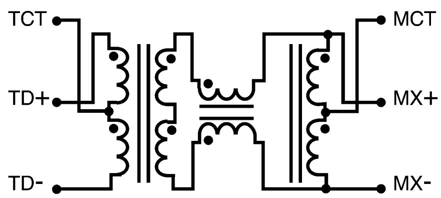


**Figure 12. Transformer Configuration (1 ch)**

**Table 4. Magnetics Requirements**

| Parameter | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|
| Turn Ratio | | 1:1 | | | ± 2% |
| Insertion Loss | -1.1 | | | dB | 0.1 - 1 MHz |
| | -0.5 | | | dB | 1 - 60 MHz |
| | -1.0 | | | dB | 60 - 100 MHz |
| | -1.2 | | | dB | 100 - 125 MHz |
| Return Loss | -18 | | | dB | 1 - 30 MHz |
| | -14.4 | | | dB | 30 - 40 MHz |
| | -13.1 | | | dB | 40 - 50 MHz |
| | -12 | | | dB | 50 - 80 MHz |
| | -10 | | | dB | 80 - 100 MHz |
| Differential to Common Rejection Ration | -43 | | | dB | 1 - 30 MHz |
| | -37 | | | dB | 30 - 60 MHz |
| | -33 | | | dB | 60 - 100 MHz |
| Crosstalk | -45 | | | dB | 1 - 30 MHz |
| | -40 | | | dB | 30 - 60 MHz |
| | -35 | | | dB | 60 - 100 MHz |
| Isolation | 1,500 | | | Vrms | HPOT |
| Rise Time | | 1.6 | 1.8 | ns | 10 - 90 % |
| Primary Inductance | 350 | | | uH | |

**Table 5. Recommended Magnetics**

| Manufacturer | Description | Part Number |
|---|---|---|
| Bel Fuse, Inc.<br>www.belfuse.com | 10/100/1000 Mbps Isolation Transformer | S558-5999-P3 |
| | 10/100/1000 Mbps Isolation Transformer | S558-5999-T3 |
| | 10/100/1000 Mbps2X1 Integrated Magnetics | 0843-2B1T-33 |
| Delta<br>www.delta.tw | 10/100/1000 Mbps Isolation Transformer | LF9203 |
| Halo<br>www.haloelectronics.com | 10/100/1000 Mbps Isolation Transformer | TG1G-S002NZ |
| Midcom<br>www.we-online.com | 10/100/1000 Mbps Isolation Transformer | 000-7093-37R |
| Pulse Engineering, Inc.<br>www.pulseeng.com | 10/100/1000 Mbps Isolation Transformer | H5007 |
| | 10/100/1000 Mbps Isolation Transformer | H5008 |
| **Note:** Contact Magnetics manufactures for latest part numbers and product specifications. All Magnetics should be thoroughly tested and validated before using them in production. | | |

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