Balancing SoC Design and Technology Challenges at 45nm

J.M.C. Stork

Texas Instruments, Inc. *13560 North Central Expressway, Dallas, TX 75243*

Abstract

The ability of advanced CMOS to integrate processor cores, memory and ASIC logic with RF and analog functions on the same die, has enabled unprecedented density and performance especially for mobile communication systems. Continuing this progress at 45nm and below requires simultaneously improving gate density, system power, and functional performance while reducing the cost per finished die.

Introduction

The economic benefit of CMOS scaling has been realized by improving at each node the density by 2x, and increasing performance over 20%, while limiting the final cost per wafer increase to less than 30%. Process technology progress calls for 193nm immersion lithography with resolution enhancements, metal gate with high-k gate dielectric, strain engineering, and low-k interconnect dielectrics. Although these changes are costly and complex, they alone are not sufficient to realize the historical performance and density trend. Design innovations need to limit static and dynamic power dissipation, tolerate escalating parameter variations, maximize increasingly restricted layout options, and incorporate analog and RF functions at low voltage. The mobile phone platform brings all these challenges together and shows the value of vertically integrated expertise to create a balanced product solution (Fig 1).

Optimizing the process “k-space”

Immersion allows for effectively shorter wavelength and higher NA lens design to improve the lithographic patterning pitch. A manufacturable implementation requires cost effective throughput, defect density, and resist solution. The large increase in capital equipment cost consumes a large fraction of the process cost budget. Contact holes and interconnect via pitches are major factors limiting SRAM and logic design density (Fig 2). Improving on the k1 patterning factor includes use of resolution enhancement techniques (RETs) such as alternating and attenuated phase shifters, sub resolution assist features, and model-based optical proximity correction (OPC). The added mask algorithm and computation complexity requires new verification tools and techniques (Fig 3).

Transistor gate length scaling is severely hindered by the inability to scale the physical thickness of the SiON gate dielectric. While the density penalty is limited, high gate leakage current presents design restrictions that limit the low voltage stability of the smallest SRAM cells. Progress on metal gate and/or high-k dielectric materials has been slower than expected due to the extreme requirements on the materials properties and limitations on the process integration schemes, e.g. FUSI. Fortunately, the physics and process control of the gate electrode-dielectric interface have recently achieved fundamentally better understanding.

Changes in the E-k structure of the conduction and valence bands of Si because of tensile (electron) and compressive (hole) strain (Fig 4) increase the carrier mobility more than any other technique known. While the gain in drive currents is large, many of the techniques impose density trade-offs (e.g. see Fig 5).

The need for lower-k interconnect dielectrics has long been recognized, but slowly realized. Simplifying the integration scheme to limit negative barrier and etch stop layer effects on performance is now widely attempted (Fig 6).

Design Implications

Absolute interconnect performance has become dominant (Fig 7), and, consequently, variations in line-width and thickness add increasingly to the design margin. While many effects are systematic, the complexity of interconnect prevents a brute force computational solution (Fig 8). Encouraging progress by the EDA tool suppliers is trailing the needs for leading product designs. While pattern variations limit interconnect density, power management sets a limit to transistor efficiency. As can be seen from Fig 9, without power management, standby leakage would prevent an acceptable product.

Integrating analog and RF functions in advanced CMOS requires an architectural approach to maximize the features of density and speed rather than precision of analog components. Additionally, understanding and modeling the impact of new processes on cutoff frequency (Fig 10), matching, 1/f noise and Q values is an early requirement.

Finally, space and cost efficiency are also required for the package. Recently, stacked die has emerged as a preferred way for large memory embedding (Fig 11). Future implementation will likely see board embedded die to maximize space and performance.

Summary

Achieving highly integrated, advanced CMOS systems at low cost can be accomplished with a joint technology and design optimization of each successive node. This allows early understanding and modeling of the process sensitivities required to optimize the economies of scaling.

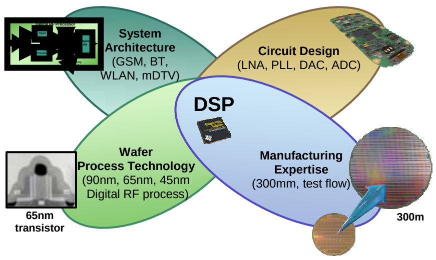

Fig.1 Realization of a cost effective integrated cell phone platform requires collaboration of systems, design and process expertise.

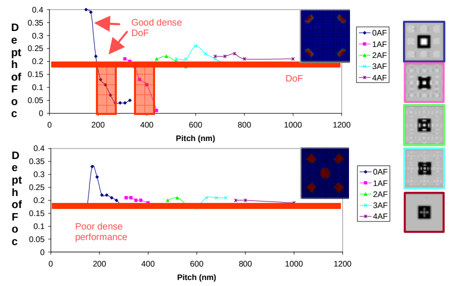

Fig.2 Patterning density is eventually a trade-off between depth of focus and design restrictions. Immersion allows much wider process window.

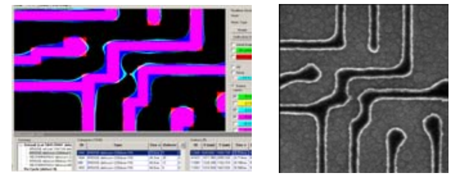

Fig.3 Computationally efficient post OPC verification systems enable rapid evaluation of the process window and allow iteration of design choices.

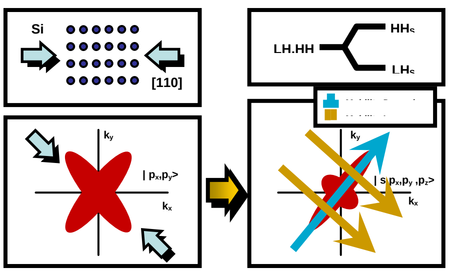

Fig.4 Valance band structure changes as a result of compressive strain. Left, without, right, with strain in the [110] direction.

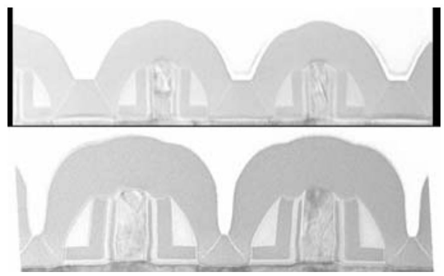

Fig.5 Thickness of the stress layer is limited by gate pitch and produces asymmetric, shear stress. Layout density is therefore compromised.

Node	130nm	90nm	65nm	45nm	32nm
No. of levels of metal (Wireless)	5	5	6	6	6
No. of levels of metal (DSP)	6	7	7	8	8
Dielectric Constant of Low-k	3.6	2.9	2.9	2.5	2.3
Effective Dielectric Constant	3.91	3.55	3.31	2.98	2.85
Aspect Ratio	1.71	1.79	1.6	1.8	1.8
Minimum width (MET3)	175	140	100	70	50
Rsheet for min width (MET3)	79.1	113	233	366	482

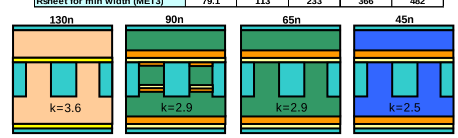

Fig.6 Interconnect materials and integration processes have allowed much slower k-eff reduction than anticipated.

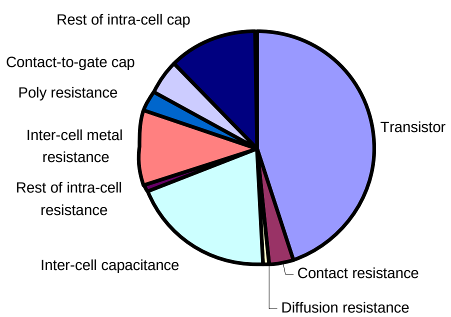

Fig.7 Interconnect related capacitance and resistance components outweigh transistor effects in 65nm designs.

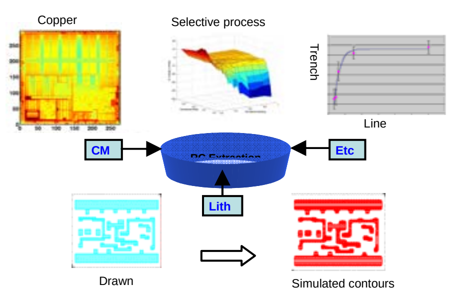

Fig.8 Systematic variations in interconnect patterns require highly efficient EDA tools for performance assessment.

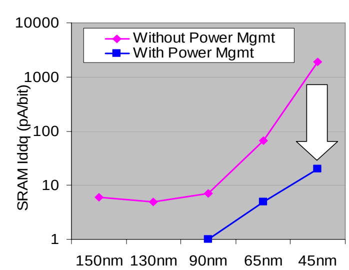

Fig.9 Starting with 90nm, power management is required to limit the expected Iddq increase per node.

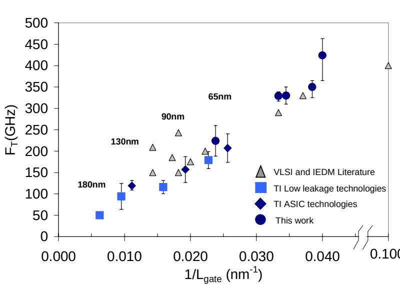

Fig.10 Cut-off frequency of NMOS devices reaches above 450GHz (PMOS ~1/2x). Accurate modeling is essential for optimized use.

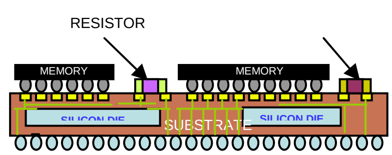

Fig.11 Embedded memory modules are the natural progression of stacked package implementations.

		90nm	65nm	45nm
Die Scaling – Low Power Flow		63%	49%	<=50%
Gate Density (kgate/mm^2)		440	930	~1900
SRAM Bit Area (um^2)		0.97	0.484	<0.25
Power Management		10x, 50x,	1000x, 5000x	5000x, 50000x
RF/Analog Components		~50	~50	~50
Max Metal Levels	Low Power Flow	6	6	6 Cu +
	TI High Performance Flow	8	8	8 Cu + 1 Al
	Microprocessor Flow	9	11	10 Cu + 1 Al
Circuit FOM	Low Power Flow	20%	12%	23%
	TI High Performance Flow	20%	20%	~20%