

# Control Law Accelerator Boosts Digital Power Performance

*Platform of cost sensitive, high performance switching regulators*

*While adoption of digital control techniques for switched power supplies may never be universal, interest has been steadily growing in the subject and commercial digital microcontrollers are now beginning to appear with features optimised for power supply control. This short article describes a new feature which significantly reduces control loop latency and extends the performance of the digital controller in power supply applications.*

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In digitally controlled switched mode regulators, the control law is normally required to execute at the switching frequency. For example, a buck regulator switching at 200kHz would require a digital controller to sample and convert an output voltage, compute a digital control law, and deliver an updated PWM duty cycle every 5 $\mu$ s. This imposes a limit on the amount of time available for the controller to process each incoming analogue sample. As switching frequencies increase, the available processing time for each sample becomes smaller and the performance of the digital controller becomes more critical.

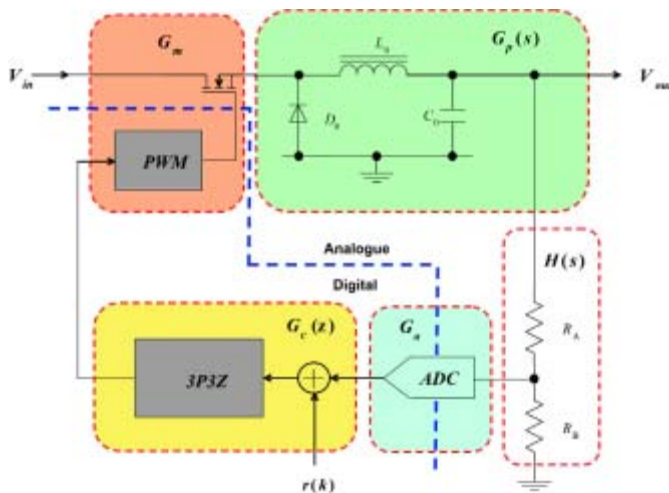
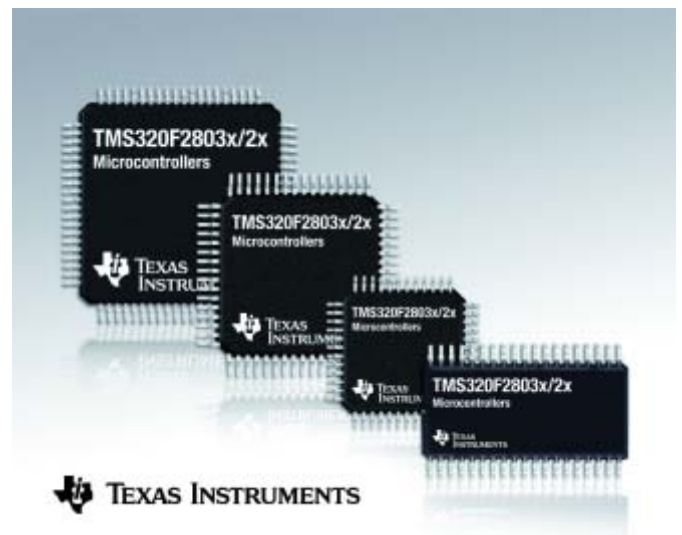


Figure 1: block diagram of a typical buck regulator

Figure 1 shows a block diagram of a typical buck regulator with a digital 3-pole, 3-zero control law. Signal flow through the digital controller – from analogue input to PWM output – involves three integrated components: an analogue-to-digital converter (ADC), the Central Processing Unit (CPU) “core” which computes the control law, and a PWM pattern generator. In this article, we will focus on the influence of the controller core on regulator performance.

Controller cores are often characterised by execution speed expressed in MHz or MIPS, but this can be very misleading. CPU performance is strongly affected by both the architecture of the core and the type of code being executed: some cores are designed for



general purpose programs, while others are optimised for specific types of algorithm, such as image or speech processing, or real-time control. Whatever the architecture, the CPU will take a finite time to collect the ADC sample, compute the control law, and deliver the result to the PWM generator. This computational delay effectively limits the duty cycle range and can significantly degrade regulator performance or even cause instability.

Figure 2 shows a timing diagram for one possible switching strategy for the buck regulator using trailing edge modulation. The output voltage is sampled during the low part of the PWM signal (indicated by the red arrow) and converted into a numerical value by the ADC. The CPU then computes a control law based on this sample and writes a modified duty cycle at the point indicated by the blue arrow in the timing diagram. The update delay, comprising ADC conversion time and computation of the 3P3Z algorithm, is shown by the time interval marked  $t_d$  in the diagram. In many systems it is important for the new PWM duty cycle to appear during the same period in which the output is sampled. Failure to do so adds a complete PWM cycle to the update delay, adding phase lag to the open loop response which erodes phase margin.

To allow for very small duty cycle values, the update point must occur before the next low-to-high transition of the PWM. This means the sample point must be placed at least  $t_d$  in advance of the next rising edge, restricting the maximum duty cycle ( $D_{max}$ ) which can be supported by this strategy. In cases where sample takes place in the high portion of the PWM, the minimum achievable duty cycle is restricted in a similar way. It is therefore important to minimise update delay as far as possible, both by using a fast ADC and by optimising computation of the control law.

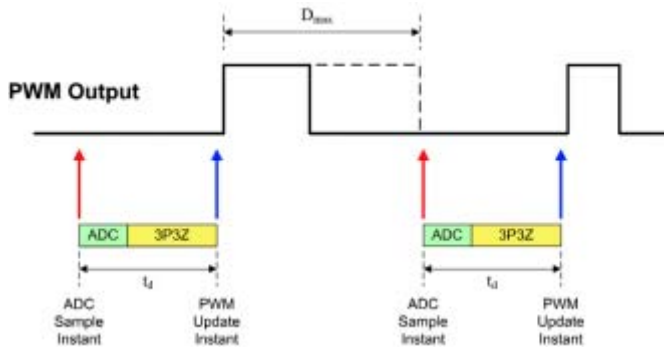


Figure 2: Timing diagram for one possible switching strategy for the buck regulator

Rapid computation of the control law becomes even more critical if multiple loops are to be controlled or when additional functions such as power factor correction must be supported by the same device, since more computational “work” has to be done in the same time. Furthermore, the digital controller often performs a range of background tasks, such as communications, fault monitoring, and data logging, which add to the computational burden on the controller and limit performance still further.

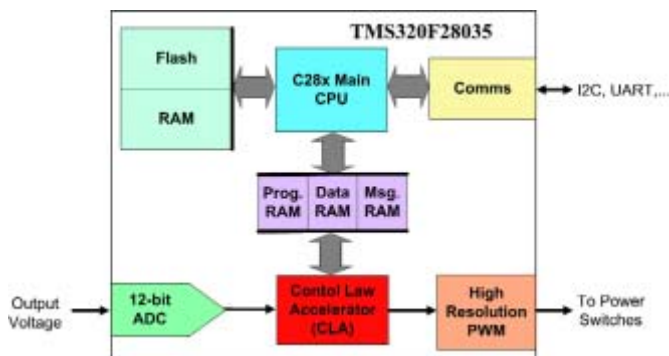


Figure 3: Block diagram of the CLA concept

A novel approach to the problem of computational delay has recently been implemented on a low cost digital controller. The TMS320F28035 from Texas Instruments incorporates a “Control Law Accelerator” (CLA) which takes the form of a separate CPU core optimised to compute the control law. The CLA executes time critical control algorithms in parallel with the main controller core which, with no real-time deadlines to meet, is free to perform supervisory and management tasks unhindered, increasing the range and complexity of background functions which can be supported.

A block diagram of the CLA concept is shown in Figure 3. The CLA is based on a 32-bit floating-point DSP core which uses the IEEE 754 numeric format. User code is loaded into shared RAM memory during device initialisation, from where it executes at the full device speed of 60 MHz. Programming the CLA can either be done manually or using a library of pre-written modules supplied with the device. Communication with the main core is achieved using blocks of shared RAM, allowing the main core to modify compensator parameters and data without disturbing the control loop.

In contrast with the main core, the CLA does not use interrupt service routines (ISRs) to achieve synchronisation with hardware. Program execution is divided into a number of software “tasks”, each mapped to a user defined hardware event such as a timer event or an ADC conversion result becoming available for processing. Up to eight separate tasks can be scheduled to run on the CLA, allowing multiple independent control loops or phases to be supported at the same time.

Some digital power supply controllers use parallel hard-wired compensators to compute the control law in parallel with a modest performance CPU. However, a major benefit of the CLA used on the F28035 is that it is fully programmable, allowing the user to freely define the compensator structure.

In our buck controller example, the 3-pole 3-zero control law code would be loaded into fast internal RAM memory from where it can be executed at the full device speed of 60MHz. A timer, phase locked with the PWM waveform, triggers the ADC to sample and convert the output voltage. As soon as the result becomes available, the CLA begins computing the control law and writes a new duty cycle into the PWM pattern generator. On completion of the control law, the CLA enters a “sleep” mode, consuming negligible current from the processor supply until triggered by the next conversion cycle. An enhancement which further reduces update delay is a “just in time” feature, which allows the CLA to capture the latest conversion result during the same clock cycle it becomes available from the ADC. Compared with traditional interrupt based schemes, the CLA approach greatly reduces sample-to-output delay and jitter.

In addition to the CLA, the F28035 also contains a powerful high-resolution PWM generator, capable of modulating pulse width, frequency and phase with a nominal edge resolution of 150ps. The modular PWM generator design enables complex switching patterns to be constructed to support practically any power supply topology. The device also includes high speed 12-bit ADC with sophisticated event trigger structure, making it the perfect platform for development of cost sensitive, high performance switching regulators.

Detailed information on the TMSF28035 device and Control Law Accelerator can be found at:

[www.ti.com/piccolo](http://www.ti.com/piccolo)