Texas Instruments
Technology Day Rochester 2009
Session Titles and Abstracts

Track & Course	Abstracts
Track 1 – Power-Supply Solutions	
Introduction to DC/DC Converter Topologies for Portable Applications	The wide variety of power-management solutions available to the designer keeps growing, particularly in integrated devices. The simplicity of the integrated converter may raise questions on how to properly test your solution; all of these questions will be addressed in this session. After a thorough review of the buck converter, we will explore other power-conversion topologies, including inductive boost, switched capacitor, SEPIC and buck/boost.
LED Lighting Power Solutions	With the rapidly expanding use of LEDs in such applications as torch lights, video displays, general lighting and many others, designers need to familiarize themselves with the component of the LED system that is getting less attention —the LED driver. This session will cover the aspects of an LED lighting system that make its drive circuitry different from that of a typical power supply. We will present typical devices used in AC/DC and DC/DC LED drivers, battery-powered drivers, RGB LED displays and LED backlighting. This session will also cover where to find additional information and what devices upcoming from TI will help to solve customer LED-lighting issues.
Battery Characteristics, Safety, Cell Balancing and Cell-Based Thermal Sensing	The lithium-ion (Li-Ion) battery has gained great popularity in recent years as the market for battery-powered portable devices has rapidly grown. The Li-Ion battery has superior characteristics, including high gravimetric and volumetric energy density, low self-discharge and no memory effect. On the other hand, it requires mandatory safety features because of its sensitivity to overcharging and high temperature. In this session we will discuss the characteristics and safety of rechargeable batteries; emerging battery chemistries such as $LiFePO_4$ and $LiMn_2O_4$; and design considerations for connecting battery cells in parallel or in series in applications. New trends toward designing safer battery solutions with longer battery life, such as advanced cell-balancing technologies and cell-based thermal monitoring, will also be discussed.
Minimizing High-Frequency Noise from Switch-Mode Power Supplies	With high efficiency, small size and ease of use, switching power supplies are now finding a place in virtually every application. However, switching power supplies may produce conducted or radiated noise that interferes with surrounding circuits in some applications that are noise-sensitive or that require regulatory testing for high-frequency emissions. This session discusses sources of high-frequency noise, common system-level noise problems, and methods to reduce noise in switching power supplies.
Introduction to Digital Power — TMS320C2000™ and UCDxxx Solutions for Point-of-Load and AC/DC	This session will present the basic control-loop theory used in digital-power solutions and its application in various point-of-load and AC/DC topologies. You don't have to be a C programmer to implement many of these solutions. Learn more about the advantages of digital power and the types of designs that benefit most from the technology.

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Track 2 – High-Speed Analog	
Clock Overview— Understanding Common Clock Parameters and Solutions	This session will present an overview of system clocking, including clock classification, PLL and non-PLL buffers, clock generators, and clock processing and signaling levels. We will also discuss typical clock parameters like jitter, skew, propagation delay and duty cycle.
Solving Common Design Issues in High-Speed Analog-to-Digital Converters	This session examines and offers solutions for some of the real-world, practical issues that commonly plague the application of ADCs. This session is for designers who already have a working understanding of data-conversion fundamentals. We will treat subjects such as clocking and jitter, driving the analog input, driving/capturing digital data effectively, and layout considerations.
High-Speed Layout Considerations	In this session we will discuss models of common components used in high-speed data converters and will offer guidance on the key points to address in creating a successful layout. We will also discuss when to use ground planes and when to clear them; optimum circuit routing; bypass capacitors; avoiding ground loops; vias; and controlling impedance with transmission-line techniques. In addition, many high-speed signal chains involve a mixed-signal boundary where the analog domain crosses into the digital domain. This session will help you know what factors to consider when domains cross.
What is SuperSpeed USB (USB 3.0) and What Can I Do with It?	With the announcement of the next evolution in USB-wired connectivity, SuperSpeed USB, you may be asking, "What is this? And what can I do with it?" The first part of this session will look at what is new about SuperSpeed USB and why it is better than USB 2.0 beyond the obvious speed increase. The session will also discuss how backward compatibility is being maintained, as this will be critical to the continued success of USB with end users who believe that "USB is USB." The second half of the session will discuss what applications will benefit from this new technology, and an early look at the SuperSpeed USB product roadmap will be presented.
ESD Protection: Protecting the Complete System	Semiconductor chips based on advanced low-voltage, small-geometry process nodes enable miniaturization, more power savings and better economy of scale. However, system-level ESD protection at the interface connector is particularly challenging and becomes even more difficult as the process geometry gets smaller. Popular choices for enhancing system-level ESD protection include external ESD clamp circuits and integrated protection devices. This session will cover key system-level ESD challenges and common techniques for overcoming them. We will also discuss TI's integrated passive devices (IPDs) and selecting the right ESD clamps for a given application.

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Track 3 – Wireless Solutions	
RF Basics	This presentation gives an overview of a complete RF system as well as an introduction to its different building blocks. Important parameters such as sensitivity, selectivity, output power, and link budget are discussed in detail. Finally, compliance to frequency regulations around the world is discussed.
Designer's Guide to Low-Power RF	This session walks you through the common decisions you must make when defining and creating a low-power wireless solution. We will discuss various network topologies, protocols (including standards like ZigBee ®), regulatory compliance, design, production and test considerations.
Improving the Range of Your Low-Power RF Designs	How far can it go? This session will present the standard calculations for estimating the range of an RF system. We will review link budgets and LNA and PA solutions and will touch on modulation schemes, forward error correction, path loss and network repeaters. We will also discuss a variety of design enhancements and trade-offs that can improve the range and throughput of an RF system.
An Introduction to Antennas and the Theories Behind Them	The antenna can be one of the most daunting components of low-power RF design. Most information available relates to larger antennas for ham radio or cellular applications. This session covers the basics you need to know to decipher the data-sheet information available and select the appropriate antenna for your application.
RF Transceiver Signal-Chain Design Considerations and Architectures for Broadband Wireless and Multicarrier, Multimode Wireless Infrastructure Systems	This session will discuss the latest cellular base-transceiver-station (BTS) and broadband architectures for multicarrier, multimode, wireless applications such as point-to-point microwave radio relay, digital repeaters, military radio, and software-defined radio. Three different RF architectural approaches will be explored: superheterodyne, high-IF heterodyne and direct conversion. The design challenges and trade-offs of these approaches will be examined, followed by a summary of the unique advantages of a direct-conversion radio architecture. The session will also cover the latest products for high-performance RF, clock synthesis, and high-speed data conversion.

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Track 4 – Precision Analog	
Op Amp Stone Soup: A "Cookbook" Collection of Single-Supply Op Amp Circuits	This session offers a "stone soup" collection of useful op amp circuits to solve linear application problems on a daily basis. Each op amp circuit (shown in an included TINA-TI™ SPICE schematic) is presented as a definition by example, with a brief overview of its functionality, applicable transfer function and/or waveforms, and key equations for rescaling the function to the exact application. A sampling of the "ingredients" includes the following circuits: • Voltage-to-current conversion • Drive circuits: Bridge-tied-load circuits, parallel op amps, high-current cascade reference buffers • Translation circuits: Single-ended to differential, differential to single-ended, differential input to differential output • Conditioning circuits: Full-wave rectifier, supply splitter, integrator amp in feedback, isolation amplifier, G = 1/G = –1 amp • Comparator circuits: AC-coupled circuits, comparator with hysteresis
Tackling EMI and RFI at the Board and System Level	Electromagnetic interference (EMI) and radio frequency interference (RFI) can affect any system in an undesirable manner as the proliferation of unintentional radiators and receptors continues to increase. EMI and RFI, which are undesirable by-products of electrical systems, produce a wide range of frequency spectra that can affect otherwise properly operating circuits. This session will review the fundamental principles of radiated interference and coupled interference along with the respective limits allowed for each. Techniques to mitigate the effects of interference on transmitters and receivers will be discussed, and other solutions covered will include effective power-line filtering, proper filtering for input signals of high-gain circuits, and details on key components. Finally, we will discuss the common rules of thumb for wire and PCB routing to minimize EMI and RFI effects. This session will provide some basic methods that will help reduce sources and receptors of EMI and RFI events in and near your circuits.
Audio Codec Solutions with Mini-DSPs and PurePath™ Studio	The latest generation of TI audio codecs, processors, touch-screen controllers and ADCs has specialized mini-DSPs built in for increased functionality and flexibility. Learn the capabilities of this audio-processing technology and see a demonstration of TI's configuration software, PurePath Studio. By just dragging and dropping popular audio algorithms into this GUI interface, you can let your codec do more of the processing work to create your own solutions without any programming.
Operation and Measurement of Class-D Audio Power Amplifiers	This session is intended for designers who are new to using class-D audio power amplifiers. The basic operation of these amplifiers will be explained, and techniques that must be used to accurately measure their performance will be presented.
Op Amp Noise Calculation, Simulation and Measurement	This session will cover the calculation, simulation and measurement of intrinsic noise, which is noise generated by resistors, op amps and other active devices in the circuit. Specific real-world examples will be presented to show how peak-to-peak output noise is predicted and measured. External noise such as RFI and EMI will not be covered.

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Track 5 – Embedded Processing	
Introduction to Code Composer Studio™ v4.0	Code Composer Studio (CCS) v4.0 is becoming the standard integrated development environment (IDE) for all of TI's embedded processors —from high-performance DSPs to ultralow-power MSP430s. Based on the open-source Eclipse platform, CCS v4.0 provides a universal tool set for development and can be easily extended with user-created plug-ins.
OMAP35x Hardware and Software Overview	This session will provide a detailed software- and hardware-architecture tutorial for TI's OMAP35x devices. OMAP35x applications processors offer a variety of combinations of the ARM® Cortex®-A8 core, multimedia-rich peripherals, OpenGL® ES 2.0 compatible graphics engine, video accelerators, and TMS320C64x+™ DSP core. You will also learn more about the TI software Framework, which supports the ARM, DSP, and ARM+DSP-based processors available from TI. Using application programming interfaces (APIs) for I/O (drivers) and the video, imaging, speech, and audio (VISA) algorithms, you can easily access the potential of TI's DSP processors and hardware accelerators within your Linux/ARM programs. This session includes a Linux review, an introduction to TI's Codec Engine along with its VISA classes, and an explanation of the purpose of xDAIS/xDM algorithm interfaces. TI processor options supported by the framework will be discussed, along with an overview of how the Codec Engine supports remote procedure calls (RPCs) from the ARM to the DSP.
Introduction to Stellaris® ARM Cortex-M3 MCUs	TI's Stellaris MCUs pair the ARM Cortex-M3 core with advanced communication capabilities, including 10/100 Ethernet MAC+PHY, CAN, USB On-The-Go, USB host/device, SSI/SPI, UARTs and I^2C. TI also provides an extensive range of over 20 reference designs and evaluation and development kits starting at $49. Stellaris MCUs are targeted at highly connected applications including monitoring, building controls, network appliances and switches, factory automation, electronic point-of-sale machines, test and measurement equipment, medical instrumentation and gaming equipment. This session will provide an overview of Stellaris MCUs, software tools and kits, StellarisWare™ software, and applications. We will close with a free-form Q&A session to handle your questions on the more than 140 microcontrollers in TI's Stellaris family of MCUs.
FRAM: The Future of Embedded Memory for Microcontrollers (MSP430)	Ferroelectric random access memory (FRAM) is the next-generation, low-power, fast nonvolatile-memory technology for embedded-microcontroller applications. Requiring no battery to retain data, it enables easy data access and features fast-write capability like DRAM. In addition, its ability to perform write operations at 1.5 V eliminates the need for an expensive charge capacitor that other nonvolatile-memory technologies such as Flash or EEPROM require. FRAM supports practically unlimited data-write cycles, unlike EEPROM or Flash, and this combined with its low power consumption and high reliability makes it ideal for sensing, data logging, motor control, and security applications. TI has over nine years of experience with FRAM and has successfully produced large FRAM memory modules of up to 4 Mbytes.
Digital Motion Control System Design—From the Ground Up *Presented by D3 Engineering*	D3 Engineering staff will present a design outline and demonstrate working hardware for a 400-W permanent magnet synchronous motor (PMSM) controller. Topics covered will include processor selection, isolation, interfaces (USB, CAN, RS-232) and driver electronics (power modules versus discrete FETs). The design is controlled through a TI F2806 DSP. D3 will demonstrate how to create a project for a custom board with MATLAB® real-time workshop tools. The demos will include both sensored and sensorless control algorithms.

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