Texas Instruments
Tech Day San Jose 2009
Session Titles and Abstracts

Track & Course	Abstracts
Track 1 (Day 1 & 2) Low-Power Wireless	
Getting Started with the TI Low-Power RF Portfolio	This presentation serves as an overview of the parameters and considerations a designer would use to select a low-power wireless (LPW) solution. It also highlights the devices and tools from TI and how they fit in a typical LPW design.
Fundamentals of Antenna Design *by LS Research*	Antenna design is one of the most intimidating and important parts of any RF design. It is critical to understand the key factors involved when choosing an antenna topology as well as what tools are needed for design, simulation and characterization. Designs must account for the effects of the enclosure material, the available space, the required radiation patterns, EMC compliance rules and regulations. This presentation discusses the fundamentals of antenna design for short range devices, as well as the tradeoffs between size, cost and performance. An antenna that is properly designed and optimized will enhance the overall performance of any radio.
RF Software System Design	How to write low-power RF software? Low-power RF protocol design from scratch: Periodic transmitter, polling receiver and TDMA. Power optimization, protocol considerations, design, debug and test. Specific low-power features of LPRF chips are explored: Wake-on radio (WOR), fast startup from sleep and low-power modes.
RF4CE and the RF-Based Remote Control Market	This presentation provides an overview of the emerging RF-based Remote Control Consumer Electronics market, specifically addressing the recently published RF4CE standard being driven by Sony, Samsung, Panasonic, and Philips. In addition to discussing this vertical, we will drill down into the HW and SW solutions available, as well as the kits, demo's, reference designs, application notes, and additional collateral material available to get our customers to production in this market quickly and at minimum cost.
Techniques for a Compliant RF Design *by LS Research*	This session will outline the importance of RF component selection and PCB layout techniques and how they can be instrumental in achieving regulatory approval and optimal design performance. This will include a brief discussion on the pros and cons of using RF modules, reducing risk with compliance prescans and the insight provided through measurement of antenna radiation patterns.

Texas Instruments
Tech Day San Jose 2009
Session Titles and Abstracts

Track & Course	Abstracts
Track 2 (Day 1 & 2) Interface & Clocks	
Circuit Isolation Techniques and Implementations	Multiple options are now available to electronics designers to implement galvanic isolation. Apart from isolation technologies like capacitive, optical and inductive/magnetic to choose from, they must also contend with the various isolation standards regarding voltage ratings and creepage/clearance distances. This discussion intends to simplify the decision making associated with choosing the right isolation solution.
Interfacing Between LVPECL, VML, CML and LVDS Levels	This session introduces the various interface standards used today in modern telecom and datacom systems and describes the methods used to interface between similar and different I/O structures used on TI serial gigabit solutions products. The main logic levels discussed during this session are low-voltage positive/pseudo emitter-coupled logic (LVPECL), current-mode logic (CML), voltage-mode logic (VML) and low-voltage differential signaling (LVDS). This session focuses on these four logic levels, because they are now the most prevalent in today's communications systems. The different SERDES devices from TI, from input/output structures, various high-speed drivers and receivers, receiver biasing, and termination schemes are discussed. Explanations and examples on how to interface different types of drivers and receivers using ac-coupling are also given.
Advantage and Flexibility of Programmable Clock Drivers	The ongoing shift towards faster systems is propelling the need for a new class of clock circuits, which enable better timing performance, lower jitter, EMI reduction and improved functionality. This session focuses on the advantage of programmable clock generators, explaining: • How to replacing crystals by PLL? • EMI reduction by spread spectrum clocking. • Low-phase noise clock generation from crystal (for Ethernet, etc.). • Who or what needs VCXO input?
Networking Clock Solutions – LAN/WAN Clocking Techniques	Networking equipment frequently has a need for clock muxing different frequencies to meet a given system application. Traditional methods involved two different clock oscillators and a clock mux device. For LAN applications, a typical 156.25-MHz clock is needed, and for WAN applications a 155.52-MHz clock is used. Due to the low jitter and accuracy needed for these clock oscillators, the cost of these oscillators may be high. To obtain lower cost but maintain the low jitter, high accuracy, and clock muxing in a single solution, TI has the answer.
Tackling EMI and RFI at the Board and System Level	Electromagnetic Interference (EMI) and Radio Frequency Interference (RFI) can affect any system in an undesirable manner as the proliferation of unintentional radiators and receptors continue to increase. EMI and RFI, an undesirable byproduct of electrical systems, produce a wide range of frequency spectra that can affect otherwise properly operating circuits. During this seminar hour, we will review the fundamental principles of radiated interference and coupled interference, along with the respective allowed limits for both of these interference sources. In this discussion, we will describe transmitters and receivers along with techniques to mitigate the effects of both culprits. The solutions we will cover will be effective power-line filtering, proper filtering for input signals of high-gain circuits, and details on key components. Finally, we will discuss the common rules of thumb for wire and PCB routing to minimize EMI and RFI effects. With this seminar you will see some basic methods that will help reduce sources and receptors of EMI and RFI events in and near your circuits

Texas Instruments
Tech Day San Jose 2009
Session Titles and Abstracts

Track & Course	Abstracts
Track 3 (Day 1 & 2) Signal Chain 1	
High-Performance Differential ADC Input Interface Design	Most emerging high-performance ADCs require a differential input interface. Designing that interface with minimal SFDR and SNR loss from the converter specifications is a task every data acquisition designer must face. A review of converter SNR and SFDR characterization will lead into a discussion of combining the SNR and SFDR delivered up to the converter with the ADC specifications. This can then be used to set a performance target in this last stage interface. Working from low-to-high frequency then, a very low distortion interface suitable for 16- to 18-bit converters will be shown. Next, a wideband first Nyquist zone design will be described and finally a high-performance IF interface for an under-sampled application will be described.
Clocking to Maximize High-Speed Signal-Chain Performance	Selecting a clock driver for a high-performance sampling system involving high-speed data converters is a hard task and often underestimated. It is especially harder for an analog-to-digital converter (ADC). If the ADC fundamentals are well understood, it makes the job of identifying required clock driver performance easier. Such a clock driver can be a simple (non-PLL) clock-distribution circuit, clock generator/synthesizer or jitter cleaner. A clock driver can do the signal processing such as frequency integer or fractional multiplication and division, level translation, skew control, etc. The higher the input frequency of an ADC, the more important the sampling clock jitter becomes and need to be kept at levels of the ADC's internal aperture jitter to achieve best possible SNR (and SFDR). This presentation will address sampling clock dependencies on the ADC performance metrics (namely SNR and SFDR), explain methods to calculate required sampling clock jitter, introduce TI high-performance synthesizers/jitter cleaners and show demonstrations of achieving best possible SNR (and SFDR) with such cost effective yet high-performance clocking devices.
Designing with High-Speed DACs and Solving the Analog Interface	A typical transmit chain, whether it be in a communications application like VDSL, test and measurement application like arbitrary waveform generator, or one of many others, starts with a DAC followed by a signal processing chain. The purpose of this presentation is to discuss key performance criteria of the signal chain and how to select components to meet them. We start with an overview of DAC specifications like sampling, images, SNR, SFDR, current sinking versus current sourcing and compliance voltage, and op-amp specifications like bandwidth versus gain, noise, distortion, input/output voltage range, and inverting versus non-inverting. Next we discuss how to translate and combine specifications to estimate the overall performance of the signal chain. To conclude, we get to the nuts and bolts of how to design around very high-performance DACs like the DAC5682Z, which has complementary current outputs. We derive the design equations required to achieve gain matching from each output and convert to a single-ended voltage and consider how to implement DAC reconstruction filtering. The presentation uses the TSW3070 16-bit 1-GSPS DAC5682Z evaluation platform to demonstrate operation and give examples of performance. Two computer design tools are provided and illustrated; an Excel spread sheet for component calculation and a TINA-TI™ spice file for circuit simulation.
High-Speed Amplifier Design Considerations	Voltage feedback (VFB) and current feedback (CFB) amplifiers are the two most common high-speed op-amp architectures in use today. This presentation develops VFB and CFB models from simplified schematics, and shows the impact on amplifier circuit design, feedback and stability, and highlights the similarities and differences. Application comparisons are shown to point the designer to the right type of op amp given the application they are developing. The presentation then shows how these principles are applied to high-speed op-amp PCB layout giving practical dos and don'ts of high-speed layout.
High-Speed Data Converter Tools	With modern high-performance DAC sample rates at 1 GHz and similarly, ADC sample rates at 500 MSPS; many customers may have challenges evaluating such high-speed parts. The high-speed data-converter team has developed a series of hardware and software tools to make it easier to demonstrate and evaluate TI's DAC and ADC portfolio. This seminar will provide relevant training on how to use the TSW3100 pattern generator and the TSW1100 logic analyzer, so you can effectively demonstrate high-speed data-converter products to your customers and assist them with their evaluations.

Texas Instruments
Tech Day San Jose 2009
Session Titles and Abstracts

Track & Course	Abstracts
Track 4 (Day 1 & 2) Signal Chain 2	
Designing Mixed-Signal Systems with Noise Reduction Techniques in Mind	Sensor applications often have low-level signals. A peaceful co-existence of the sensor signal, analog circuitry, and processor requires careful attention to layout and noise reduction techniques. In this session we will discuss three sources of noise, the paths noise travels and how to reduce noise to tolerable levels. We will discuss the proper selection and placement of noise isolating and limiting components to keep analog and digital noise out of sensitive input circuits.
Optimizing Your SAR-ADC Design	The most popular and versatile Analog-to-Digital Converter (ADC) has a Successive Approximation Register (SAR) topology. These converters work by comparing an analog voltage signal to known fractions of the full-scale input voltage and then setting or clearing bits in the ADC's data register. Modern SAR converters use a Capacitive Data Acquisition Converter (C-DAC) to successively compare bit combinations. Usually these devices have an integrated sample/hold input function. It is common to use an operational amplifier (Op Amp) to directly drive the input of a SAR Analog-to-digital converter (SAR-ADC). Although this configuration is an acceptable practice in manufacturer's data sheets, it has the potential to create circuit performance limitations. For optimum performance, C-DAC SAR-ADCs require the correct front-end buffer and filter. The additional input filter or RC-network will relax the driving Op Amp requirements. This presentation details the reasons for an input filter and buffer amplifier to the C-DAC SAR-ADC along with an analytical approach to selecting the filter components and op amp characteristics.
Optimize Your Delta Sigma – Mux System with Low-Latency Strategies	Small-signal sensors often generate slow-moving dc signals. For these types of sensors, the delta-sigma (ΔΣ) analog-to-digital converters (ADCs) eliminate most of the analog input circuitry by providing a complete, high-resolution, low-noise solution. Some systems have multiple sensors generating low-frequency signals. This situation may require a high-resolution, low-noise ADC with a multiplexer at its input. Even though the sensors at the input of the multiplexer in these systems present low-frequency (nearly dc) signals, switching from channel to channel creates the need for an ADC that is capable of a high-speed response. This session focuses on how to use latency issues with ΔΣ ADCs in multiplexed systems to your advantage.
Advanced TINA SPICE Simulation	You can use this class to expand your knowledge into TINA's advanced simulation capability. In this class we will look deeper into the power behind the Transient, AC, Monte Carlo Analysis and Parameter Stepping tools. In addition you will learn how to build your own macro-models. We will achieve this depth using definition by example, rules-of-thumb and simulation tricks. When you finish this class you will be able to take full advantage of the power of the full version of TINA SPICE to expedite and simplify complicated analysis.
Evaluating Analog-to-Digital Converters with ADCPro™	When you consider an analog-to-digital converter (ADC) for a new design, you can get a rapid assessment of the device with an evaluation board (EVM). If you intend to view collected time-domain, histogram, or FFT data, the new ADCPro software from TI will ease your evaluation. During this session we will identify the appropriate test equipment for your EVM and introduce basic ADC evaluation test methods. We will show how ADCPro will simplify the tasks of collecting and analyzing ADC data.

Texas Instruments
Tech Day San Jose 2009
Session Titles and Abstracts

Track & Course	Abstracts
Track 5 (Day 1 & 2) Power Management	
The Magic of Multiphase – A Comparison of a 2-Phase DC/DC Power Supply versus a Similar Single-Phase Controller Highlighting the Trade-Offs and Challenges of Each Design	Several multi-phase DC/DC controllers have recently been introduced by TI (and competitors) that promise more than a higher-output current capability. A multi-phase and single-phase design with the same output voltage and current are constructed and analyzed to compare and contrast the trade-offs of size, ripple, component choice, efficiency and size. Learn when to recommend a multi-phase over a single-phase solution and how to extract its value based on the designer's system requirements.
Battery Fundamentals	Definition of basic battery performance parameters; overview of performance tradeoffs for different chemical systems (for example – Li-Ion, NiMH, NiCd, PbSO4 and disposable ZnMnO2 alkaline cells); physical construction of different battery systems and how this affects application-performance criteria for selecting the type and configuration of batteries for a specific application; safety, transport and disposal issues associated with batteries; charging methods for different battery systems cycle-life impact of battery management implementations and storage conditions
Power-Supply Layout Considerations	This topic will address methods for keeping circuit parasitic components from degrading the operation of your designs. Techniques to minimize the impact of parasitic inductance and capacitance of filter components and PWB traces will be discussed, together with a description of the impact that PWB trace resistance can have on power-supply regulation and current capacity. A general overview of thermal design is also included as well as sample temperature rise calculations in a natural- and forced-air environment. Finally, some practical examples of power-stage and control-IC layouts are reviewed.
Digital-Power UCD Buck Converter	Digital power technology promises to revolutionize the way power architectures are designed. In this session, we will review TI's latest product developments along with the theory of digital control. System-level benefits and application examples will also be covered along with device configuration details using an intuitive graphical user interface (GUI). A product demonstration using the Fusion Digital Power™ Design Tool and the UCD9240 evaluation board will be given
Meeting Battery Power Management Design Challenges	Battery operated devices require safe reliable systems, longer run-time, and simultaneous system operation while charging in a deeply discharged or defective battery. This session starts with the battery charger front end over-voltage and over-current protection which prevents failure due to the use of unregulated, inexpensive adapters. We will then cover power-path-management charging technology for charging the battery while powering the system. To avoid shutdown surprises from a depleted battery, many mobile applications depend on accurate remaining capacity information. An accurate gas gauge can predict the remaining capacity allowing the system the most out of the battery. We will show how the TI patented Impedance Track™ technology addresses this issue

Texas Instruments
Tech Day San Jose 2009
Session Titles and Abstracts

Track & Course	Abstracts
Track 6 (Day 1) Embedded Processors Workshop	
Understanding 32-Bit MCU Peripherals Advanced Capability in Embedded Systems using the Piccolo™ MCU ControlSTICK *(Part 1)*	This hands-on workshop will provide an overview of the Piccolo MCU C28x™ core and a deep dive into the functionality and benefits offered in its feature-rich peripheral set optimized for real-time control applications. With the use of labs, attendees will gain insight into the onboard ADC, ePWM, HiResPWM, analog comparator and more. Sample projects include generation of an asymmetric PWM output with period and duty variation, triggered ADC conversion using an onboard filtered PWM output, use of comparators to generate a CPU interrupt on a cycle-by-cycle basis and more. Attendees will leave with a comprehensive understanding of the performance and capability offered in the Piccolo MCU series of devices.
Understanding 32-Bit MCU Peripherals Advanced Capability in Embedded Systems using the Piccolo MCU ControlSTICK *(Part 2)*	This hands-on workshop will provide an overview of the Piccolo MCU C28x core and a deep dive into the functionality and benefits offered in its feature-rich peripheral set optimized for real-time control applications. With the use of labs, attendees will gain insight into the onboard ADC, ePWM, HiResPWM, analog comparator and more. Sample projects include generation of an asymmetric PWM output with period and duty variation, triggered ADC conversion using an onboard filtered PWM output, use of comparators to generate a CPU interrupt on a cycle-by-cycle basis and more. Attendees will leave with a comprehensive understanding of the performance and capability offered in the Piccolo MCU series of devices.
Hands-On OMAP™-L1x Boot-Camp *(Part 1)*	The OMAP-L137 is a low-power applications processor based on an ARM926EJ-S™ and a C674x DSP core. The OMAP-L137 features robust operating systems support, rich user interfaces, and high processing performance life through the maximum flexibility of a fully integrated mixed processor solution. This hands-on workshop will provide attendees with a detailed technical overview of the device's architecture and will cover supporting hardware/software such as the Linux Boot process and Codec Engine/ DSPLink functionality.
Hands-On OMAP-L1x Boot-Camp *(Part 2)*	The OMAP-L137 is a low-power applications processor based on an ARM926EJ-S™ and a C674x DSP core. The OMAP-L137 features robust operating systems support, rich user interfaces, and high processing performance life through the maximum flexibility of a fully integrated mixed processor solution. This hands-on workshop will provide attendees with a detailed technical overview of the device's architecture and will cover supporting hardware/software such as the Linux Boot process and Codec Engine/ DSPLink functionality.
Hands-On OMAP-L1x Boot-Camp (Part 3)	The OMAP-L137 is a low-power applications processor based on an ARM926EJ-S™ and a C674x DSP core. The OMAP-L137 features robust operating systems support, rich user interfaces, and high processing performance life through the maximum flexibility of a fully integrated mixed processor solution. This hands-on workshop will provide attendees with a detailed technical overview of the device's architecture and will cover supporting hardware/software such as the Linux Boot process and Codec Engine/ DSPLink functionality.

Texas Instruments
Tech Day San Jose 2009
Session Titles and Abstracts

Track & Course	Abstracts
Track 6 (Day 2) Embedded Processors Workshop	
MSP430F5xx Hands-On Workshop *(Part 1)*	This hands-on workshop is intended to educate the experienced MCU designer on the capabilities of the MSP430F5xx and learn first hand how to use them. You will experience embedded design with the MSP430, get familiar with an MSP430 development environment, learn where to find and how to use resources and better understand the MSP430 low-power concept. The course is perfect for those getting started or who want a refresher on MSP430. Basic experience with general MCUs and knowledge of assembler- and C-language programming is assumed.
MSP430F5xx Hands-On Workshop *(Part 2)*	This hands-on workshop is intended to educate the experienced MCU designer on the capabilities of the MSP430F5xx and learn first hand how to use them. You will experience embedded design with the MSP430, get familiar with an MSP430 development environment, learn where to find and how to use resources and better understand the MSP430 low-power concept. The course is perfect for those getting started or who want a refresher on MSP430. Basic experience with general MCUs and knowledge of assembler- and C-language programming is assumed.
Hands-On OMAP Lab *(Part 1)*	This session will provide a review of the ARM Cortex-A8 core, graphics engine, C64x+™ DSP core, and on chip peripherals. Attendees will learn how to get up and running with the OMAP EVM. Key features of the Cortex A8, Neon, 3D graphics, IVAHD will be demonstrated.
Hands-On OMAP Lab *(Part 2)*	This session will provide a review of the ARM Cortex-A8 core, graphics engine, C64x+ DSP core, and on chip peripherals. Attendees will learn how to get up and running with the OMAP EVM. Key features of the Cortex A8, Neon, 3D graphics, IVAHD will be demonstrated.
Hands-On OMAP Lab *(Part 3)*	This session will provide a review of the ARM Cortex-A8 core, graphics engine, C64x+ DSP core, and on chip peripherals. Attendees will learn how to get up and running with the OMAP EVM. Key features of the Cortex A8, Neon, 3D graphics, IVAHD will be demonstrated.

Texas Instruments
Tech Day San Jose 2009
Session Titles and Abstracts

Track & Course	Abstracts
Track 7 (Day 1) High-Performance Processors	
Getting to Faster Performance with Serial Rapid IO™	Today's technologies require very high data rates to move into and within the processor cluster. Serial Rapid IO (sRIO) is able to move data rates up to 3.125 Gbps in each direction per lane. Faster interconnect implementations such as sRIO are especially important for any high bandwidth application needing dependable data transmissions. This session will provide an overview of how to implement your applications using the Serial Rapid IO interfaces found on TI's high-performance processors.
Understanding Virtualization for TI's C64x™ Devices	Today virtualization technology is reducing the cost of servers in the IT industry. Virtualization technology has also been extended on TI DSPs for embedded applications. VLX for Embedded Systems allows Linux and TI DSP/BIOS™ to run on a single core concurrently allowing the user to implement real-time applications on TI DSP/BIOS and general-purpose applications on VLX Linux . VLX virtualization allows each operating system to run independently of one other, and uses its own scheduling, drivers and memory management without sacrificing real-time performance. This session will present practical tips for using this technology to lower the cost of your embedded system.
Power and Thermal Considerations for TI's DM6467	As integrated circuit (IC) components become more complex, the challenge of producing an end equipment product with good thermal performance also increases. To address this challenge, TI provides a Power and Thermal Spreadsheet for its embedded processors. This spreadsheet simplifies the task of designing systems to account for the worst-case power and thermal characteristics of an embedded processor. This session will walk though the various features of the Power and Thermal Spreadsheet for the DM6467 embedded processor and provide a demonstration of how these features enable a simplified approach estimating device power and thermal performance.
Tutorial on the New Code Composer Studio™ v4.0 and Software Libraries – Get Coding in Record Time	This session will provide a demonstration and tutorial on the new Code Composer Studio v4.0, as well as explain TI's software libraries. Code Composer Studio version 4.0 is based on the Eclipse opensource software framework. Eclipse is becoming very popular in the embedded development community and is now becoming a standard in development environments. To further simplify system design efforts, TI has many software libraries written and available for the C64x+ DSP. These libraries are typically used in computationally intensive real-time applications where optimal execution speed is critical. One example of these libraries is TMS320C64x+ IMGLIB. TMS320C64x+ IMGLIB is an optimized Image/Video Processing Functions Library for C programmers using TMS320C64x+ devices.
Tips and Tricks for Increasing Performance with TI's Multi-Core Embedded Processors	Multi-core architectures provide the resources needed to manage today's real-time performance density demands. TI's multi-core architectures are cost, power, and board-space efficient when compared to using multiple single-core solutions. This session will provide attendees with a technical primer for navigating their way in these complex environments. Learn how to run multiple instances of an application while taking advantage of shared resources. Also, addressed are tips for effectively splitting an application across multiple cores and using development tools for these types of environments.

Texas Instruments
Tech Day San Jose 2009
Session Titles and Abstracts

Track & Course	Abstracts
Track 7 (Day 2) Video Processors	
The Ins and Outs of TI's Video Interfaces	TI has several embedded processing solutions tailored for digital video applications. They consist of integrated processors, software, tools and support to aid in simplifying the design process and accelerate innovation. In this session, attendees will learn how to leverage the video port interfaces on digital media devices in order to interface to popular video displays.
Implementing High-Definition Codecs Using DM6467	TI's DM6467 is finely tuned to handle complex video applications. The DM6467 can offload video encoding/decoding tasks from the DSP core to the HD Video Imaging CoProcessor (HD-VICP) allowing more DSP MIPS to be available for common video and imaging algorithms. This session will cover the capabilities of encoding/decoding HD content along with information on available libraries to reduce time to market for video applications. A demo will be shown during this session.
Image Pipe (IPIPE) Overview	The Image Pipe (IPIPE) is a programmable hardware image processing module on DM35x that generates image data in YCbCr-4:2:2 format from RAW CCD/CMOS data. This session will provide a overview of the IPIPE and explain how to use and optimize for your image sensor and application.
HD On-Screen Display Using DM6467 and DM6437	The TI DM6437 has hardwired On Screen Display (OSD) acellerators which can be leveraged in conjuntion with the DM6467 device to do high-definition (720p) decode and OSD. The OSD engine is capable of handling two separate video windows and two separate OSD windows. This session will be an overview of how this can be done and highlight reference designs available to use in your application.
Multi-Channel Video Aggregation for Digital Media Products	TIs digital media processors have many video port configurations tailored at different video end segments. This session will provide an overview of the video port configurations across the digital media product portfolio in the context of handling multiple video streams concurrently.

Texas Instruments
Tech Day San Jose 2009
Session Titles and Abstracts

Track & Course	Abstracts
Track 8 (Day 1) Low-Power Processors and Microcontrollers	
Breaking the mW/MHz Mindset: How to Navigate TI's Processor Portfolio	This session will explain how TI's low-power processors map to end application needs. Topics such as fixed-/floating-point decisions, performance benchmarks, peripheral throughputs, driver availability and features, and getting started with EVMs will be covered. Additionally, this session will show detailed, high-level block diagrams and side-by-side comparisons between new and legacy processors to get the customer started. As a result of attending this session, the attendee will understand which TI processor(s) are right for their application(s) and how to get started today.
Understanding the Elements of On-Chip Power	Embedded power consumption can vary widely depending on how the on-chip resources are used. Thus, power consumption cannot be estimated accurately without an understanding of the components in use and the usage patterns for those components. By providing the usage parameters that describe how and what is being used, accurate consumption numbers can be obtained for power-supply and thermal analysis. This session is intended to provide a detailed discussion of on-chip resources and how they impact overall chip power. Attendees will also be provided with an overview of TI's power estimation spreadsheet.
CC430: MCUs for Space Constrained, Ultra-Low-Power, Wireless Applications	The CC430 platform is a highly integrated, monolithic SoC based on the industry-leading MSP430 MCU architecture and TI's ultra-low-power RF solutions. By making RF design easy, small, performance-rich and power-efficient, the CC430 platform helps advance applications including RF networking, energy harvesting, industrial monitoring and tamper detection, personal wireless networks, automatic metering infrastructure (AMI) and heat cost allocators.
Integrated USB Connectivity with MSP430 MCUs	Modern MSP430s have integrated USB peripherals allowing for serial communication over a single plug-and-play cable, intelligent human interface devices like mice and keyboards that don't require driver installation, or mass storage devices for data retention. MSP430 devices that feature a USB peripheral will be discussed as well as the software USB stacks required to create USB applications.
Implementing Digital Motor Control with High-Performance Low-Cost MCUs	In this presentation, we will discuss the capability of using a low-cost Piccolo 32-bit MCU in advanced motor control. We will demonstrate the usage of a single Piccolo MCU to control multiple motors with advanced vector motor control algorithms such as Field Oriented Control (FOC). In addition, the same Piccolo MCU device is used as the controller for the front-end Power Factor Correction (PFC). An introduction of basic motor types, motor drive inverters, and motor control methods will also be presented. The goal of this presentation is to equip customers with both advanced and introductory knowledge of advanced motor control and the value of TI's low-cost motor-control MCUs.

Texas Instruments
Tech Day San Jose 2009
Session Titles and Abstracts

Track & Course	Abstracts
Track 8 (Day 2) Application Processors and Microcontrollers	
10 Reasons You Should Use OMAP 3 in Your Next Design	OMAP applications processors offer a variety of combinations of the Cortex-A8 core, multimedia-rich peripherals, OpenGL® ES 2.0 compatible graphics engine, video accelerators and TMS320C64x+™ DSP core. The modular and extensible OMAP35x evaluation module (EVM) provides all the components needed to start developing today on the OMAP3503 processor including an OMAP3503 Linux board support package based on the 2.6.22 kernel. Join this session to get an overview of this device's features and capabilities. The attendee will learn how to evaluate OMAP-3 fit for their application (processor and accelerator performance benchmarks, throughput analysis, peripherals, drivers, etc.)
High-Speed Board Design Considerations for OMAP	The OMAP35x BGA package was designed to simply board layout. However, when trying to maximize performance, they can be sensitive to certain hardware design pitfalls. This session will provide a primer and offer recommendations on routing a BGA package. Also outlined are common high-speed issues and recommendations are given for avoiding common problems. Specific examples will be given using TI's OMAP35x and will address memory interfacing, camera interfacing and USB.
Implementing Smart and Flexible Power-Line Modem for AMR/AMI and Industrial Applications on TMS320F28x 32-Bit controllers	Power Line Communication (PLC) is booming and becoming a popular communication solution to implement remote control. The TMS320F28x 32-bit microcontrollers from TI enable developers to implement flexible and smart PLC modems in software for narrowband solutions (up to hundreds of kbps) and provide the unique opportunity to integrate the primary application on the same device if desired. This presentation will highlight system implementation examples, share new developments TI is pursuing in PLC and show developers how to get started today on PLC modem development with the F28x.
FRAM: The Future of Embedded Memory for Microcontrollers	FRAM (Ferroelectric Random Access Memory) is the next-generation low-power, fast non-volatile memory technology for embedded-microcontroller applications. Requiring no battery to retain data, it enables easy data access and features fast write capability like DRAM. In addition, its ability to perform write operations at 1.5 V eliminates the need for an expensive charge capacitor that other current non-volatile memory technologies such as Flash or EEPROM require. FRAM supports practically unlimited data write cycles unlike EEPROM or Flash and this combined with its low power consumption and high reliability makes it ideal for sensoring, datalogging, motor control and security applications. TI has over nine years of experience with FRAM and has successfully produced large FRAM memory modules up to 4 MB.
C2000™ MCU Digital Power Solutions: AC/DC and DC/DC	Digitally controlled power conversion is the enabling force of efficiency and performance improvement in today's power-supply and power-conversion designs. This presentation will focus on introducing TI's latest development solutions for both AC/DC rectifier power supply and DC/DC converters including Power Factor Correction (PFC), phase-shifted DC/DC, and highly efficient resonant DC/DC, etc. An introduction of basic power-conversion concepts and topologies such as PFC, DC/DC, interleaved PFC and DC/DC, and resonant DC/DC, will also be presented. Attendees will learn basic and advanced digital power-conversion concepts and gain an understanding of TI's digital power solutions.

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