Synergy between innovative telecom start-up and leading silicon vendor results in revolutionary platform designed to handle access services and transport in a single high-density, economical enclosure.

When Calix set out to create a simplified services platform that would integrate all of the functionality required to deliver voice, data, and video services to both business and residential customers in a single enclosure, it turned to Texas Instruments, an industry-leading application-specific integrated circuit (ASIC) vendor.

Calix started developing the C7 in 1999 and knew from the beginning that it would need a highly integrated, power-efficient ASIC solution to support one of the key elements of the platform: the high-speed SERDES (serializer-deserializer) backplane. At the time, SERDES was only being used for core switches and routers – Calix was the first developer to extend use of the high-speed backplane technology to achieve massive density in its access chassis. SERDES helped eliminate the need for bulky parallel buses which allowed Calix to increase the capacity of the C7 platform without increasing the size of the shelf.

Teaming with the SERDES leader
Texas Instruments offered Calix SERDES expertise and a leading-edge CMOS process. It was clear that TI was the industry leader in integrating high-performance SERDES interfaces onto ASIC devices since it was the first vendor to announce the availability of SERDES cells in its ASIC libraries, and to have already provided multiple generations of integrated and discrete SERDES functions. Calix knew TI would be the right vendor to team-up with to create the C7 platform’s backplane ASIC.

By leveraging TI’s expertise, Calix was able to develop two different types of ASICs for the C7 – a switch and a line unit. With the switch ASIC, TI and Calix managed to integrate 22 SERDES channels onto a single chip, each capable of transmitting 3.125 gigabits per second (Gbps) of data across the backplane. The line unit ASIC required the integration of two SERDES channels as well as two ARM microprocessors to control the backplane. As an ARM licensee, TI was able fulfill this requirement, saving Calix the time and resources that would have been necessary to license the technology themselves.

Memory and millions of gates of logic were also included in both ASICs resulting in space savings that enabled Calix to put transport-scale capacity of 220Gbps in a flexible access enclosure. Calix’s revolutionary platform provides services ranging from simple POTS and DS0 up to OC-48 and Gigabit Ethernet directly to the customer. The C7’s design allows scaling of up to 88 SERDES channels, and the company has the option of building future Line Units for OC-192 and 10-Gigabit Ethernet operation, depending upon customer demand.

Success Story
Texas Instruments Develops ASIC Solution to Support Calix’s C7™ Simplified Services Platform SERDES Backplane

The Challenge
Calix, a telecom equipment supplier, needed an ASIC vendor with SERDES integration expertise to build a high-speed telecommunications backplane designed to support extremely high capacity levels as well as access services in a compact platform. Additional Calix requirements included:

- Integrated ARM microprocessor from a licensed supplier
- A leading-edge CMOS process that balances high performance processing capability with low power consumption and a low noise signature.
- Support for industry-standard ASIC design tools

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- Support for industry-standard ASIC design tools
Collaboration brings success
Calix’s collaboration with TI proved to be a success in the telecommunications market. By the time Calix had introduced its C7 simplified services platform in February 2003, it had already deployed over 500 units to more than 50 customers. Today, Calix’s success continues to grow and the company is already engaged in another ASIC design with TI.

“TI had the technology we needed, and they were eager to work with us,” said Jason Dove, director of technology at Calix. “With its ASIC libraries, processes and flows, as well as development support and other products, TI enabled us to get the C7 platform into the marketplace much faster than we could have with any of the other ASIC suppliers we considered.”

Meeting additional requirements
TI’s underlying CMOS process technology offers a high level of processing performance at very low noise and power levels – key performance criteria for high-density telecom equipment. TI’s process roadmaps lead to cost reduction with even higher levels of performance for the future enhancement of Calix products.

TI’s depth of technology and broad product portfolio also made a difference. When Calix started the design, TI’s ASIC library for its 180-nanometer (nm) CMOS process was still in development. But Calix was able to work out much of its design using TI’s discreet SERDES devices based on its 250-nm ASIC library, and then migrate the design to the 180-nm library when it became available. In addition, discrete SERDES devices from TI allowed Calix to verify its backplane design with FPGA logic, saving development time later on after the ASIC was built. In another part of the system, Calix made use of TI’s broadband solutions for the C7’s ADSL line card, taking advantage of yet another of TI’s core technologies.

“We were excited about working with Calix because they wanted to leverage our technology and expertise to the fullest,” said Steve Sutton, vice president of the TI ASIC business. “Calix not only wanted to push our SERDES integration to what was the limit at that time. They also wanted to make optimum use of our process technology and other capabilities.”

TI’s support of industry-standard ASIC tools accelerated the development flow and saved non-recurring engineering (NRE) costs for Calix. Less duplication of effort was involved than would been the case with proprietary tools, allowing Calix designers to handle more of the flow themselves and stay closer to the development of the ASIC device throughout the process.

Committed to the future
Calix is already engaged with TI on building new ASICs for its next product generation. As CMOS geometries scale to 130-nm, 90-nm and beyond, Calix will continue to benefit from TI’s expertise of combining density and speed with low power consumption at a competitive cost. Calix is committed to continuing the simplified access revolution it began with the C7 simplified services platform. Leading-edge manufacturing processes, ASIC libraries and other technologies from TI will help Calix keep that commitment.

Defining Success
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