

Topic 1

Improving Power Supply Efficiency – The Global Perspective

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ABSTRACT

There should be no question that we have seen increasing importance placed on efficiency as a goal in power supply design. This topic addresses the incentives for this emphasis, both market driven and regulatory, by describing some effective voluntary programs and reviewing the status of developing governmental requirements. A review of contributors to power losses will be given together with design techniques and suggestions for minimizing their impact with new power supply architectures.

I. INTRODUCTION

Energy efficiency has always been a consideration in the design of power supplies. After all, losses in the conversion of power from a primary source into that necessary to meet specific system load requirements serve no value to the system and, in fact, impose an added cost to both the system and its user. It was largely the quest for improved efficiency that drove the transition from linear regulators and 50/60 Hz power transformers to high-frequency switching technologies.

However, that quest remains unabated today with perhaps even greater urgency, as we see ever-increasing world-wide demands for electrical power coupled with diminishing availability of low-cost fossil fuels to generate that power. Some of the statistics that have been generated to illustrate the need for improved electrical efficiency include the following:

- Today there are over 10 Billion electronic power supplies in use world wide, more than 3.1 Billion just in the United States. The typical efficiency of these power supplies lies within the range of 30% to 60% today.
- Energy consumed internally in these power supplies amounts to some 110 to 150 Billion kWhrs/year, representing a loss of ~3 to 4% of the total electricity usage in the U.S.

- Increasing the average efficiency of these power supplies by just 10% would:
 - Reduce lost power by 30 Billion kWhrs/year, which in turn would
 - Save approximately \$3 Billion per year
 - An amount equal to the cost of building 4 to 6 new generating plants
- Savings attributable to the Energy Star program in 2005 have:
 - Saved more than \$6.8 Billion in consumer energy bills
 - Saved enough electricity to power 8.2 Million homes
 - Reduced generating emissions equivalent to removing 15.2 Million cars

And, of course, the United States is not alone in coping with these numbers. In fact, the US may well be following the leads of many other countries in efforts to improve energy utilization, but the point is that today, improving electrical efficiency has become a world-wide issue. Fig. 1. is a collection of just some of the logos for governmental agencies established to encourage energy efficiency within their countries. The methods used in these endeavors range from education, through developing market incentives, to mandated regulations. Access to many of these agency's web sites can be made through the Power Sources Manufacturers Association (PSMA) via this link:

http://www.psm.com/index.php?directory=forums&area=forums&page=energy&which_tech=regs

 <p>European Code of Conduct</p>	 <p>EPA Energy Star</p>
 <p>Nordic Swan</p>	 <p>CA Energy Commission</p>
 <p>German Blue Angel</p>	 <p>China Energy Conservation Project</p>
 <p>Korea Energy Management Corp</p>	 <p>Japan Environment Association</p>
 <p>European Union Eco Label</p>	 <p>Australian Greenhouse Office</p>

Fig. 1. Logos representing a sampling of government agencies promoting improved energy efficiency throughout the world.

II. ACTIVE ENERGY-SAVING PROGRAMS

With many countries independently developing standards and programs for improving efficiency of power supplies, one would expect that there would develop a wide range of requirements and methods for implementation. Actually, much has been accomplished toward the harmonization of both test procedures and specifications through world-wide discussions and collaboration, although there are differences in plans for making these requirements mandatory.

Most countries have initially begun their efforts for higher efficiency with a “carrot” approach of education to develop consumer awareness leading to a demand for products earning a higher efficiency rating, and showcasing that accomplishment by the use of the applicable agency logo on the product’s packaging. The Energy Star label has been particularly successful in this endeavor within the US, and the resultant gains have been impressive. An excellent web site for exploring these activities can be found at: <http://www.efficientpowersupplies.org>.

This idea of a product marking approach to achieving continuous improvement through market incentives has been developed further by the Australian Greenhouse Office through a program designed for external, modular power supplies that establishes a scale of numerical grades for meeting a range of efficiency goals. The efficiency grade level earned for a particular product, indicated by a Roman numeral of I through VI, can then be incorporated into the product’s label as shown in Fig. 2. (Grade I means no efficiency specification, Grade III is equivalent to Energy Star Tier 1 requirements, Grades to VI are reserved for future improvements in performance).

III. MANDATORY STANDARDS

Voluntary programs of those mentioned above, as well as many others, have done much to raise general awareness while driving performance improvements in many specific applications. But since there is almost always some cost for improving efficiency, eventually we reach a position where the “carrot” of marketing pull must be aided with the “stick” of mandated requirements. These, of course, usually take the form of government specifications for equipment to meet specific limits of minimum energy efficiency. This is beginning to happen in China and Australia, with the United States not far behind with the 2005 Energy Policy Act including a provision tasking the Department of Energy to develop a mandatory US standard for power supplies. The California Energy Commission has acted faster by requiring that all external power supplies sold in that state must meet specified efficiency limits by July of 2006.



Fig. 2. The efficiency level of an external power supply can be evaluated by a prospective user through a Roman numeral marking on the name plate.

The levels are established by a measure of “Average Efficiency”, which is defined as the arithmetic average of efficiency measurements taken at 25%, 50%, 75%, and 100% of rated full power of the unit, and with a visible, quantitative indicator, users can compare efficiency on a par with other performance and cost parameters in making buy decisions. Many other countries are expected to join with Australia in applying this idea.

Another marketing incentive developed through Ecos Consulting, with support from the Energy Star group within the Environmental Protection Agency (EPA) and the California Energy Commission (CEC), has been named “80 Plus” and is specifically directed toward computer power supplies. This program has established a specific efficiency requirement of 80% at each of three load levels – 20%, 50%, and 100% of full load – plus an input power factor of at least 0.9. The incentive for meeting this requirement is a cash rebate to the manufacturer for each computer with a compliant power supply, of \$5.00 for desktops and \$10.00 for servers, sold into specific geographical regions. The funding for these incentives has been negotiated to come from the particular power utility serving those regions. And again, power supplies achieving this standard may wear a unique logo on their label, as shown in Fig. 3.

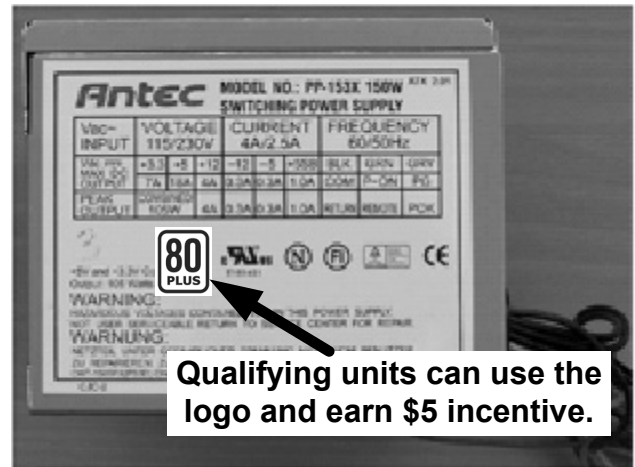


Fig. 3. The “80 Plus” program provides a cash incentive, as well as a marking indicator, for meeting a specific efficiency standard.

Of course, any organized attempt to impact the power supply industry broadly immediately runs into the reality of the breadth of this industry. Questions as, What types of power supplies?, What applications?, What power ratings?, What operating conditions?, and What test procedures? must be answered before even getting to the question of what the limits will be. But much work has transpired in addressing these issues.

Test specifications have been developed and harmonized between the various agencies for many applications. And the general philosophy has been to start with specific applications that have the potential for the greatest gain in overall energy savings, and then expand the program into areas that have the next-highest potential for energy reductions.

In power supplies, the first targeted application for mandatory standards has been external, or modular supplies, both ac/dc and ac/ac inverters with power ratings from zero to 250 Watts. The standard developed by Energy Star – with the participation of many other agencies - subdivides into two operating conditions: No Load (or Standby), where the criteria is in terms of input current (since the output current is zero), and Active Load, where efficiency is determined as the average of measurements at four values of load – 25%, 50%, 75%, and 100% of rated (nameplate) load. These requirements are summarized in Table I and Table II shown below.

TABLE I. NO LOAD REQUIREMENTS (STANDBY)

Nameplate Po Rating (W)	Maximum Input Power (W)
0 to 10	0.5 (Tier 2 proposed @ 0.3)
10 to 250	0.75 (Tier 2 proposed @ 0.5)

TABLE II. ACTIVE-LOAD REQUIREMENTS (AVERAGE 25% TO 100% LOAD DATA))

Nameplate Po Rating (W)	Maximum Efficiency (η)
0 to 1	49% x Po rating
1 to 49	49% + 0.09 x ln (Po rating)
49 to 250	84% (May be 80% with PFC)

IV. REQUIREMENTS FOR COMPUTER POWER SUPPLIES

The next application to be addressed by Energy Star (and others) is for power supplies internal to desktop computer systems. At the time of this writing, standards have been prepared in draft form with effectivity proposed for July of 2007. It should be noted that there will also be a requirement that no systems may be “grandfathered” – meaning that the entire supply pipeline must be cleared of non-conforming components to allow a computer to wear the Energy Star label after the effective date. A further tightening of this standard is tentatively proposed for January 2009.

The first version of this standard identifies four categories of computers: notebooks, desktop computers and servers, workstations, and integrated computers (computer and monitor in a single housing). Four operating conditions are also identified as:

1. **Standby (or Off) Mode** – The lowest power, non-user-controlled mode.
2. **Sleep Mode** – An automatic, but user defined, low-power mode with fast wake-up.
3. **Idle Mode** – The unit fully operational but inactive.
4. **Active Mode** – Doing useful work.

The “Standby Mode” is built into the computer and can remain active for an indefinite period of time when the system is connected to line power. The “Sleep Mode” can be either automatic or user defined to occur after a period of inactivity, but from which the system can quickly resume activity with inputs from a variety of interface devices. There may be multiple levels of “sleep” within a given system, but it is the lowest power mode to which these requirements apply. The “Idle Mode” is a new definition defining the condition when a user leaves the system while in the middle of a project. It is a subset of the Active Mode and is proposed with both an efficiency limit and a time limit (15 minutes) before automatically switching to a sleep

mode. The need for this mode stems from the fact that it is the state of most computers for most of the time. (Often with screen savers active.) A survey conducted by NRDC (Natural Resources Defense Council) justifying an idle state requirement is shown in Fig. 4.

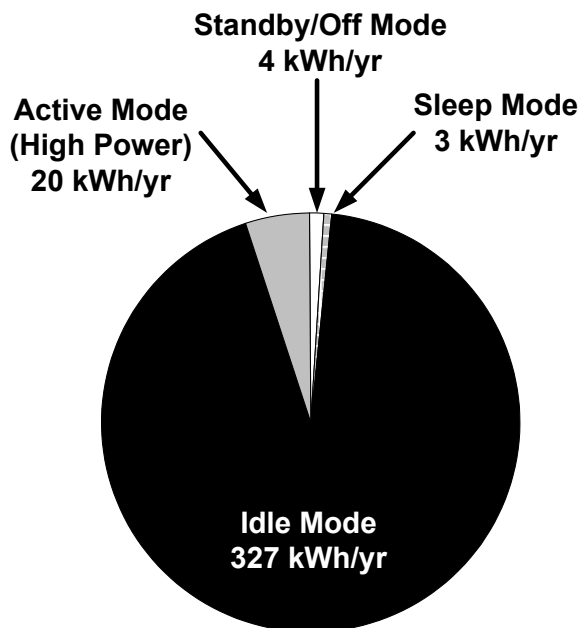


Fig. 4. Total annual energy consumption for typical commercial desktop: 354 kWh

So within these various types of computer systems, and with four modes of operation, the initially proposed requirements for internal computer power supplies are given in Table III.

(Note that at the time of this writing, Energy Star requirements for the Active Mode appear firm, while the lower-power modes are still under discussion).

V. POWER SUPPLY DESIGN ISSUES

While we have just discussed energy efficiency requirements for two specific applications above, it is clear that there will be a steady effort to address additional power systems in the future. One area, large data centers, are an obvious target, although in this market, line power availability and cooling considerations will drive improvements in efficiency without any governmental encouragement. However, lower power users in the consumer marketplace are also a sure bet for regulatory efforts because, even though many of these applications do not consume a lot of power individually, the numbers of units are huge. Television set top boxes and battery chargers are just two that will soon be addressed.

TABLE III. PROPOSED ENERGY CONSUMPTION LIMITS FOR COMPUTERS

Mode	Unit	Watts	Notes
Standby (Off)	Notebooks	0.5	Same as external power supplies
	Desktops & Workstations	2	
	Integrated Computers	3	
Sleep	Notebooks	5	Enter automatically within 15 minutes of inactivity
	Desktops & Workstations	5	
	Integrated Computers	7	
Idle	Notebooks	15	Solution to "network" problem TBD
	Desktops	50	
	Integrated Computers	52	
	Workstations	90	
Active	All with external supplies	Same as external power supply specifications	
	All computer with internal power supplies	80% minimum efficiency at 20%, 50%, 100% rated power plus power factor > 0.9 @ 100% load	

Thus, it would seem prudent that energy efficiency be considered in any new power supply development activity. But in reviewing the requirements that have already been published, it is easy to see that the challenges have become more complicated. As a minimum, a designer will not be able to consider his task completed just by meeting a specified efficiency number at nominal, or full power loading.

While full-load efficiency is important – as it always has been – if nothing else, efficiency requirements are demanding a flatter efficiency curve, with requirements at light loads as well, in order to accommodate the increasing standby modes of operation.

Note that while the requirements for external power supplies specify efficiency, averaging data taken at four different load values, the internal computer power supply document is being written with a minimum efficiency requirement given for *each* of four different loads. In either case, maintaining high efficiency at a load of 20% of full rating, represents a significant and challenging design task. And the problem is further exacerbated when the system under power can achieve a very low standby, or off state, so that “no load” operation also applies to the power supply.

Referring back to the requirements for external power supplies shown in Table I, a power supply designed for a load of as much as 250 W, must also meet a requirement of drawing less than a Watt of input power when the load goes to zero. With a 220-V AC line, that means the total input current must be less than 3 mA!

Clearly, there will be a cost for many of these benefits. The “tug-of-war” picture of Fig. 5. is used to illustrate the trade-off challenges facing every power supply designer. While there are many forces pulling on a designer to optimize some aspect of a given design, the three shown in the illustration are significant because they are each both important and conflicting. For example, with the emphasis on achieving the lowest cost, a given design cannot incorporate the multi-layer PC boards that would minimize the supply’s volume. Similarly, reducing the size of the components by increasing the switching frequency

will likely incur an efficiency hit. And power devices with the lowest conductive losses will cost more. The point of this exercise is to demonstrate that the industry’s past tendency to place low cost as an almost sole objective will need to be replaced with the goal of finding the lowest cost solutions that will ALSO meet specific and quantitative efficiency requirements. There is no one way to design a power supply. An optimum design must always balance several conflicting goals.

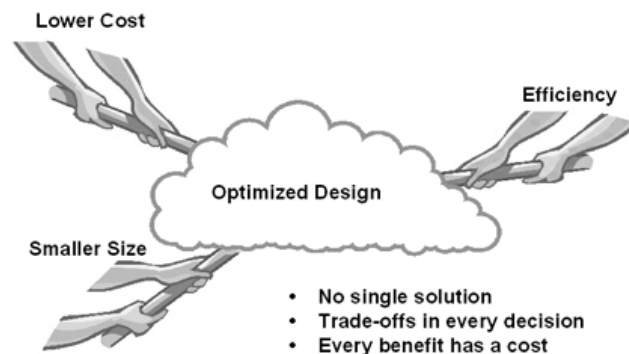


Fig. 5. No one way to design a power supply.

VI. MINIMIZING POWER LOSSES

Calculating losses in today’s power systems have become significantly more complicated with the advent of high-frequency switching technology, which has added the major contributors of switching losses to the simpler dissipation from current moving in a conductor. However, for an efficient design, every contributor to loss must be considered and decisions made as to whether improvements could be made. This analysis would consider such factors as: how the loss could be reduced, the impact on other elements of the design, the cost implication, and whether the gain justifies the change. The following is an overview of the most obvious potential loss contributors.

A. Conductive Losses

As stated above, power is dissipated (lost) when current flows through a conductive path that offers some resistance. The current can be either

DC or AC and in some components, such as magnetic devices, both have to be considered separately. If the resistance is linear, as it typically is in printed circuit traces, copper wire, the windings in magnetics, and the drain-source resistance of power MOSFETs, the loss term is just:

$$P = I^2 \times R \quad (1)$$

where the current can be steady-state dc, dc during a portion of a switching cycle where duty-cycle would be a factor, or the rms value of an ac current.

Note that resistance almost always has a temperature coefficient so temperature also becomes a contributor.

Where the resistance is non-linear, for example: the forward drop of a diode, the input-output differential of a linear regulator, or the supply current required by various elements of the control circuitry, the power loss is:

$$P = I \times V \quad (2)$$

where

- V is the voltage across the element caused by the current flowing through it.

B. Switching Losses

These are losses made much more significant as we move to higher and higher switching frequencies. They are generally caused by the sudden change in current caused by the turn-on and turn-off characteristics of a power switching device. With power MOSFETs, there are commonly three major contributors that cumulatively add to the total switching loss:

Gate Charge

$$P = V_{DRV} \times Qg \times f_{SW} \quad (3)$$

where

- V_{DRV} is the DC voltage supplying the gate drive circuitry
- Qg is the total gate charge required for switching the MOSFET
- f_{SW} is the switching frequency.

Drain Capacitance

$$P = 0.5 \times C_{DS} \times (V_{DS})^2 \times f_{SW} \quad (4)$$

where

- C_{DS} is the total capacitance from drain to source of the MOSFET
- V_{DS} is the voltage change across C_{DS} .

Switching Overlap

$$P = 0.5 \times V_{DS} \times I_{ON} \times t_{TR} \times f_{SW} \quad (5)$$

This term is topology dependent, caused by the presence of both voltage and current during a portion of a MOSFET's switching time.

To these losses, a designer must add the core losses in transformers and inductors, losses from recovery currents in switching diodes, losses from snubbing circuits, and losses induced by parasitic elements throughout the supply. Parasitic components such as stray capacitance and leakage inductance may not be lossy in themselves, but can store energy that is later transferred to a dissipative element elsewhere in the circuit.

C. Topology Considerations

While minimizing the component-by-component losses is important, there are many elements in these stringent new energy requirements that will require a higher-level solution – specifically addressing the basic architecture of the power system. It is clear that as we strive for higher switching frequencies, the fact that there is a frequency term in every switching loss equation means that these efficiency goals will be progressively more difficult to achieve, even at high power output levels. But with the requirement for high-efficiency at light loads as well, simple fixed-frequency operation over a wide load range is probably not possible. IC controllers have adapted with a variety of more sophisticated control algorithms – pulse skipping, frequency foldback, burst mode, or hysteretic, to name a few – that have the capability to lower the switching frequency of the controller as the loading is reduced. However, with these solutions have

come a new set of issues such as audible noise when the frequency is reduced, and the speed of light-load to full-load step recovery. Clearly, solutions can become complex.

The requirement for minimal input power consumption at zero load on the output – while maintaining the regulated output voltage level – becomes even more challenging. Techniques such as disabling unneeded functions, reducing the gate drive for the power devices, low current controllers, minimizing or eliminating start-up current sources, and developing lower current solutions for isolated feedback are all areas that will be explored and considered to meet these very stringent standards.

And then there is the basic power conversion topology itself to consider. Circuit techniques to minimize switching losses at higher frequencies have long been known but their added complexity limited their application when cost was the major issue. With the possibility that cost may become secondary to efficiency, renewed emphasis is

being given to solutions such as active reset, soft switching, and resonant operation. Additionally, the need for added complexity may give a substantial boost to the application of digital controls to power system designs, where microprocessor control can provide a ready answer to the problem of changing the algorithm to match changing system operating conditions.

But even remaining in the analog world, many gains have been made in the development of what have been called “Green-Mode” or “Efficiency-Optimized” controllers. A good example of this is the recently-released UCC28600 controller from TI, shown in Fig. 6).

This device, which is designed as a highly integrated controller for low-power, universal off-line converters offers the following features specifically optimized to meet the latest energy-efficient requirements with a wide margin to allow for further tightening of the requirements.

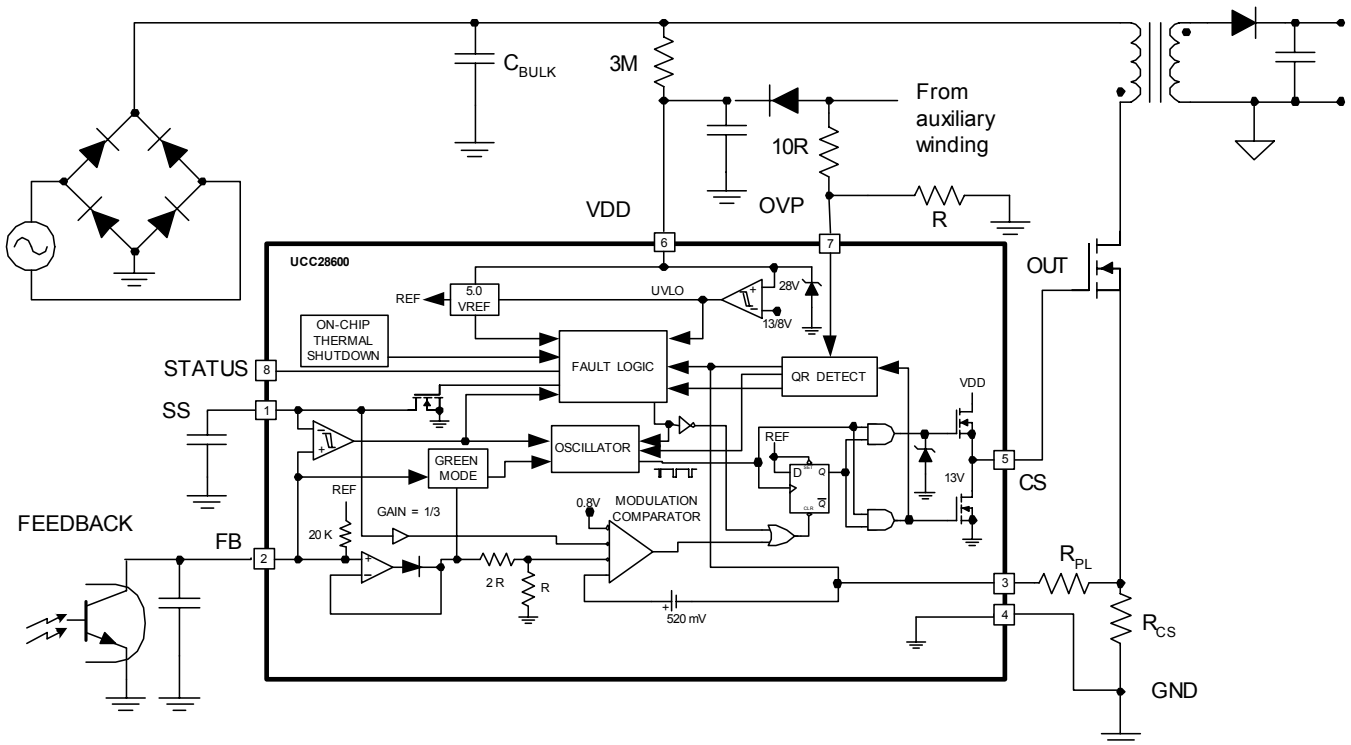


Fig. 6. UCC28600 Green-Mode controller.

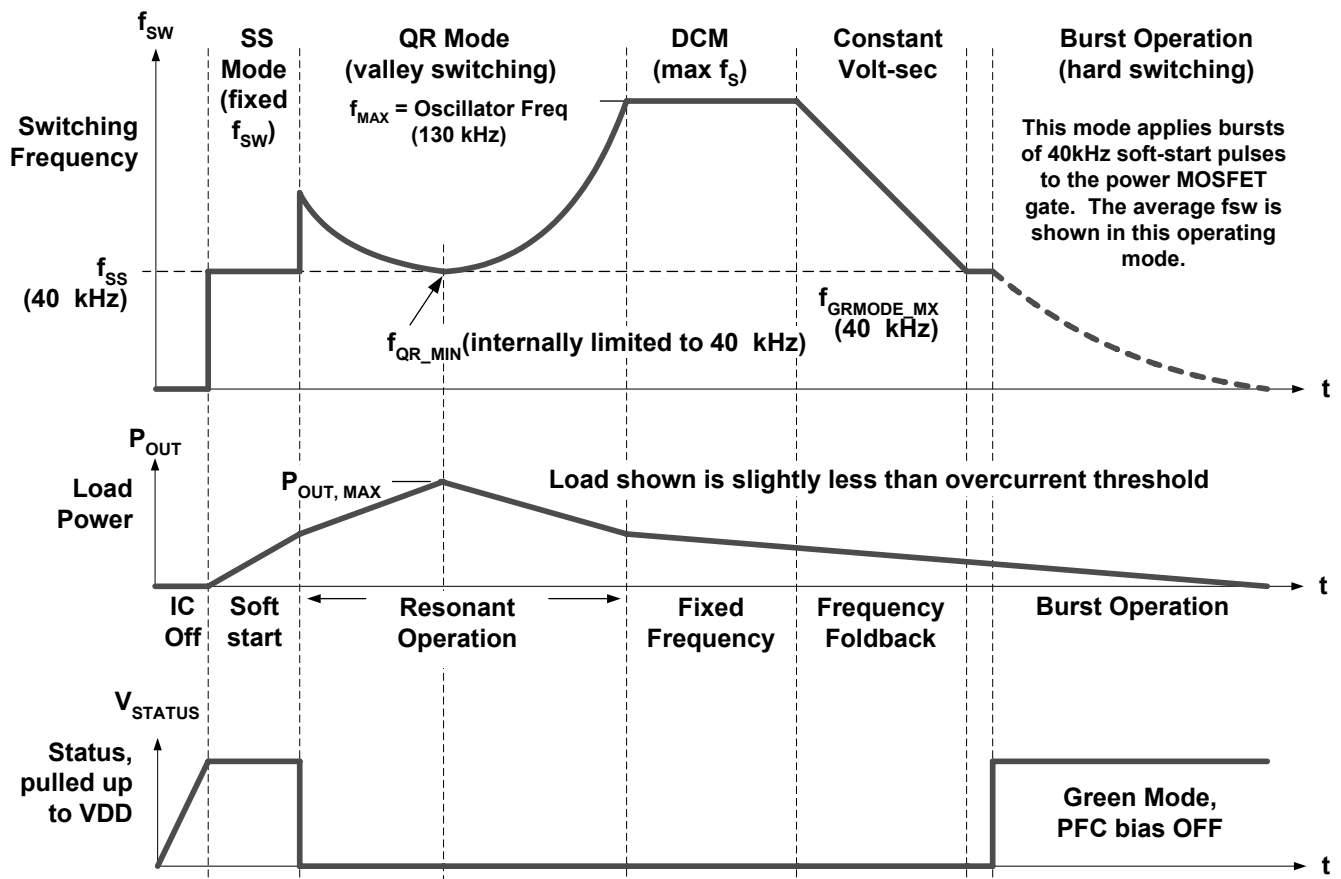


Fig. 7. UCC28600 operating modes.

- Low-current start-up and control (300-mW maximum input power at no load)
- Quasi-resonant operation at nominal load (variable frequency, valley-current switching)
- Frequency-clamped at 130 kHz (variable duty-cycle DCM operation)
- Constant volt-second operation at light load. (fixed pulse-width, extended off-time)
- Burst operation at standby load (40-kHz bursts as needed)
- A “Green-Mode” status pin useful for disabling functions unnecessary at light loads (PFC, for example)

The various operating modes of this device – and how they are related to the power supply load demand - are illustrated with the graphs of Fig. 7. In this illustration, time is arbitrary and the graphs are intended to show the relationship between switching frequency and load.

The UCC28600 represents just one of a wide variety of IC controllers that are – or will become – available to allow designers to create power solutions that will meet these demanding energy saving requirements. And they WILL be needed because energy efficiency will be needed. Not only because it will be government mandated, but also because it’s the RIGHT thing to do.

