Topic 2

Green-Mode Power by the Milli-Watt

Texas Instruments

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Michael Madigan, Texas Instruments

ABSTRACT

Recent regulations promote high power supply efficiency over wide-load ranges, and they impose limits for the maximum AC power during idle and no-load conditions. This work describes a power system architecture proposed to meet these new efficiency goals. The features of this architecture include a low power converter that operates in multiple modes that are determined by power demand, where each mode enhances the efficiency within its power range. A flyback converter is highlighted as the solution; it is controlled in burst, frequency foldback, discontinuous conduction, and quasi-resonant modes that are shown to enhance efficiency from no-load to full-load, respectively. In addition to the design steps, this topic also includes test techniques and performance verification.

I. GREEN-MODE POWER SYSTEM

Today's converters must operate efficiently from full-load to no-load. Converter efficiency is often judged as the average of the efficiency at 25%, 50%, 75% and 100% full rated load, between the AC line and the output of the converter.[1] An additional no-load AC line power criterion is further imposed on the converter in order to judge the conservation merits of the power converter. Thus, power supply efficiency and performance at light loads is as important as at full rated load.

Modern appliances such as battery chargers, personal computers, monitors, printers and televisions require a small amount of bias power so that they can quickly spring to life, perform their tasks and slip back into their idle state without operator intervention. Previously, idle state power was simply eliminated with an AC line switch; now, many modern systems must have regulated power available at all times. During idle states, the systems enter "sleep-modes" where they impose micro-watts of load on the DC converter output. During idle state, the seemingly small operational and parasitic losses in the power supply are the most significant loads that are ultimately imposed on the AC line. During full load operation, the mode of control must change in order to efficiently meet the power demand.

The power supply must have the ability to change modes of operation based on load in order to maximize efficiency over a broad load range. Often, the task of coordinating the different modes falls upon a primary-side controller, such as the UCC28600.

Furthermore, the power system architecture may need a small power supply to coordinate larger internal power supplies in order to reduce no-load power. Intuitively, it is easier to make a 50-W power supply have an idle power less than 500 mW than it is to make a 500-W power supply have an idle power less than 500 mW.

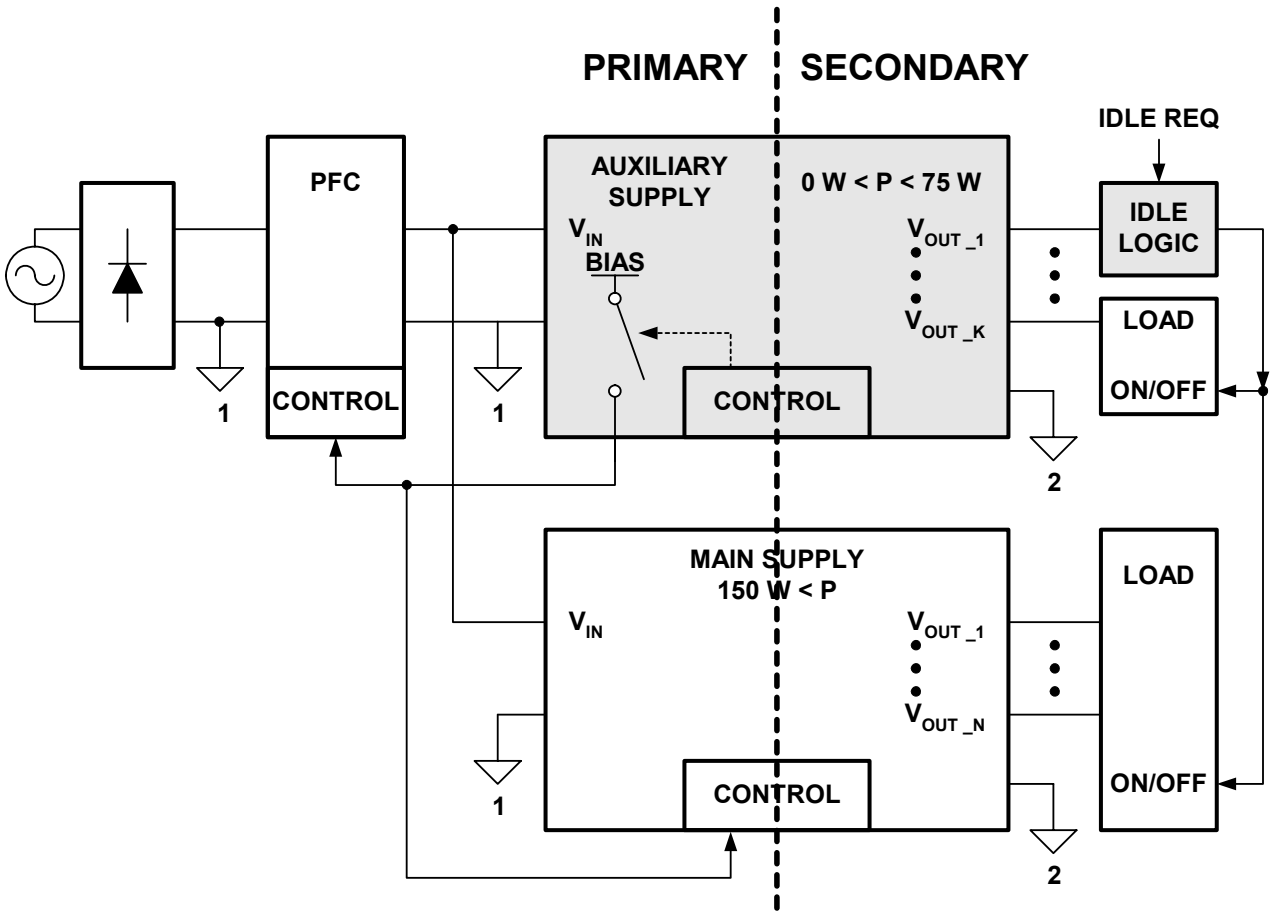

Fig. 1. High-power system architecture for green mode.

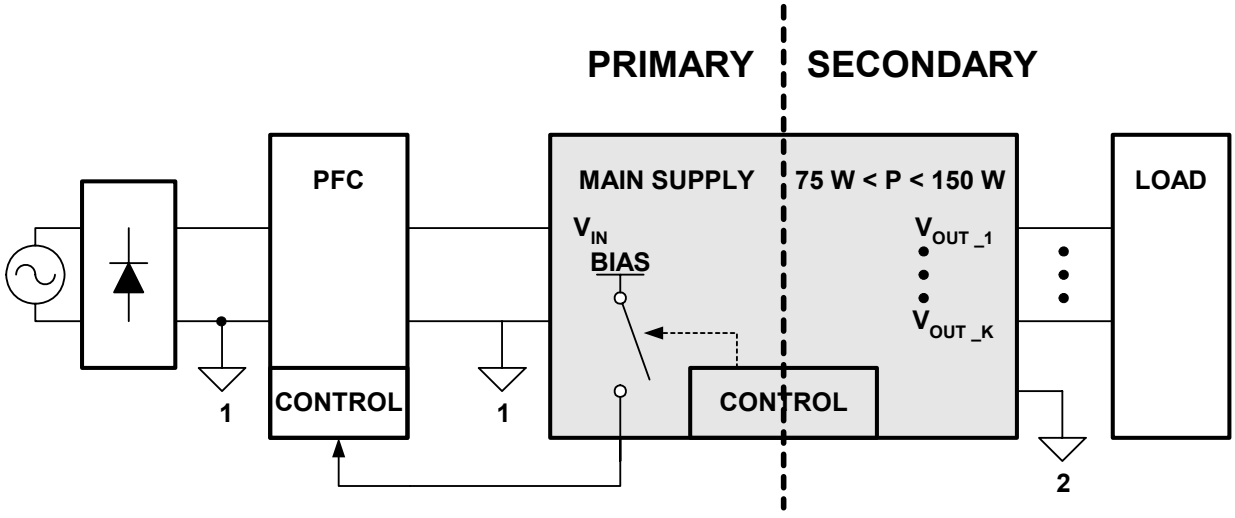

Fig. 2. Mid-power system architecture for green mode.

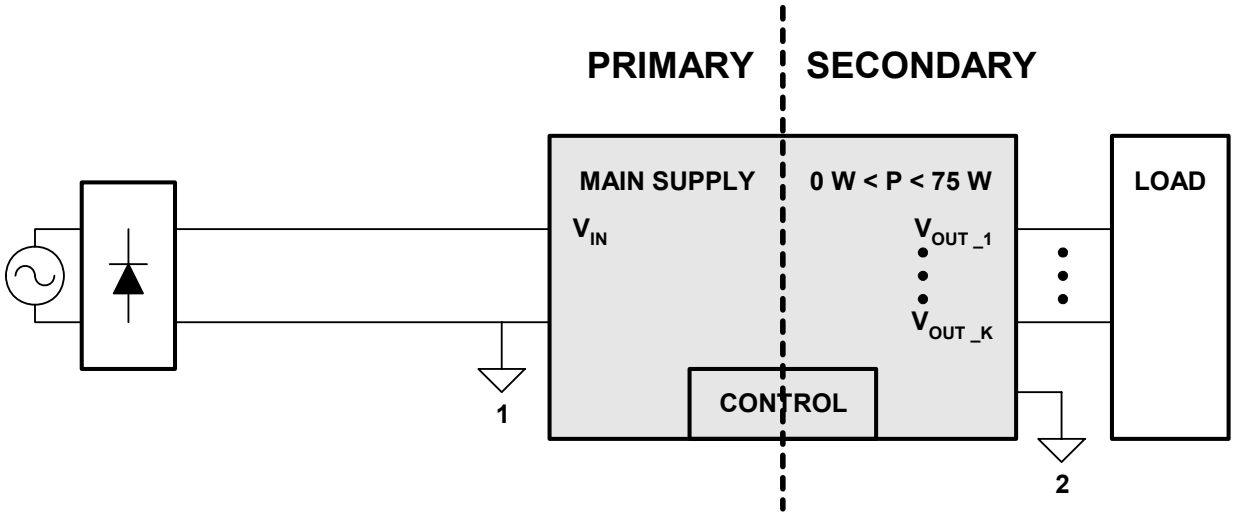

Fig. 3. Low-power system, the main supply has green mode.

Power system architecture for power levels that have more than 75 W capacity often include multiple power processors such as, a Power Factor Corrector (PFC), an isolated auxiliary supply, an isolated main converter, etc., as shown in Fig. 1. During idle periods, all of the supplies are turned-OFF except the isolated auxiliary supply that maintains the minimum amount of system functionality in order to properly revive the power system. There is a mid range of power supplies, shown in Fig. 2, that have large enough loads to require PFC, yet they do not merit the complications of the high-power systems. We can address the mid-range converters with the power system architecture that is shown in Fig. 2. Lower power level systems (below 75 W) can be implemented with single converter that can provide true regulation from 0 W to full load, such as Fig. 3. The isolated auxiliary supply in high-power systems and the single converter in low-power systems must both have a feature that enables them to maintain control at zero load power while drawing minimal power from the AC line. We call this feature "Green Mode".

One of the typical green-mode specifications is a maximum no-load power, usually below 500 mW. Unfortunately, it is difficult to predict the no-load power of a converter because of the myriad of interdependencies and non-linear switching losses. As of this writing, it is not possible to directly use a predefined no-load AC line power as a direct design parameter for power supplies; we must simply take the best measures that we can during the design process and be prepared to iterate the design.

The recurring element in the power systems of Fig.1 and Fig. 3 is a small (usually less than 75 W, perhaps as large as 150 W), wide input line converter. The flyback topology is a popular solution for this kind of application. It can be less expensive to add a low power green-mode converter to a high power system than to try to make a high power converter meet a small no-load AC load specification. If the controller includes a feature that detects when the converter is operating at extremely light loads and uses that information to turn-OFF a PFC and it offers quasi-resonant full-load control, the flyback topology can be extended to be sufficient for the 75 W-150 W range, in Fig. 2.

II. MULTI-MODE FLYBACK CONTROL

The flyback topology has a minimum number of components while providing galvanic isolation for the outputs. Input ripple current, output ripple current and leakage inductance energy usually limits the practical power range. The flyback converter is also popular in the role of an isolated auxiliary supply due to power level and the low cost of having multiple outputs. Keep in mind that a multiple output topology will have poor cross regulation during idle states due to the power-saving Discontinuous Conduction Mode (DCM) operation.

There are a variety of operational modes that are compatible with the flyback topology; fixed f_S Continuous Conduction Mode (CCM), fixed f_S Discontinuous Conduction Mode (DCM), Quasi-Resonant (QR) Mode, constant-on time Frequency Fold-back Mode (FFM) and hysteretic burst mode. Controllers that are suited to simultaneous wide-line and wide-load operation often employ at least three of the aforementioned modes, if not four of them, so that the converter can maintain high efficiency at any rated operating point.

A. QR and DCM Modes

During heavy load operation, the practical choices are CCM, DCM or QR modes. Reverse recovery losses from the output rectifier and stability issues often eliminate the CCM option. Operation in DCM is limited by turn-ON loss and high RMS currents in the primary side. The QR mode offers the lowest turn-ON loss because the switching event occurs at the valley of the resonance that occurs after the flyback transformer is de-energized, as illustrated in Fig. 4. In DCM operation, the turn-ON loss can be as large as $\frac{1}{2}C_D(V_1 + nV_2)^2$ Joules, depending on line and load conditions. In QR operation, the turn-ON loss is $\frac{1}{2}C_D(V_1 - nV_2)^2$ Joules for valley switching and 0 Joules for Zero Voltage Switching (ZVS).

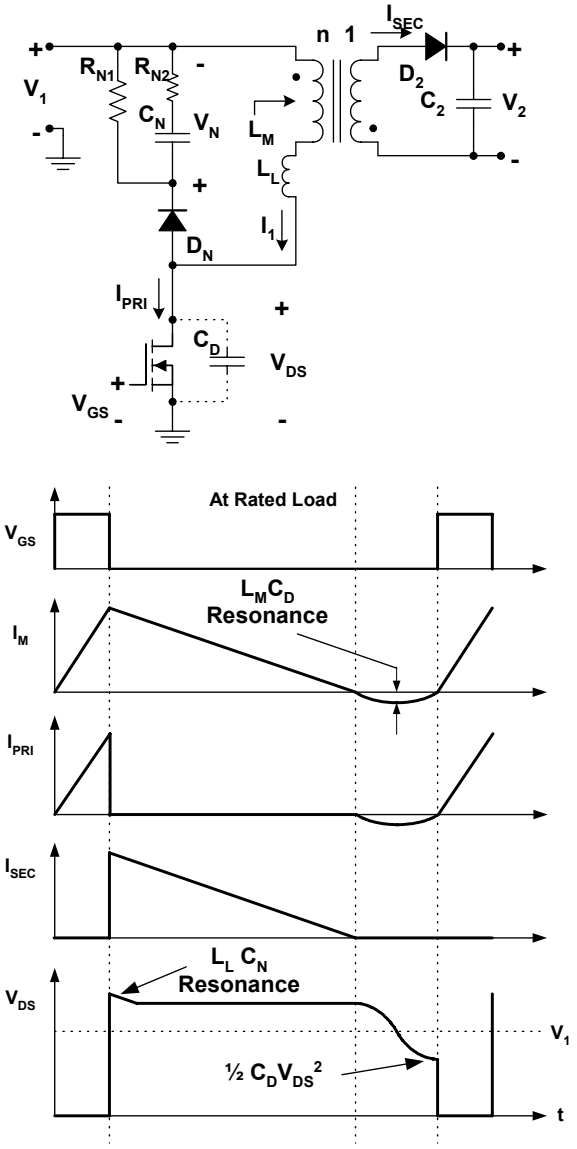

Fig. 4. Flyback converter (top), QR waveforms (bottom).

Why should we settle for valley switching; why not choose a transformer turns ratio that will always operate in the QR mode with ZVS? Unfortunately, the MOSFET stress voltage would be at least twice the input voltage at all line conditions. Operation at the maximum universal AC line voltage ($265V_{AC}$) translates to a peak operational stress voltage of at least 748 V_{DC}. As of this writing, MOSFET switching devices with sufficient voltage ratings and low $R_{DS(on)}$ are not economical.

Valley switching saves nearly 2 W of loss for a 65-W test converter with a 600-V MOSFET and a reflected secondary voltage of 100 V. Furthermore, the output rectifier commutates-OFF when it has zero current. Thus, the output rectifier does not incur reverse recovery losses. So, QR control with valley switching has merits over fixed frequency CCM and DCM designs. The price for saving the MOSFET turn-ON loss and the output rectifier reverse recovery loss is that the switching frequency must vary in order to maintain valley switching.

What happens to the switching frequency of the QR flyback converter when the input voltage changes or the load changes? In general, the switching frequency increases with increasing input voltage and with decreasing load, as shown in Fig. 5. Non-linear steady state behavior of the converter leads to complications in quantitatively determining the steady state peak current, I_P, and switching frequency, f_S.

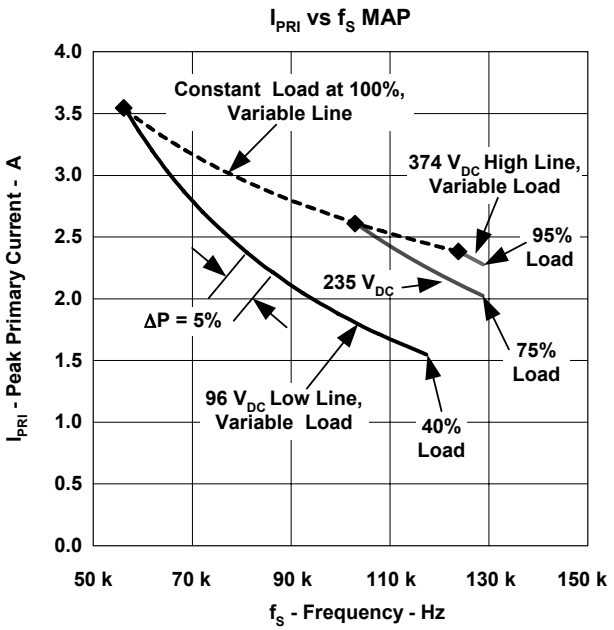

Fig 5. QR flyback operating plane.

The form of the steady state relationship for a QR flyback converter is a cubic equation, as shown in equation (3). In order to avoid the issues of root selection and ill conditioning, a bracketed search routine can be applied to equation (3) to solve for the peak primary current, I_P. Switching frequency is then solved using the DCM flyback input power relationship in equation (1). Due to the elaborate nature of the calculations, quantified solutions are best left to a spreadsheet. A bracketed search algorithm, such as the one in Reference [2] will find the correct root for I_P.

$$P_{IN} = \frac{1}{2} I_P^2 L_M f_S \tag{1}$$

Further steady state estimates of duty cycle can be made using the familiar relationships that are typically used for DCM flyback design, such as equation (2).

$$\frac{V_O}{V_{IN}} = D\sqrt{\frac{RT_S}{2L_M}} \tag{2}$$

$$0 = \frac{L_m + L_L}{2\,Pin} I_P{}^3 - \left(\frac{1}{V_1} + \frac{1}{nV_2}\right) L_m I_P{}^2 - \left(\pi\sqrt{L_m C_D} + \sqrt{L_L C_D}\right) I_P - \left(V_1 + nV_2\right) C_D \tag{3}$$

In practice, drain-source MOSFET capacitance varies with drain-source voltage. So, the effective C_D value must be calculated for each bulk capacitor voltage level using an average model that conserves charge. Furthermore, stray capacitances, such as TO-220 tab to ground capacitance (~25 pF) and reflected secondary capacitance, can be significant enough to require inclusion in the calculations. Sometimes, the resonance between C_D and L_M or L_L may require adjustment or stabilization due to system sensitivities. Additional capacitance can be connected between the drain and source nodes to trim the resonant frequencies. Additional capacitance should be kept small because frequency adjustment comes at the cost of efficiency.

The 100% load trajectory on the operating plane in Fig. 5 reveals that the circuit for limiting the maximum power must consider the line voltage. In fixed frequency designs, power is clamped on a cycle-by-cycle basis by a fixed threshold on the PWM comparator. In this case, low-line voltage must permit a larger $I_{P(max)}$ current than at high line voltages. This function can be achieved at a great expense of idle using a resistor connected to the bulk capacitor. An alternate technique that is more efficient uses the reflected line voltage signal, such as the UCC28600 implementation that is shown in Fig 6.

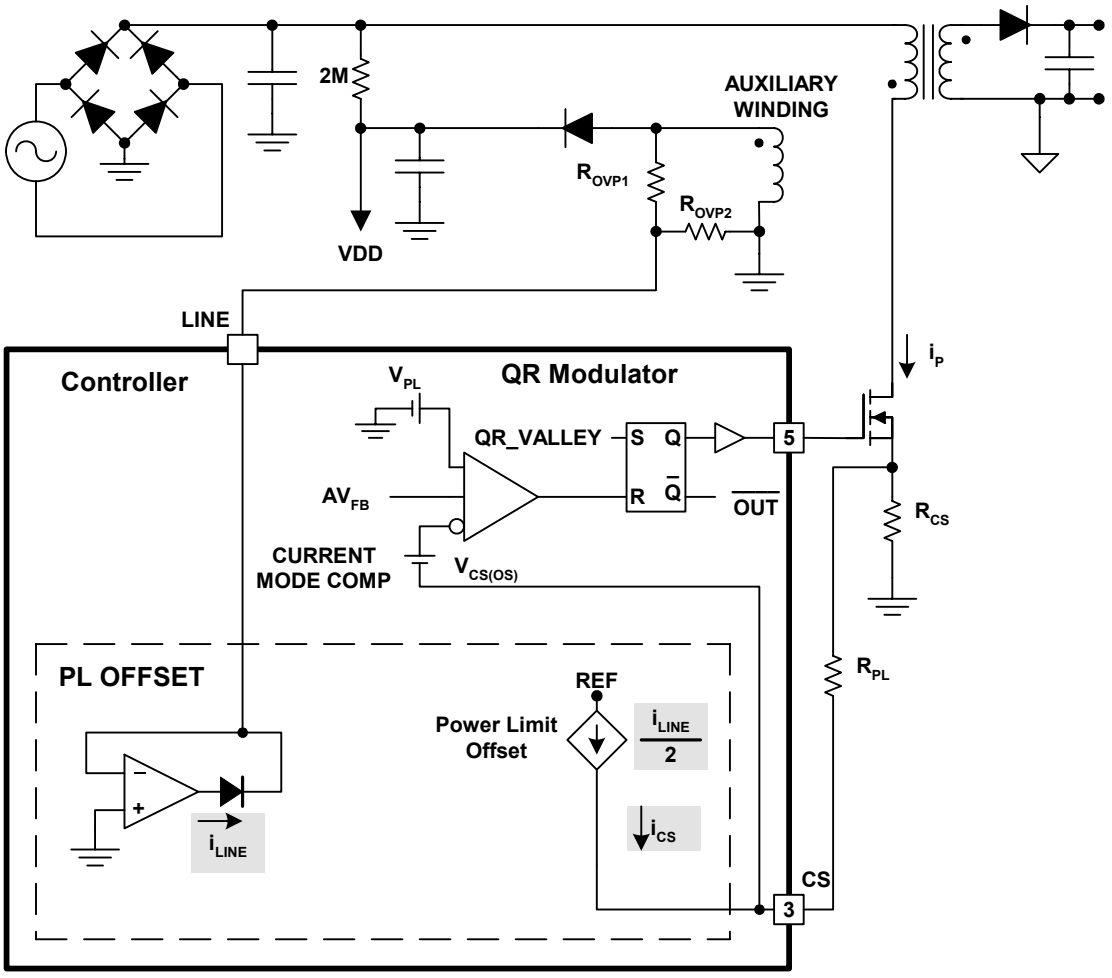

Fig. 6. Power limit circuit in UCC28600 controller.

Programming the power limit in Fig. 6 is achieved by using equation (4). The equation effectively offsets the 100% power trajectory in Fig. 5 so that it is approximately horizontal, as viewed by the CS pin. Notice that not only are the calculations of R_{CS} and R_{PL} dependent on one another, they are also dependent on the calculation of R_{OVP1} and R_{OVP2}. The offset also makes the MOSFET-ON duration narrower for other modes of operation. During burst operation, the pulse width is typically too narrow for good efficiency during ultra light loads. So, the power limit offset is sometimes turned-OFF during burst operation.

Quasi-resonant control causes the steady state switching frequency to increase with decreasing load. For example, the Low-line trajectory in Fig 5 shows the switching frequency spanning from 65 kHz at 100% load to nearly 120 kHz at 40% load. Intuition rightly tells us that beyond a point, the switching frequency in QR mode is going the wrong way for lighter loads! At an operating point where the MOSFET ON duration is large enough to make up for switching losses, the controller mode must change so that the switching frequency decreases in order to reduce switching losses.

B. Frequency Foldback Mode

Typically, a constant ON-time Frequency Fold-back Mode (FFM) is employed for moderate to light loading ranges. In the interest of keeping the line filter small to meet EMI agency limits, the upper frequency should be clamped to a set level that is below 150 kHz. Transformer size can be minimized by setting the full-load, maximum-line operating point near the upper-frequency clamp. Efficiency can be maintained if the upper-frequency clamp enables switching on the next V_{DS} valley after a minimum switch period. High efficiency during FFM can be maintained if the MOSFET turn-ON event is forced to occur at the V_{DS} resonance valley. Limit-cycling can occur between adjacent resonant valleys causing the average duty ratio to agree with equation (2).

$$\begin{bmatrix} R_{CS} \\ R_{PL} \end{bmatrix} = \begin{bmatrix} I_{P(min\_line)} I_{CS(min\_line)} \\ I_{P(max\_line)} I_{CS(max\_line)} \end{bmatrix}^{-1} \begin{bmatrix} \left(V_{PL} - V_{CS(os)}\right) \\ \left(V_{PL} - V_{CS(os)}\right) \end{bmatrix} \tag{4}$$

Without power limit correction to the CS voltage, the duration of the ON-time during FFM mode is actually a constant flux-variable-frequency control. However, power limit correction further reduces the ON-time as a function of line voltage. At high line, the peak transformer flux is lower than it is at low line. In the 65-W example that is used in this paper, the difference is a peak flux reduction of about 30% from low line to high line. The steady state trajectories can be illustrated as an operating plane, as shown in Fig. 7. In this design, the converter never operates at the upper clamp during low-line conditions; the converter goes directly between QR mode and FFM mode without ever reaching DCM. A green mode controller with an upper frequency clamp must allow for both transition sets: QR ↔ FFM and QR ↔ DCM ↔ FFM.

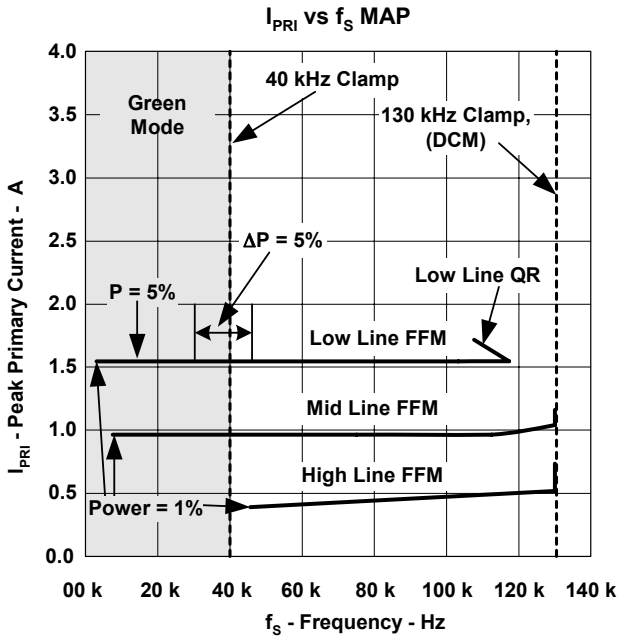

Fig. 7. Frequency fold-back mode operating plane.

An upper frequency clamp has several benefits. Without it, switching efficiency is reduced at higher frequencies due to MOSFET and diode characteristics along with a host of leakage inductances and stray capacitances. The core loss per unit energy transferred increases with switching frequency. The attenuation requirements and size of the input filter also increases due to the aforementioned agency specifications.[3]

If the power supply has multiple outputs, cross regulation deteriorates as the frequency folds back because of the reduction in the percentage of demagnetization time to the total switching period. Cross regulation reduction is particularly noticeable in the primary-side bias supply. During light-load conditions, the primary-bias voltage will be lower than during full-load conditions. That is why the primary bias voltage should be designed to be as high at full-load operation as the primary-side controller can comfortably allow. An RCD snubber clamp on the drain of the power MOSFET is effectively another output that is also impacted by cross regulation. During extremely light-load conditions, the RCD clamp capacitor can completely discharge between ON intervals of the power MOSFET.

C. Green Mode

At ultra-light loads where the average frequency would be in the audio range, many green-mode controllers offer a hysteretic mode of operation. Another advantage of green mode is that it minimizes how often the snubber clamp capacitor must be charged to the reflected output voltage in order to permit commutation on the main output. In contrast, FFM tends to cause higher average voltages to be maintained on the RCD snubber clamp as a result of maintaining regulation on the main output. Green-mode control permits the RCD snubber clamp voltage to completely discharge between bursts, which results in higher efficiency at ultra-light loads.

Green mode is implemented by employing a clamp for low switching frequencies and forcing the converter to operate in hysteretic mode. Some controllers have constant ON-time while in green mode; others modulate the gate pulse with a soft-start ramp in an effort to abate possible audio noise problems. A constant ON-time green mode is more efficient than a ramp modulated burst operation because the narrow pulses at the beginning of the ramp can be so short that they expend switching loss without being sufficiently long to transfer energy to the main output of the converter.

Under no-load conditions, the converter always carries load of the secondary controller bias, primary controller bias and opto-coupler, as shown in Fig. 8. In the best circumstances, these loads pose between 25 mW and 50 mW, depending on the line voltage. We must also add the loss in the start-up device, such as R_{SU} in Fig. 8, to the total no-load system loss. A typical value for the start-up resistor in a universal line application is 2 MΩ. At 110 V_{AC}, the start-up resistor, R_{SU} dissipates 11 mW; at 230 V_{AC} it dissipates 50 mW. Notice here that the start-up device can nearly equal, if not surpass the green-mode energy requirements for the primary and secondary control circuits. In spite of this, the no-load loss for the controls and the start-up device is still only 25 mW to 64 mW. Why does achieving less than 500 mW of AC line power at no-load pose such a significant challenge?

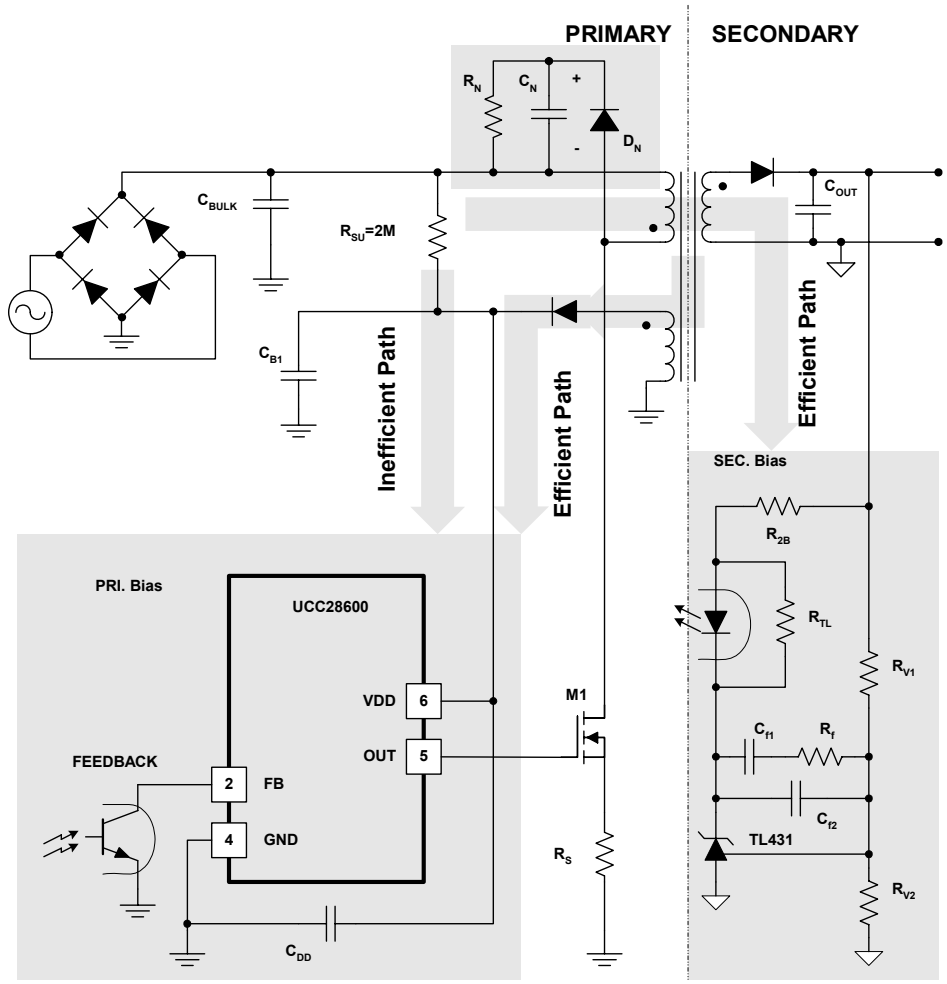

Fig. 8. No-load energy paths in an isolated converter.

Notice in Fig. 8 that the snubber is activated with each switch cycle. In the least, the snubber presents itself as a third output with a peak voltage that equals the reflected secondary output voltage. Although the most efficient path to transfer energy in the converter at full power is through the transformer, the snubber can severely reduce efficiency at no-load, as shown in Fig. 9. Zener diode based snubber clamps can help reduce no-load losses by eliminating the need to charge up the snubber on the first switch cycle of a burst, but it can be a challenge to match the tolerances with the application. Regardless of whether the snubber is an RCD clamp or a Zener clamp, it plays a major role in no-load AC power for flyback converters.

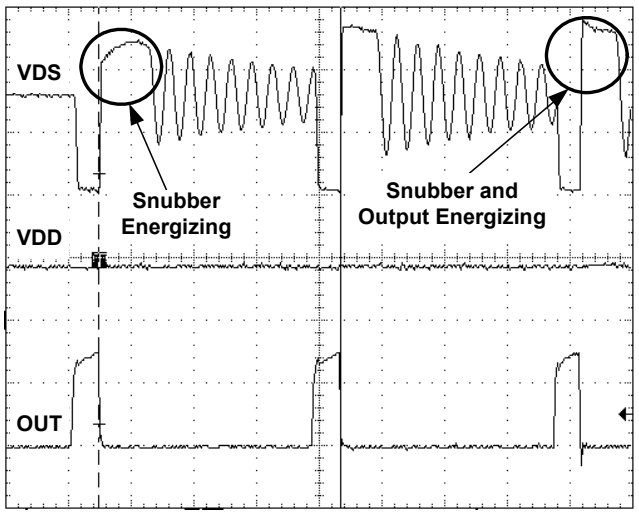

Fig. 9. Snubber taking all of first burst pulse energy.

In the example of Fig. 8, the total power for controlling the power supply is between 25 mW and 64 mW, depending on line voltage. This minimum level also assumes very high efficiency during green mode. In a practical converter, the no-load power is typically closer to 150 mW to 350 mW over the same line range. Is there anything that can be done to reduce the no-load power even further? The answer is yes, provided the system can afford to trade ripple and recovery time for lower no-load power.

No-load power can be significantly reduced if the burst period is longer than the primary bias hold-up time. In other words, this system intentionally lets the primary bias fall below the UVLO-OFF threshold, which in turn, causes a shutdown-retry event, as shown in Fig. 10. We will call this mode a UVLO controlled green mode. Between shut-down and retry, the converter cannot switch the power MOSFET, which dramatically reduces the snubber losses. The main output ripple is significantly increased. Also, if the load "happens" to turn-ON when the controller is between shut-down and retry states, the output voltage will not begin correction until the controller reaches UVLO-ON.

The delay for recovery in this case will be in the range of hundreds of milli-seconds in contrast to the hundreds of micro-second response time for a functional closed loop control. Applications where the load always starts-up lightly and has a known delay before changing to a full power state can work well with this requirement. For instance, a battery charger that always begins a charging cycle with a trickle charge interval could conveniently function with a power supply that is configured with a UVLO controlled green mode.

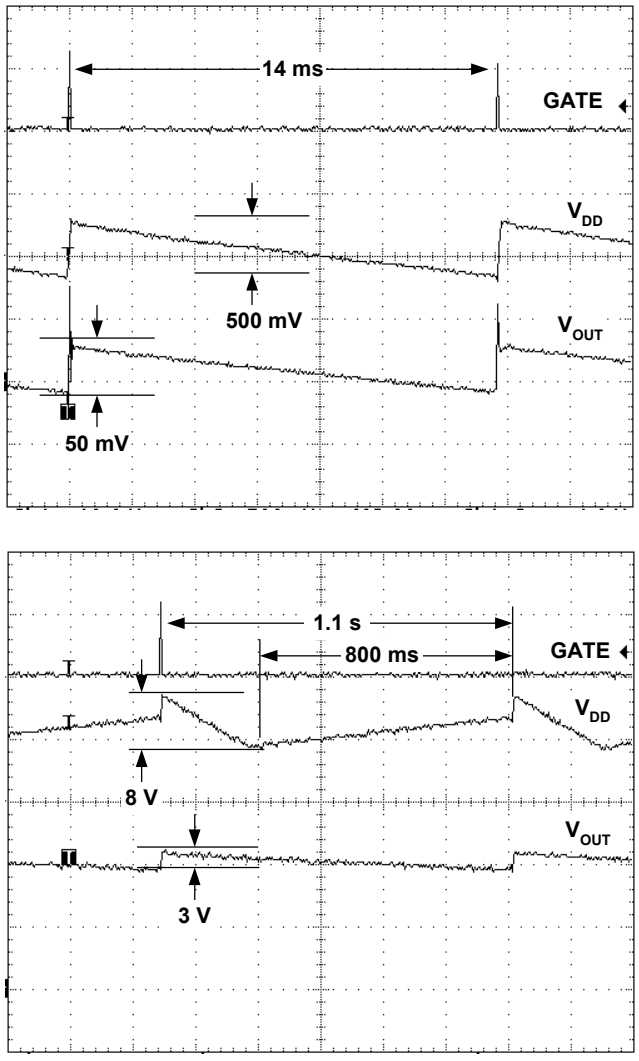

Fig. 10. Power supply outputs during (top) FB hysteresis burst, P_{AC} = 160 mW and (bottom) UVLO hysteresis burst, P_{AC} = 35 mW.

For some systems, the UVLO controlled green mode can be reached by through a soft-start event when the output has an initial voltage in a no-load condition. In no-load condition, the power supply can easily raise the output voltage; the power supply cannot reduce the output voltage. Normal operation will be regained when a small load is applied to the power supply output. In the past, the UVLO controlled green mode was sometimes avoided using a dummy load, which is not a suitable green-mode solution.

At this point, we can see that the requirement to have high efficiency at all loads, ranging from zero to full rated power brings a few new elements to the control function. Frequency foldback and green modes are required. If the power level is sufficiently large, QR mode is also desirable. We can now turn our attention to design techniques.

III. Designing a QR Resonant Flyback for Green-Mode

Variable operating frequency characteristics of a QR resonant flyback adds a few complications to the design process of the converter. A spreadsheet calculator, such as the one in reference [2], can help reduce hardware iterations. See sub section *A, QR-Flyback Design Iteration,* on the next page. Many of the specifications can be met without iteration. The design process begins as usual, with gathering the terminal specifications about the power supply (input voltage, range, output voltage, power out, efficiency). The designer must also have a power MOSFET that has sufficient current and voltage ratings, as if it were being used for a fixed frequency DCM converter with similar terminal specifications. Peculiar to QR design, the MOSFET drain-source capacitance is needed. Also, an estimate of the percentage of primary leakage inductance is necessary.

For a minimum-sized converter, a QR-flyback design will usually target the maximum load, maximum line condition as close to the upper frequency clamp as possible. The design should also use as much of the voltage stress that we can comfortably permit in order to maximize the duty ratio of the converter. The design is fully constrained by imposing the previous two elements plus the terminal requirements plus the MOSFET drain-source capacitance plus the percentage of leakage inductance. However, the problem is highly non-linear and the exact turn ratio can rarely be achieved. Yet, a design can be synthesized that is close enough to make minor changes.

A. QR-Flyback Design Iteration

1) Gather power supply terminal specifications
2) Estimate MOSFET
3) Transformer
   a) Estimate leakage
   b) Turn ratio for V_{DS} stress
   c) Inductance to fit high line to $f_{S(max)}$ clamp
   d) Bias turns for maximum VDD (~20 V)
4) Non-PFC design point for xfmr
5) PFC design point for xfmr
6) Select output capacitor and rectifier
7) Select R_{DD} to eliminate primary bias leakage overshoot at full load.
8) Controls: stability over QR through FFM range
9) Programming OVP, PL and OCP
   a) Program R_{OVP1}, R_{OVP2}, R_{CS}, R_{PL} as a set
      i) Program OVP (R_{OVP1}, R_{OVP2})
      ii) Program current sense and power limit (R_S, R_{PL})
   b) If the desired R_{CS} is not available, use Thevinin's equivalent

Conspicuously missing from the QR-Flyback Design Iteration is an estimate for the primary bias capacitor. Selection of the primary bias capacitor is much easier using data from the operational converter because estimation during the design process requires knowledge of the number of pulses in a burst group and the duration between bursts. The profile of the burst cycles depends on the loop gain, switching losses, snubber conduction and bias supply loads.

At the end of the first iteration, it is time to look for a transformer core. Detailed transformer design is beyond the scope of this paper. However, some of the unique design considerations for the QR flyback transformer will be presented here because of the significant impact on the transformer design process and optimization opportunities.

B. Transformer Considerations

The optimum transformer design will be different with non-PFC and boost follower applications than with regulated PFC stage applications. Applications with a regulated PFC stage can use a smaller flyback transformer if the design includes over-temperature protection in the event of a PFC fault.

At this point, the current swing is known, the primary and secondary RMS currents can be solved for a given line condition. Either the area product method or the K_g method can be used for core selection.[5][6] Obviously, the transformer must be selected for maximum load. What line condition should be used to determine the core size? For a moment, compare the case where input voltage to the QR flyback converter is at the lower extreme with the case where the input voltage to the QR flyback converter is at the upper extreme. For a given transformer design, the copper loss is elevated at low line over the high-line condition because of the larger low-line RMS winding current. In contrast, core loss variations over line voltage are not as obvious. At low line, the switching frequency is lower and the flux swing is higher than at high-line voltage.

In general, core loss is described by:

$$P_{Fe} = K_{feo}\ f_S^{\kappa}\ \Delta B^{\beta}\ A_C\ l_M \tag{4}$$

where,

- K_{feo}, κ and β are core constants
- f_S is the switching frequency
- ΔB is the flux density swing
- A_C is the area of the core
- l_M is the mean magnetic length

If equation (4) is reformulated for the specific case of the flyback transformer, the loss equation is in terms of the primary current swing:

$$P_{Fe} = K_{feo}\ f_S^{\kappa}\ L_M\ \Delta I^{\beta}\ A_C^{(1-\beta)}\ l_M \tag{5}$$

where,

- L_M is the magnetizing inductance
- ΔI is the primary current ripple (1/2 times the peak-to-peak value)

If the winding allocations are optimized using the Lagrange multiplier technique[7], and considering a single-output transformer, we can express the copper loss as:

$$P_{Cu} = \frac{\rho\,(MLT)\,n_1^2\ I_{tot}^2}{W_A\ K_u} \tag{6}$$

where,

- ρ is the resistivity of copper,
- MLT is the mean length per turn
- N_1 is the number of primary turns
- W_A is the window area
- K_u is the winding fill factor
- I_{tot} is the total rms winding currents, referred to the primary

For the single output case, the square of I_{tot} can be described by:

$$I_{tot}^2 = \left(I_1 + \frac{N_2}{N_1} I_2\right)^2 \tag{7}$$

Equations (5) and (6) can be expressed in a form where they are normalized to their mean value in an operating range in order to show their relative variation over the full operating range of a specific flyback converter. The normalized equations are given by:

$$P_{Fe,norm} = \frac{f_{S,i}^{\kappa}\ \Delta I_i^{\beta}}{\left\langle f_S^{\kappa}\ \Delta I^{\beta}\right\rangle_{op.\,range}} \tag{8}$$

$$P_{Cu} = \frac{I_{tot,i}^2}{\left\langle I_{tot}^2\right\rangle_{op.range}} \tag{9}$$

To get an idea of the variation in core loss compared to the variation in copper loss, we will consider a specific core material for a specific power supply over the full range of universal input voltage. The converter is a 65-W universal AC in to 19.4 V_{OUT} single-output converter. The peak currents and switching frequencies are calculated over the range of operation. The core material that is used is 3C90, which is typical for converters with switching frequencies in the 130 kHz range. A normalized form of P_{Fe} and P_{Cu} can be plotted, as shown in Fig. 11, to compare the change in loss over the operating range of the converter.

The relevant core constants for 3C90 are:

- $\kappa = 1.40$
- $\beta = 2.74$

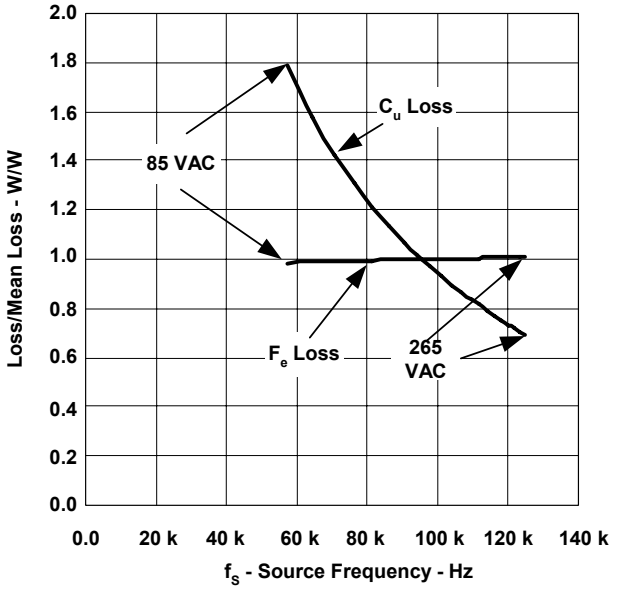

Fig. 11. Normalized core and copper losses at full load over the range of line voltage.

Fig. 11 indicates that the core loss hardly varies +2%, -1% over the full range of operation while the copper loss varies +80%, -30% over the same range. In other words, the core loss remains nearly constant because any reduction in flux swing is nearly offset by switching frequency. The results here may change incrementally with core material or power supply line range because the core material constants do not vary enough to significantly change the slope of the normalized power.

For a universal AC line, non-PFC application or a boost follower PFC application[4], the core and number of turns should be selected for the minimum input voltage. Make sure that strands in the windings are compatible with the high-line, full-load conditions that include increased frequency with reduced RMS primary current, particularly with the secondary winding. Skin effect losses in the primary winding tend to be offset with reduced RMS primary current.

For a universal AC line power system with a PFC, the QR-flyback stage will always operate at steady-state with heavy load at the regulated output voltage of the PFC stage. In this case, the QR flyback transformer can be optimized for steady-state, high-line operation. But beware, if the core is optimized for steady-state operation at the average PFC output voltage, be sure to include an over temperature shutdown circuit in the event that the PFC stage fails in the OFF state. In addition, the core must not saturate at the low line condition. Generally, the QR mode will impose a core loss limit on the transformer design rather than a saturation limitation.

C. Control Considerations

In the power supply industry, the standard crossover frequency limit of the control loop is 1/5 of the switching frequency. The switching frequency of green mode converters varies, yet the compensator is static. Select a crossover frequency that is compatible with the lowest switching frequency. For controllers that have a green mode, such as the UCC28600, the crossover frequency must be at least 1/5 of the frequency of pulses within a burst packet (40 kHz for the UCC28600). During green mode, the converter operates in a bang-bang mode that is bounded-output stable. The highest gain condition occurs during high line with the lightest load that allows the converter to operate at the maximum switching frequency clamp. The power supply designer can count on the crossover frequency to vary more than 3:1 for a universal AC supply.

Crossover frequency can affect the no-load power because of its impact on the number of pulses in a burst packet. The faster the control loop response, the lower the number of pulses in a burst packet. Fig. 12 and Fig. 13 shows that the number of pulses in a burst packet can nearly double for a 1.75 times increase in crossover frequency. However, the number of pulses for either case does not significantly change for voltage variations.

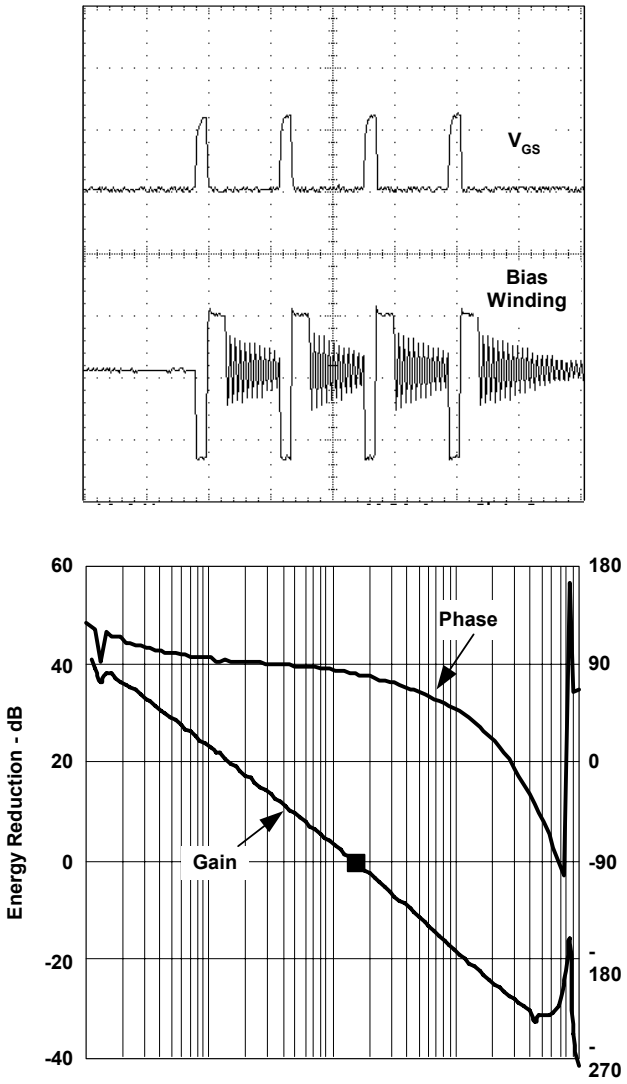

Fig. 12. Burst pulses and loop gain for high-loop gain controller; f_{CO} is 1.5 kHz at 36 W and 110 V_{AC}.

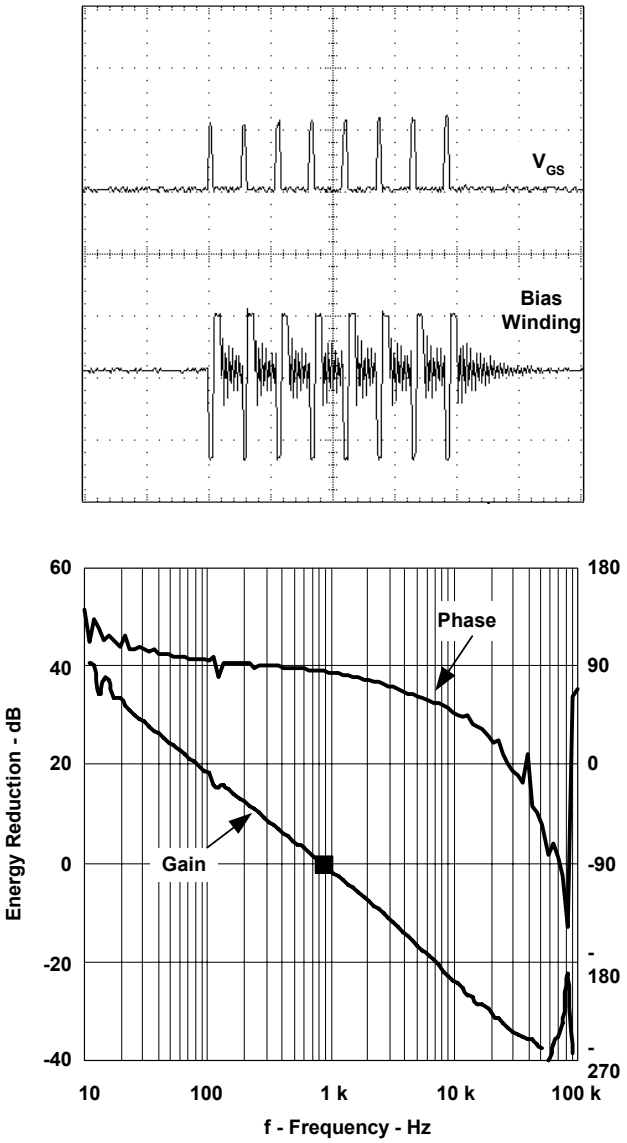

Fig. 13. Burst pulses and loop gain for low-loop gain controller; f_{CO} is 850 Hz at 36 W and 110 V_{AC}.

IV. EXPERIMENTAL DATA

High efficiency over wide load ranges is demonstrated in this section, along with several key waveforms. Prior to demonstrating the performance of a green-mode controller, a technique for measuring no-load power must be discussed. It turns out that low power levels and burst mode poses a measurement challenge, particularly when the wattmeter is designed to measure hundreds of watts.

A. Power Measurement Techniques

Power measurements refer to real power, not apparent power. In order to make a power measurement, especially where the PFC stage might be turned-OFF, the wattmeter must read the average of the product of the line current times the line voltage. Simply reading RMS line voltage and RMS line current and multiplying the result will yield a wrong answer that is too large. However, average output voltage times average output current gives adequately accurate results due to the DC nature of the output voltage.

When measuring the efficiency, use calibrated meters rather than power supply indicator readings. Measurements of high efficiencies are extremely sensitive to meter accuracy. Often, the voltage and current meters are digital in nature; be sure that there is adequate resolution for the measurement.

Average efficiency measurement and calculation is often controlled by an agency or organization specification. For example, Energy Star® requires the efficiency of a single output external AC-DC power supply to be the average of the efficiencies that are measured at 100%, 75%, 50% and 25% of the nameplate rated output current at a thermal steady state.[8][9]

No-load power measurement requires extra care due to its extraordinarily low level and the issue that the burst frequency can occur at much lower frequencies than the AC line frequency. The wattmeter must resolve small currents and be capable of averaging the instantaneous power measurement over many line cycles.

It is best to use a resistive shunt to measure the AC line current because the burst harmonic can be much lower than the frequency response of an AC current probe and thus, compromise the measurement. The burst frequency can be too low for a clip-on magnetic current sensor. For this reason, agencies often require the AC shunt to be resistive[10], as shown in Fig. 14. The resistance of the AC shunt will probably need to be larger than the shunt that is used at full power. It is not unusual to require a 10-Ω shunt in order to measure the no-load power to the fullest ability of the wattmeter. Remember to change the shunt to a much lower value before making measurements at larger loads.

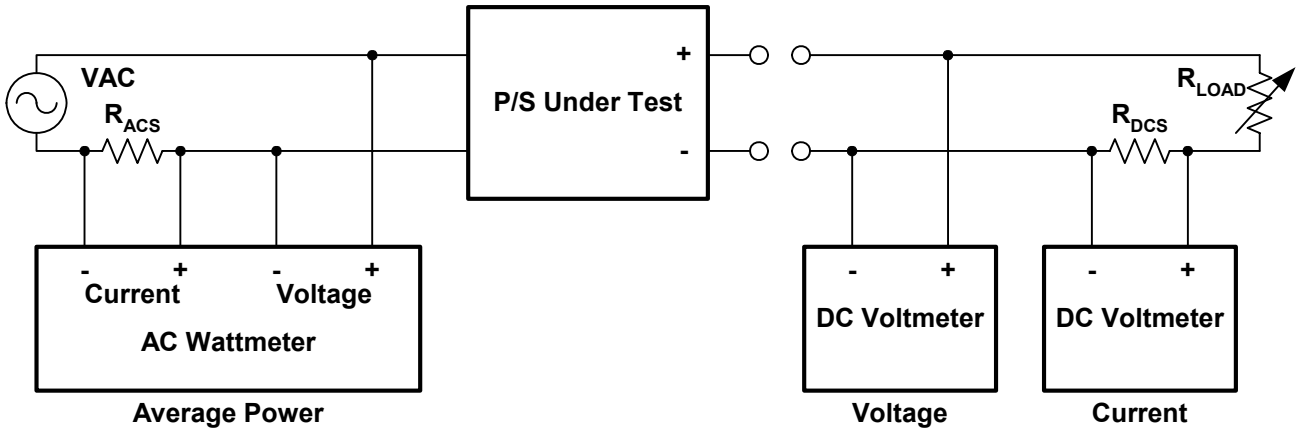

Fig. 14. Power measurement circuit. R_{ACS} may need to be much larger for no-load power measurement than other power levels.

Another important factor for accurately measuring the no-load power is the averaging interval.[11] The burst frequency can be lower than the line frequency and the averaging interval must be long enough so that an extra cycle per sample will cause a significant deviation in the result. The IEC recommends that the averaging interval is at least 5 minutes or long enough to sample an average of 200 bursts.

B. Experimental Performance

The test converter that we will examine is a 65 W, 85-V_{AC} to 265-V_{AC} input to 19.4-V_{DC} output power supply. The schematic is shown in Fig. 15, and the components are listed in Table I. This power supply is typical of laptop computer AC adapters. The experimental waveforms in the previous figures are actual data from this converter.

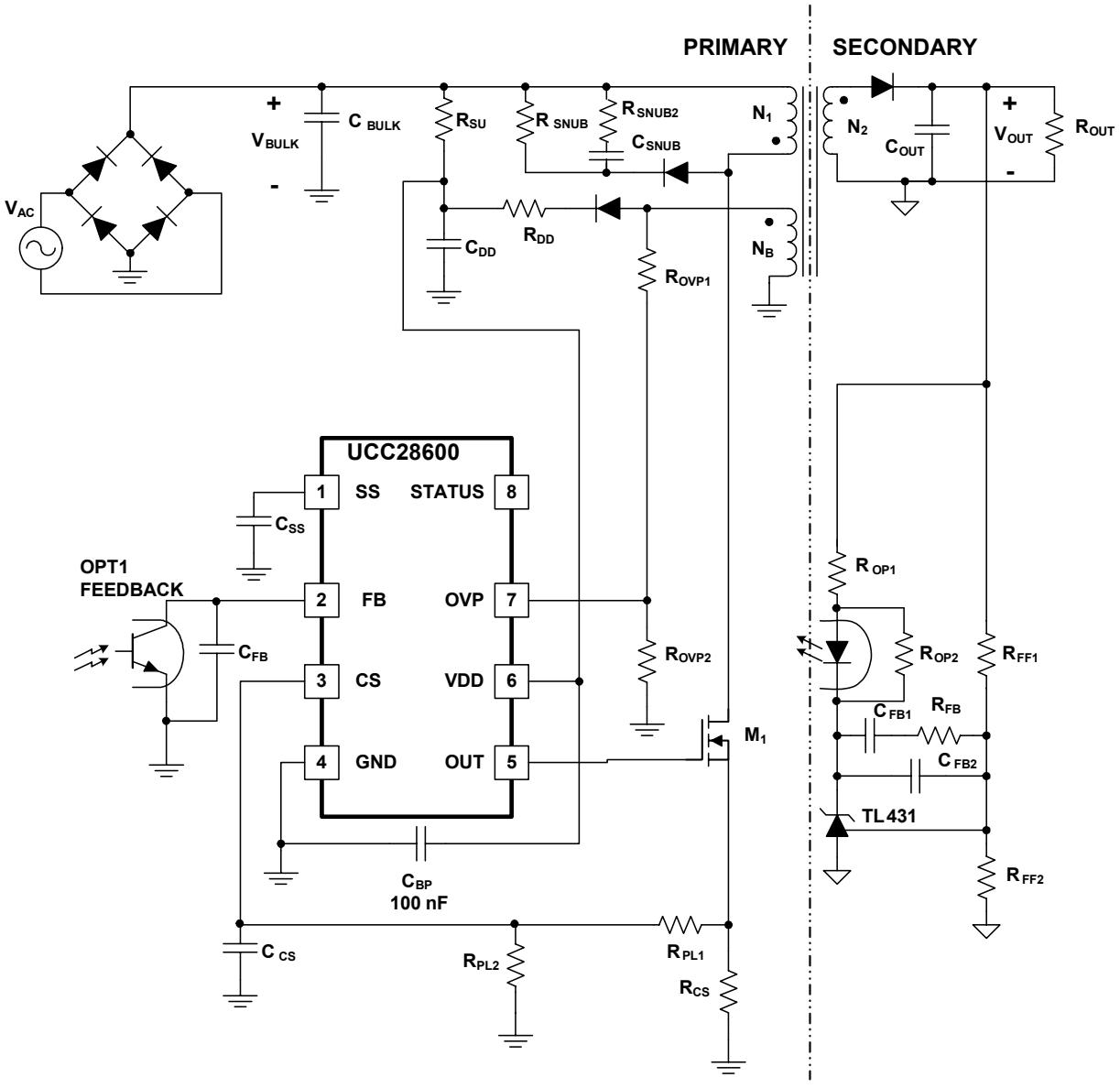

Fig. 15. Schematic of 65-W, 85-V_{AC} to 265-V_{AC} to 19.4 V_{DC} test converter.

TABLE I. COMPONENTS FOR FIG. 15.

Reference Designator	Description
C_{BP}	100 nF
C_{BULK}	330 µF, 450 V
C_{CS}	180 pF
C_{DD}	10 µF
C_{FB}	390 pF
C_{FB1}	330 nF
C_{FB2}	470 pF
C_{OUT}	2000 µF
C_{SNUB}	10 nF, 200 V
C_{SS}	10 nF
M_1	11N60C3
OPT1	CNY17-1
R_{CS}	0.25 Ω, 1 W
R_{DD}	33 Ω
R_{FB}	100 kΩ
R_{FF1}	20.2 kΩ
R_{FF2}	3.01 kΩ
R_{OP1}	2.00 kΩ
R_{OP2}	750 Ω
R_{OVP1}	169 kΩ
R_{OVP2}	29.4 kΩ
R_{PL1}	2.21 kΩ
R_{PL2}	61.9 kΩ
R_{SNUB1}	10 kΩ, 5 W
R_{SNUB2}	33 Ω, 1 W
R_{SU}	1.0 MΩ
R_Z	2.49 kΩ
T1	32:6:6, 294 µH, PQ2625
U1	UCC28600

A useful tool for judging the general performance of a power source is a plot of output voltage versus output current, or the I-V curves, as shown in Fig. 16. This plot indicates the effective steady state output impedance of a power supply as a result of the load. Ideally, it should have a constant voltage section for low current levels and it should exhibit some sort of power limiting. It should also have a foldback point which prevents the converter from attempting to deliver excessive output current. The power limit portion of the curves followed the programmed power limit for output voltages between 19 V and 16 V. Heavier loads were further limited due to loop saturation that was caused by interactions between the internal 5 V reference of the UCC28600 and magnetizing inductance. The additional power limiting at high current is generally a welcomed feature. Foldback occurs when the output voltage reaches about 7.5 V, which is due to the bias voltage, VDD, of the UCC28600 falling below UVLO-OFF.

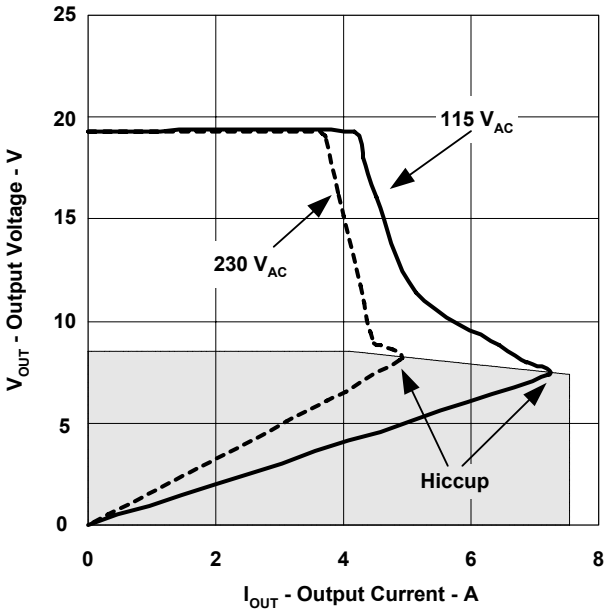

Fig. 16. I-V curves of 65-W test converter.

The overall efficiency of the converter is fairly constant from 10% to 100% full rated load, as shown in Fig. 17. The data in the figure includes measurements for power output from 0.96 W to 65 W. Inflections in the curves occur near the mode boundaries. Notice that the inflections are simpler for the 115 V_{AC} case than the 230 V_{AC} case.

In the 230 V_{AC} case, the converter transitions between the modes: green mode ⇔ FFM ⇔ fixed f_S DCM ⇔ QR. Evidence of the transition between DCM and FFM (15 W) and the transition between FFM and green mode (BW) is given by the inflections in the 230 V_{AC} efficiency curve.

In the 115 V_{AC} case, the converter only transitions between the modes: green mode ⇔ FFM ⇔ QR. At the line voltage, this converter does not reach the upper f_S clamp, eliminating the fixed f_S DCM mode. Evidence of this is seen in a simpler curve at 115 V_{AC} with inflection only at the transition between FFM and green mode.

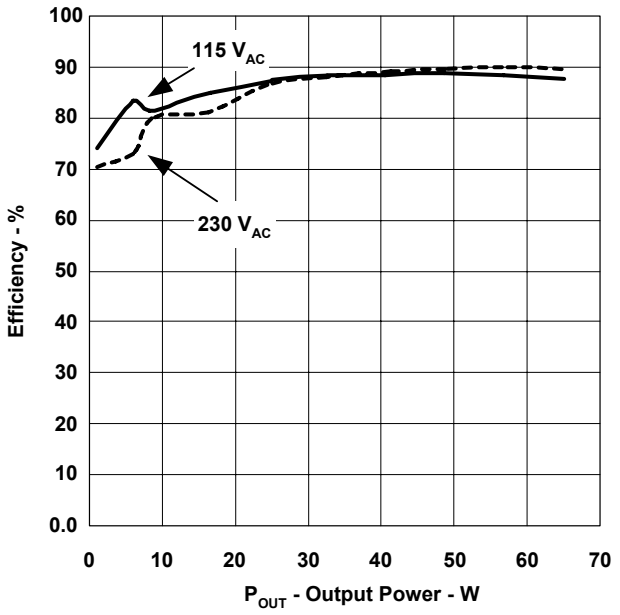

Fig. 17. Efficiency curves of 65-W test converter.

The average power, measured and calculated per Energy Star® specifications (average at 100%, 75%, 50% and 25% rated load) is 87% at both 115VAC and 230VAC. All four efficiency measurements in the average calculation are above 80% for both line conditions.

Standby power assumes a no-load condition and it is measured per IEC62301 using a Voltech wattmeter in the configuration that was shown in Fig. 14. The shunt resistor is 5 Ω; at each measurement, there is a five minute stabilization period followed by a power averaging time of five minutes. The results are shown in Table II. Usually, the no-load power criterion relies on nominal line voltages (115 V_{AC} or 230 V_{AC}) rather than the extremes (85 V_{AC} or 265 V_{AC}).

TABLE II. NO-LOAD POWER

VAC, V_{RMS}	P(AC line), W	Output Voltage Ripple, V_{p-p}
85	0.1573	0.0492
115	0.1421	0.0520
230	0.2216	0.0464
265	0.2732	0.0488

V. CONCLUSIONS

In order to meet efficiency requirements without exceeding the no-load power limitation, we must consider a power architecture that includes a specialized converter with good no-load performance in addition to efficient full-load performance. The QR-flyback converter has been demonstrated here as a strong choice for this application.

Quasi-resonant, frequency foldback and burst modes are necessary features that expand the high efficiency range of the flyback converter. Variable frequency and multiple modes add complexity to the design process yet, they impose insignificant change to the complexity of the converter. Furthermore, design tools are available that simplify the design process. Other benefits beyond efficiency and load range extension arise from using quasi-resonant control. If a regulated boost PFC stage is present, the QR-flyback transformer will be significantly smaller than a DCM flyback transformer.

Unfortunately, the no-load power cannot be predicted until the simulation or testing phases of the design process. Although no-load power depends on predictable elements, such as bias loads and control loop performance, it also depends on switching loss and snubbers. There are also two types of bias operation to consider during no-load power; hysteretic burst and UVLO controlled burst. Here, the trade is fast recovery speed (hysteretic burst) with low idle power (UVLO controlled burst).

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