Topic 3

Feedback in the Fast Lane – Modeling Current-Mode Control in High-Frequency Converters

Texas Instruments

Feedback in the Fast Lane
Modeling Extending Current-Mode Control in High-Frequency Converters

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ABSTRACT

Conventional small-signal analysis of current-mode control, combined with classical loop measurement techniques, has guided power supply designers for nearly thirty years. As switching frequencies increase to the megahertz range, timing delays introduced by circuit components begin to affect overall loop response creating discrepancies between measured and predicted results. Using the example of a buck converter, this paper re-examines a small-signal current-mode control model from a circuit analysis perspective, discusses circuit parameter effects on loop performance and in particular, investigates the effect on the open loop gain of the modulator.

I. INTRODUCTION

State-space averaging eliminates switching elements by averaging the contributions of each circuit topology they create. This technique enables analysis of switching power supply feedback loops by the use of relatively simple small-signal analysis techniques. Previous discussions of averaged modeling,[1][2] provide guidance in applying the technique. For example, the output filter must contain a double pole far below the converter switching frequency to ensure the validity of the model. A linear equivalent to the pulse width modulator (PWM) then replaces the pulse generating circuit, allowing analysis of the system in the frequency domain. By necessity, design, or because the effects were negligible at low operating frequencies, earlier modeling efforts simplified analysis by ignoring influences such as circuit propagation delay and complex pole-zero output filters. These factors become increasingly significant as switching frequencies and closed loop bandwidths increase. The following discussion revisits the averaged model from a circuit analysis perspective and investigates the effects physical circuit characteristics impart on feedback loop performance.

The approach followed is to model a simple DC/DC converter with voltage-mode control (VMC) operating in continuous conduction mode, and then increases the complexity of the model on a systematic basis each time pausing to review the change to the previous system. The addition of current feedback produces in an updated model for a current-mode control (CMC) DC/DC converter extendable to any buck-derived topology. The TPS40180 DC/DC buck controller incorporating both voltage-mode and current-mode modulation elements serves as the vehicle for an illustrative example. (See Appendix A). Predicted results from the completed model favorably compare with lab measurements for a converter operating at 1 MHz.

II. DEVELOPMENT OF THE NEW MODEL

A. *Review of a Simple System*

Fig. 1 illustrates a voltage-mode synchronous buck converter and the equivalent small-signal block diagram. In this block diagram, the error amplifier and compensation components form blocks K_{EA} and K_{FB}. The pulse width modulator, drivers, and MOSFET switches become an averaged circuit block, K_{PWM}. The output filter and the load combine to form filter block X_{LC}.

The closed loop response of the system equals, (See Appendix B):

$$Tv(s) = V_{IN} \times K_{FB} \times K_{EA}(s) \times K_{PWM} \times X_{LC}(s) \quad (1)$$

Once the output filter and modulator satisfy the converter design requirements, the feedback network, $K_{FB}K_{EA,}$ must ensure the closed loop response meets stability requirements. Other authors provide full details of techniques[3][4] for synthesizing feedback networks to stabilize a system. This paper focuses on the effect of high frequency operation upon the modulator and filter blocks, or more specifically, the control-to-output transfer function V_{OUT}/V_C.

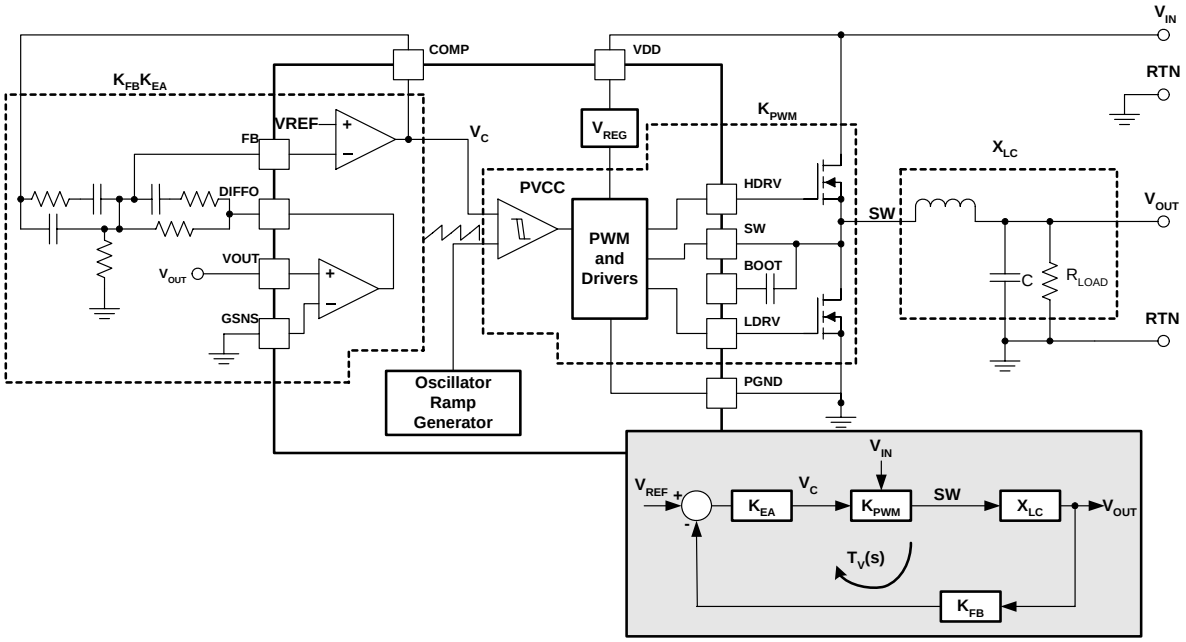

Fig. 1. VMC buck converter schematic and block diagram.

B. Modulator Gain

Fig. 2 illustrates a typical VMC PWM comparator with the associated waveforms. An oscillator derived saw tooth waveform compared to a control signal generates a pulse-width-modulated signal. Of keen interest is the transfer function of the control voltage (V_C) to the switching node (*SW*).

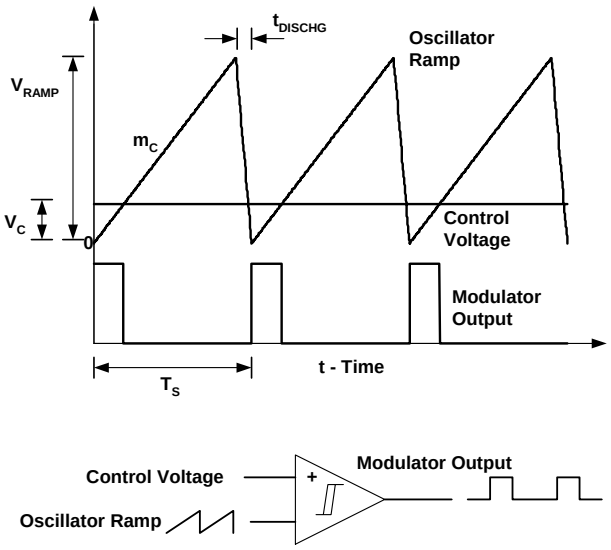

Fig. 2. VMC modulation.

An averaged model linearizes the PWM block, negating all switching effects, leaving only a simple linear relationship:

$$V_{OUT} = V_{IN} \times D \tag{2}$$

In the ideal case, and assuming continuous conduction mode operation, the output voltage is equal to the product of the input voltage and the duty cycle (*D*). A change in the duty cycle translates to an equivalent change in the *average* voltage at the SW node, and ultimately, to a similar change in the output voltage. Simplistically, a change in the control voltage (V_C) translates to a change in the duty cycle. The averaged model requires knowledge of this relationship between duty cycle and control voltage. Given that the duty cycle equals the control voltage divided by the peak-to-peak voltage of the ramp ($V_{RAMPp\text{-}p}$) the control to duty cycle gain (K_{PWM}) equals

$$K_{PWM} = \frac{\Delta D}{\Delta V_C} = \frac{\Delta D}{\Delta D \times V_{RAMPp-p}} = \frac{1}{m_C \times Ts} \tag{3}$$

In the last term of equation (3), the product of the *slope* of the modulator ramp and a *time interval* replaces the *amplitude* of the modulator ramp. The relevant time interval is the switching period less a ramp discharge time. The benefits of this substitution become evident in Section III, where current feedback and circuit parameter effects modify the PWM gain. For the example controller,

$$K_{PWM} = \frac{1}{\frac{0.5V}{1\mu s - 0.1\mu s} \times (1\mu s)} = 1.8 \times \frac{1}{V} \tag{4}$$

C. Output Filter

Many models assume ideal components when determining the L-C corner frequency. In practice, the output filter comprises a much more complicated circuit. The inductor has winding resistance, and there may be different of types of capacitors used, each with ESR and ESL characteristics that place a complex array of poles and zeros in frequencies of interest. A realistic output filter model as in Fig. 3 includes each component with its relevant parasitic elements.

In this model, the effective resistances of the switch and synchronous rectifier MOSFET are included into the filter block to account for variances in equivalent source loss due to duty cycle.

$$Z_{IN} = R_{DS(on\_sw)} \times D + R_{DS(on\_sr)} \times (1 - D) \qquad (5)$$

A simple voltage divider then creates the output filter transfer function:

$$X_{LC}(s) = \frac{Z_{OUT}(s)}{Z_{OUT}(s) + Z_L(s) + Z_{IN}} \qquad (6)$$

Where $Z_{OUT}(s)$, Z_{IN}, $Z_L(s)$ are the series and parallel combined impedances of the components within the dashed boxes in Fig. 3. Fig. 3 plots the filter transfer function for an ideal case in which all parasitic influences of ESR, ESL, and $R_{DS(on)}$ are set to zero, and for a more practical case where parasitic elements are included.

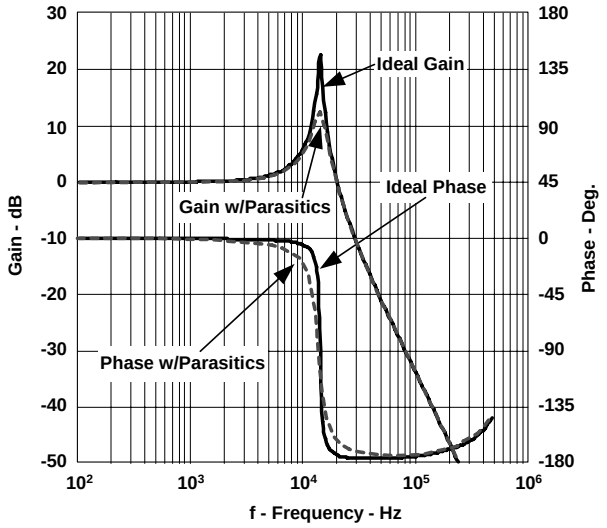

Fig. 3. Transfer function of the filter in Fig. 3.

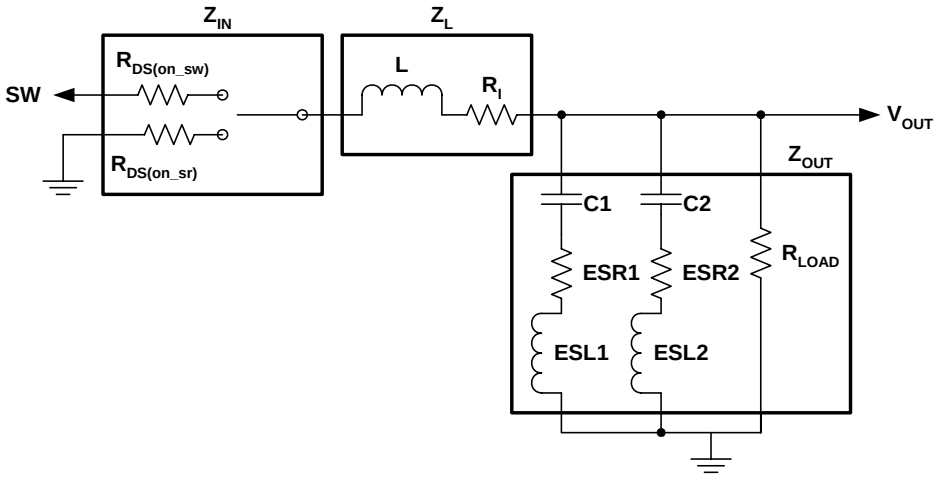

Fig. 4. Output filter schematic including parasitic elements.

The MOSFET resistance in series with the output inductor contributes an additional loss term that dampens the Q of the filter and attenuates the output voltage. The additional damping may affect the overall phase margin, depending on the selection of the final loop crossover frequency and the magnitude of the losses. This gain loss corresponds to a control correction required to maintain DC regulation. The degree of this correction becomes clear from a more realistic approximation of the duty cycle:

$$D = \frac{V_{OUT} + I_{OUT} \times (R_{DS(on\_sr)} + Rl)}{V_{IN} - I_{OUT} \times (R_{DS(on\_sw)} - R_{DS(on\_sr)})} \qquad (7)$$

For the example, evaluation of equation (7) estimates the amount of change in duty cycle in a change from no load to full load. Under no load condition, the duty cycle will be 3.3/12 = 27.5%, and under fully loaded conditions:

$$D_{FULL\_LOAD} = \frac{3.3 + 5 \times (5.5m + 2.2m)}{12 - 5 \times (5.5m - 4.5m)} = 27.9\% \qquad (8)$$

The difference between these two represents a 0.4% increase in duty cycle due to filter and MOSFET conduction losses. This calculation gives a good first-order approximation of the difference in duty cycle, and thus the gain loss. One should consider this effect when compensating a converter over a wide range of loads.

D. Control to Output

The filter and PWM blocks together create the control-to-output transfer function. With this, and the desired response of the overall loop, a designer can synthesize a suitable error amplifier compensation network. Fig. 5 shows the control-to-output frequency responses for the example converter using voltage-mode control at input voltages of 5 V and 12 V. Note that the gain $X_{CO}(s)$ depends linearly upon the input voltage V_{IN}:

$$X_{CO}(s) = \frac{V_{OUT}(s)}{V_C(s)} = V_{IN} \times K_{PWM} \times X_{LC}(s) \qquad (9)$$

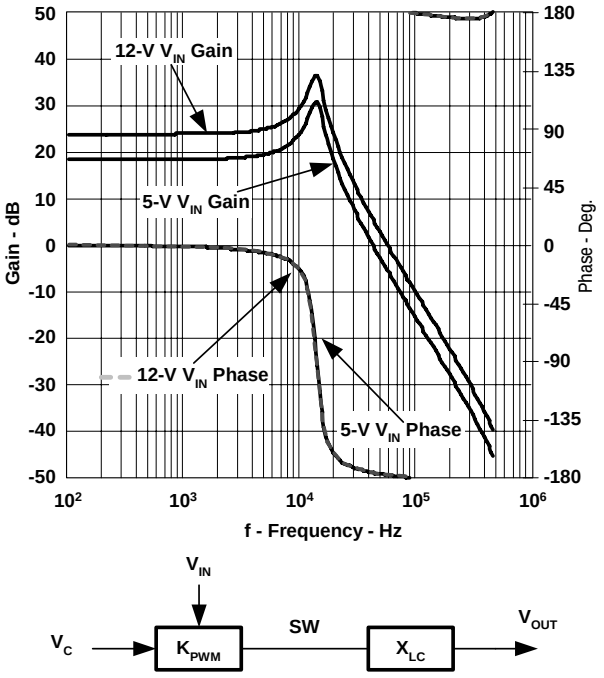

Fig. 5. Control-to-output transfer function.

III. PEAK CURRENT FEEDBACK

The previous section examined the control-to-output transfer function for voltage-mode control. The next step increases the complexity of the system by adding current feedback.

Fig. 6 depicts the schematic and block diagram of a buck controller containing an inner current feedback loop. The schematic illustrates one of several peak-current feedback topologies. Other topologies, including peak MOSFET current sensing uses the same analysis. Current feedback adds three new blocks to the diagram: current sense, $X_i(s)$, current gain, $K_{CS}(s)$, and sampling gain $H_e(s)$[5]. The current-sense transfer function and the current-sense gain both have counterparts in a physical design. The sampling gain, which has no such physical counterpart, allows the application of a discrete-time function (in this case, current sampling) to a continuous-time analysis.

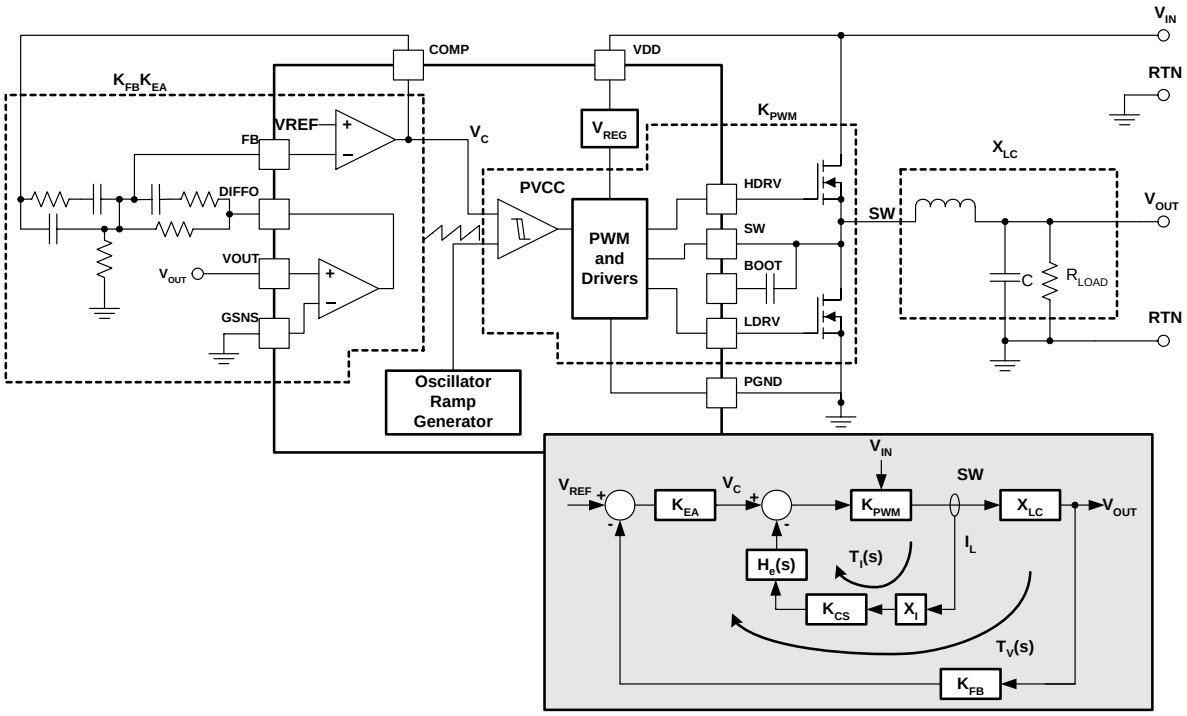

Fig. 6. CMC buck converter schematic and block diagram.

A. *Sampling Gain*

Since a peak current-mode controller acts as a first order sample and hold circuit, the sampling gain equals:

$$H_e(s) = \frac{s \times T_s}{e^{s \cdot T_s} - 1} \tag{10}$$

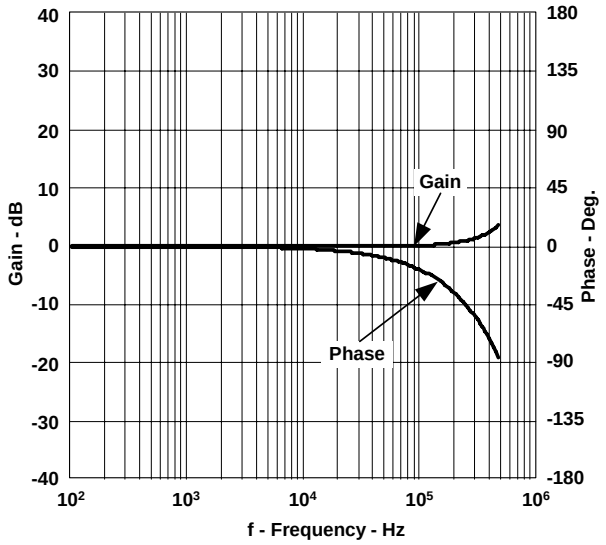

Fig. 7. $H_e(s)$.

The sampling gain introduces a gain boost and a phase lag beginning at about 1/10th the switching frequency. Fig. 7 indicates that the phase lag reaches 90° at about half of the switching frequency (or 500 kHz in this example). This effect predicts possible sub-harmonic oscillation in current-mode converters.

B. *Current Sensing*

This analysis divides the current feedback signal into two portions: a small-signal AC transfer characteristic and the slope information used to determine the modulator gain.

The current-sense AC transfer characteristic represents the small-signal current feedback to the control system. The transfer function derived using nodal analysis includes the effects of the complex filter model. Fig. 8 illustrates two methods of output current sensing, one method (upper), uses a resistor in series with the output inductor to sense current directly. The other method, (lower), uses an R-C network across the inductor to construct a signal similar to the inductor current waveform. (See Appendix C).

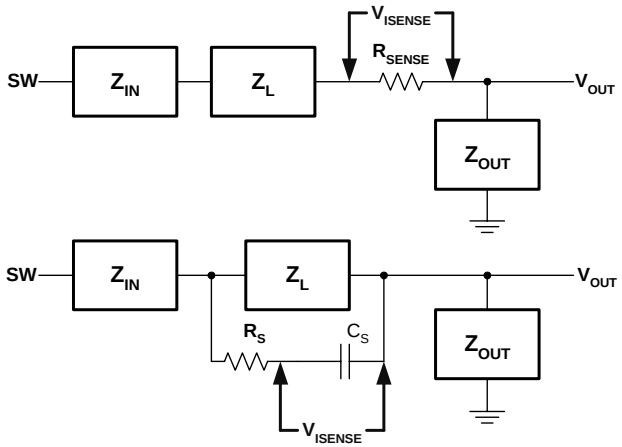

Fig. 8. Output current sensing.

By extending the methodology of Section II., sub section C, the duty cycle to current sense transfer function for simple resistor sensing equals:

$$X_i(s) = \frac{\Delta V_{ISENSE}}{\Delta V_{SW}} = \frac{R_{SENSE}}{Z_{LOAD}(s) + Z_{IN}(s) + Z_L(s) + R_{SENSE}} \tag{11}$$

and for R-C sensing equals:

$$X_i(s) = \frac{\Delta V_{ISENSE}}{\Delta V_{SW}} = \frac{1}{\left[Z_{LOAD}(s) + Z_{IN}(s) + R_S \times \left(1 + \frac{Z_{LOAD}(s) + Z_{IN}}{Z_L(s)} \right) \right] \times s \times C_S + \frac{Z_{LOAD}(s) + Z_{IN}}{Z_L(s)} + 1} \tag{12}$$

C. Modulator Gain

The VMC modulator gain depends on both the control voltage and the slope of the oscillator ramp. Current feedback sums the control voltage with a saw tooth waveform whish has a slope proportional to the slope of the inductor current. Fig. 9 shows a physical embodiment of a modulator in which the current feedback signal, scaled by a transconductance amplifier, subtracts from the error amplifier output voltage. Comparison of this composite signal with the oscillator ramp generates the PWM signal. This analysis depends only upon the relative slopes of the intersecting waveforms. Thus, a modulator that sums the current feedback signal with the oscillator ramp waveform produces the same results as the modulator of Fig. 9. This approach differs from others in that current feedback modifies a VMC system, rather than the reverse.

Referring to Fig. 8 and assuming V_{ISENSE} is small in amplitude compared to the switching waveform at SW, the slope of the current signal for direct resistor sensing equals (see equation (13)) and for R-C sensing equals (see equation (14)).

The effects of input voltage and load current variation appear in the equation for the on-time slope of the inductor current, and therefore they also appear in the expression for the modulator gain.

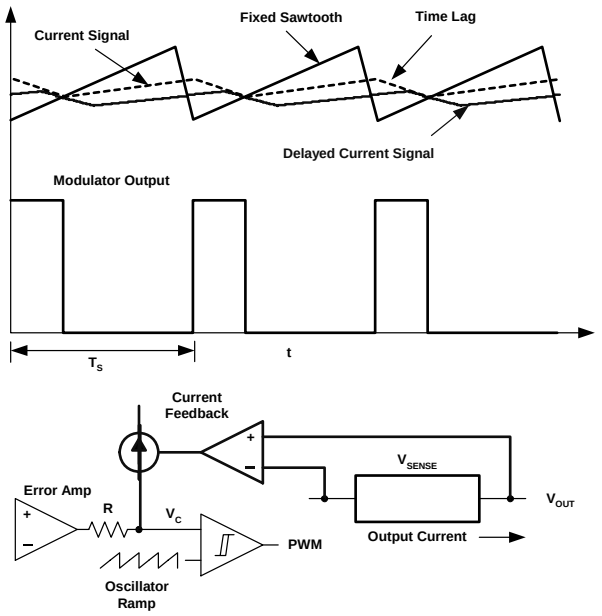

Fig. 9. Current feedback into the modulator.

For the example using R-C sensing, and assuming for now that $K_{CS}(s)$ is 12.5 over the frequency range, (see equation (15)).

The PWM gain now includes the effect of current feedback, decreasing modulator gain by an amount proportional to the slope of the current signal as shown in equation (16).

$$m_n = \frac{V_{IN} - V_{OUT} - I_{OUT} \times (R_{DS(on\_sw)} + R_L + R_{SENSE})}{L} \times R_{SENSE} \times K_{CS}(s) \tag{13}$$

$$m_n = \frac{V_{IN} - V_{OUT} - I_{OUT} \times (R_{DS(on\_sw)} + R_L)}{Rs \times Cs} \times K_{CS}(s) \tag{14}$$

$$m_n = \frac{12 - 3.3 - 5 \times (5.5\,m + 2.2\,m)}{9.1k\Omega \times 100\,n} \times 12.5 = 119\frac{mV}{\mu s} \tag{15}$$

$$K_{PWM} = \frac{1}{(m_C + m_n) \times T_s} = \frac{1}{(\frac{0.556V}{1\mu s} + \frac{0.119V}{1\mu s}) \times (1\mu s)} = 1.48\frac{1}{V} \tag{16}$$

D. Completing the Current Loop

The completed current loop ($T_i(s)$ in Fig. 6) described by the equation below is plotted in Fig. 10 for input voltages of 5 V and 12 V. The slope increases with increasing input voltage, in accordance with equation (14). However, the magnitude of this increase is less than that of the input voltage itself. The current loop gain therefore shows only a moderate increase with increasing input voltage. There is no phase change with a change in input voltage.

$$T_i(s) = V_{IN} \times K_{PWM} \times X_i(s) \times K_{CS}(s) \times H_e(s) \quad (17)$$

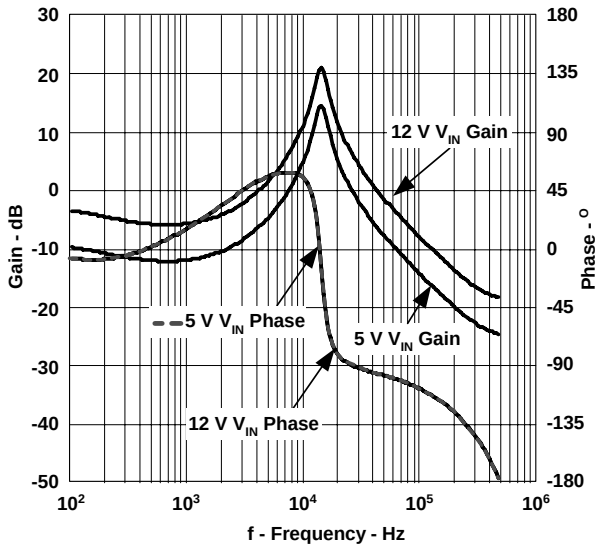

Fig. 10. Current loop gain, $T_i(s)$.

E. Control-to-Output Gain

The control-to-output transfer function of Fig. 6 equals:

$$Xco(s) = \frac{V_{OUT}(s)}{V_C(s)} = \frac{V_{IN} \cdot K_{PWM}(s) \times X_{LC}(s)}{1 + T_i(s)} \quad (18)$$

This equation makes clear the effect of the inner current loop on the overall transfer function. A current loop gain of zero reduces the transfer function to that of voltage-mode control (equation (9)). In this example, the small amount of current feedback further reduces the Q of the output filter.

Fig. 11 illustrates the control-to-output transfer function of equation (18) at input voltages of 5 V and 12 V. The gain increases modestly with increasing input voltage because of the relatively small amount of current feedback in this example. The control-to-output gain of a pure CMC modulator incorporating no VMC ramp would vary less over the input voltage range. The control-to-output gain of a pure VMC without any current feedback would vary more over the input voltage range.

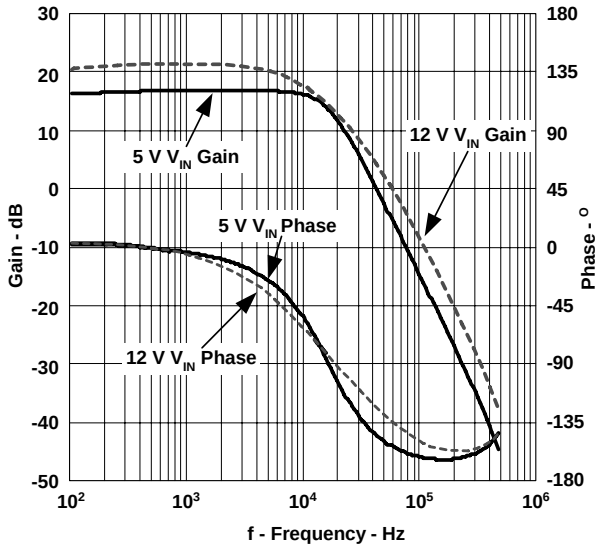

Fig. 11. Control to output transfer function.

IV. Including Component Parameter Effects

Having completed the basic model derivation, we now consider the effects certain component parameters have upon the control-to-output response.

A. Delay in PWM Path

Signals require time to propagate from the input terminals of the PWM comparator to the SW node. The PWM comparator, the PWM latch, the gate drivers, and even the power transistors themselves, each delay the signal by a finite amount. The accumulation of these time delays appears in the small-signal model as a phase lag. Incorporating a propagation time t_{DELAY} into the modulator gain gives:

$$K_{PWM}(s) = \frac{e^{-s \times t_{delay}}}{(m_C + m_n) \times T_s} \tag{19}$$

The illustrative example assumes a switching frequency of 1 MHz and a unity gain bandwidth goal of 200 kHz. The controller propagation delay of 100 ns adds to the 111-ns turn-on delay of the switch MOSFET[6] to generate a phase lag of 17° at 200 kHz (Fig. 12.). This phase lag significantly complicates efforts to obtain 45° of phase margin at the desires unity gain bandwidth.

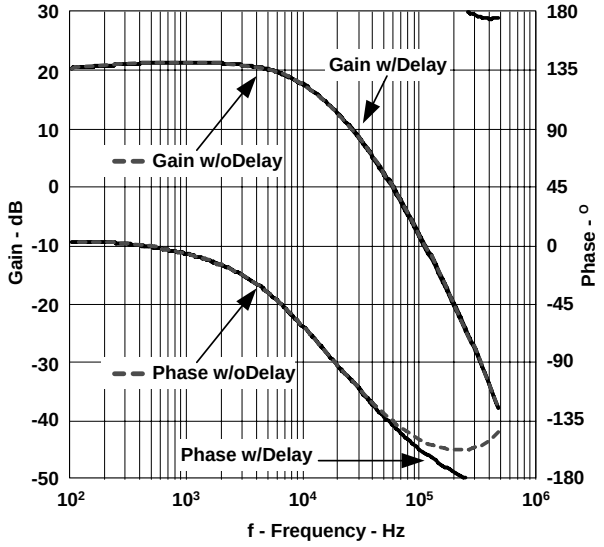

Fig. 12. Impact of PWM time delay.

B. Delay in the Current Sense Path

A signal delay also occurs in the current sense amplifier (K_{CS} in Fig. 6.). If the converter PWM on-time becomes shorter than the sum of the current sense and PWM delay times, then the current feedback slope at the time of PWM "decision" changes from the desired positive value seen during the on-time (Fig. 13. top), to a negative value seen during the off-time (Fig. 13. bottom). This in turn causes a step change in modulator gain, which if sufficiently large, can cause loop instabilities near that operating point.

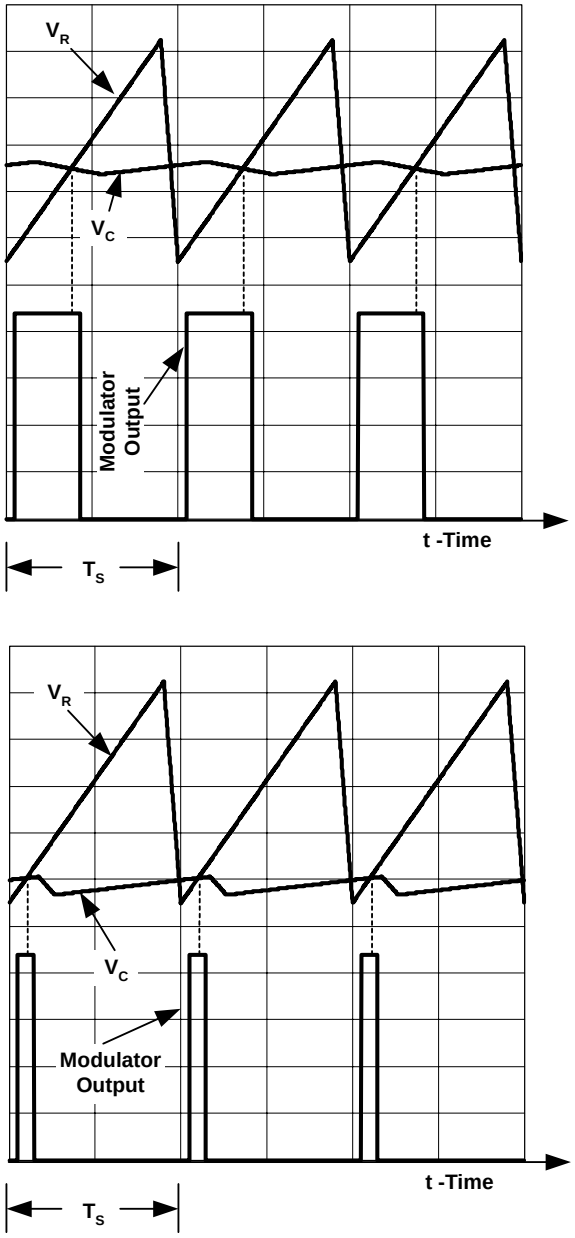

Fig. 13. Impact of current sensing delay.

To estimate the delay in the current sense path, evaluate the current sense amplifier gain-bandwidth curve at the switching frequency. This gives a first-order approximation of the delay through the amplifier even though the signal is not sinusoidal. In practice, this procedure requires first writing a transfer function based on the unity gain bandwidth and the open loop gain listed in the data sheet, and then evaluating this transfer function at the switching frequency to determine the propagation delay.

For the illustrative example, the amplifier transfer function approximately equals:

$$K_{CS}(s) = \frac{gm \times R}{1 + \frac{s}{2\pi \times \frac{UGBW}{gm \times R}}} \tag{20}$$

$$K_{CS}(Fs) = \frac{625\,\mu F \times 20\,k\Omega}{1 + \frac{2\,j\pi \times 1MHz}{2\pi \times \frac{30MHz}{625\,\mu F \times 20\,k\Omega}}} = 10.65 + 4.44\,j \tag{21}$$

Dividing the argument (phase angle) by the switching frequency yields the time delay.

$$t_{DELAY} = \frac{\arg(K_{CS}(s))}{2\pi \times Fs} \tag{22}$$

$$t_{DELAY} = \frac{\arg(K_{CS}(1MHz))}{2\pi \times 1MHz} = 64\,ns \tag{23}$$

To obtain the total time delay, add the amplifier delay to the PWM delay previously obtained. For the example, the total time delay equals 64 ns + 211 ns, or 275 ns. The modulator gain will therefore pass through a step change at a pulse width of 275 ns. Instability may occur at this point. On "either side" of this transition area, the gain will be constant. It is only with pulse widths at the decision point of the modulator that the gain will be unstable.

For the example, the PWM gain changes from the value of 1.48/V computed to a new value shown in equation (24).

At the transition point of 275 ns, and where S_f, the "off time" slope of the current waveform is shown in equation (25).

At 12-volt input, the gain shift becomes:

$$\Delta K = 20\log(1.96 - 1.48) = 6.6\,dB \tag{26}$$

The gain shift increase of 6.6 dB in the current loop results in only a 1.5 dB gain increase in the control-to-output transfer function and a phase increase of only 3.6° (Fig. 14).

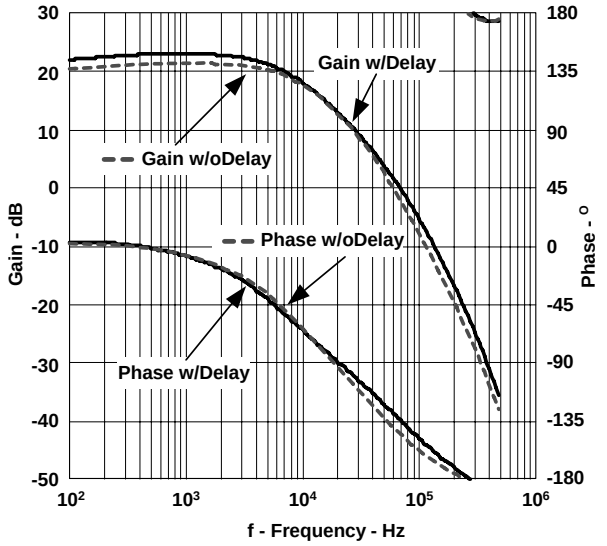

Fig. 14. Control to output due to modulator gain shift.

$$K_{PWM} = \frac{1}{(m_C + m_f) \times T_s} = \frac{1}{(\frac{0.556V}{1\mu s} + \frac{-0.047V}{1\mu s}) \times (1\,\mu s)} = 1.96\frac{1}{V} \tag{24}$$

$$m_f = \frac{V_{OUT} + I_{OUT} \times (R_{DS(on\_sr)} + R_L)}{R_S \times C_S} \times K_{CS} = \frac{3.3 + 5 \times (4.2\,m + 2.2\,m)}{9.1k\Omega \times 100\,n} \times 12.5 = \frac{0.046V}{\mu s} \tag{25}$$

V. Comparison to Measurement

Comparison of measured and predicted results puts the model to the test. The TPS40180 incorporates current-mode control with a large voltage-compensating ramp. Appendix A gives the details of the test circuit. The predicted results of the model developed in this paper closely follow the actual measurements of control-to-output gain and phase (Fig. 15.). By contrast, results predicted by previous models, correlate poorly with measured results at both low and high frequencies.

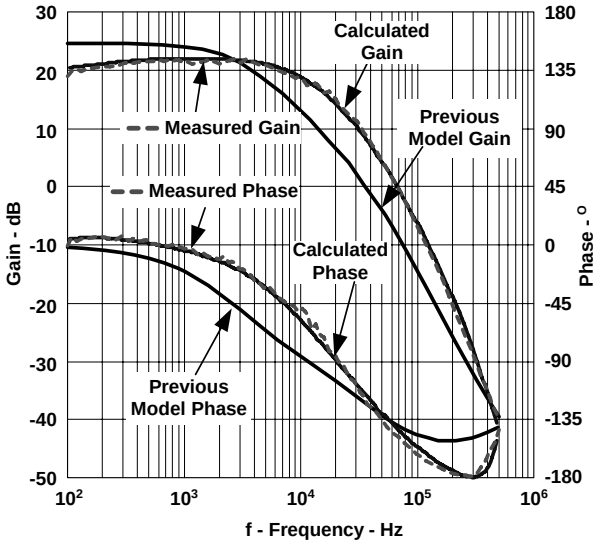

Fig. 15. Control to output comparison of results.

This converter, operating at a switching frequency of 1 MHz and a crossover frequency of 200 kHz, exhibits a gain 6 dB less, and a phase margin 24° degrees less, than previous models predict. The new model accurately predicts converter performance and thus reduces the number of design iterations required to achieve satisfactory results.

VI. Conclusions

As switching frequencies edge into the megahertz region, the effects of time lag and component bandwidth become significant contributors to converter loop behavior, creating the need for a more comprehensive analysis. The feedback loop model described deviates from traditional analysis by examining a system from a different perspective. In particular, 1) the small-signal feedback of the current sense signal follows as a function of the averaged signal fed to the filter network, and 2) the modulator gain equation now includes gain change and time delay effects. Arguably, where this analysis lacks direct insight into pole-zero locations and their effect on loop stability, it does allow better understanding of parameter variation effects upon loop performance.

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APPENDIX A. DC/DC CONVERTER EXAMPLE

A DC/DC converter using a prototype TPS40180 controller serves to correlate the model to an actual circuit. The converter is a 12-V to 3.3-V, 5-A DC/DC converter operating at 1 MHz. Important to the design evaluation are the following parameters:

CIRCUIT PARAMETERS

Input voltage	V_{IN} = 12 V
Output voltage	V_{OUT} = 3.3 V
Output current	I_{OUT} = 5 A
Output inductor	L = 1.3 µH with DCR Rl = 2.2 mΩ
Bulk output capacitors	C1 = 2 x 47 µF each with ESR1 = 3 mΩ and ESL1 = 4 nH
High frequency output capacitor	C2 = 1.0 µF with ESR2 = 2 mΩ and ESL2 = 3 nH
Upper switch MOSFET	Q1 = Si4866 with $R_{DS(on\_sw)}$ = 5.5 mΩ
Synchronous rectifier	Q2 = Si4336 with $R_{DS(on\_sr)}$ = 4.2 mΩ
Current sensing network	C_s = 100 nF, R_s = 9.1 kΩ

In addition to the circuit parameters listed above, the controller exhibits the following characteristics of importance:

CONTROLLER CHARACTERISTICS

Oscillator ramp amplitude	$V_{RAMPp\text{-}p}$ = 500 $mV_{p\text{-}p}$
Oscillator ramp discharge time	T_{DISCH} = 100 ns
Modulator-to-gate drive output delay time	T_{DELAY} = 100 ns
Current sense amplifier	Unity gain bandwidth = 30 MHz, g_m = 625 µS working into a 20-kΩ resistor
Gate drive voltage	5 V
Gate drive impedance	1 Ω

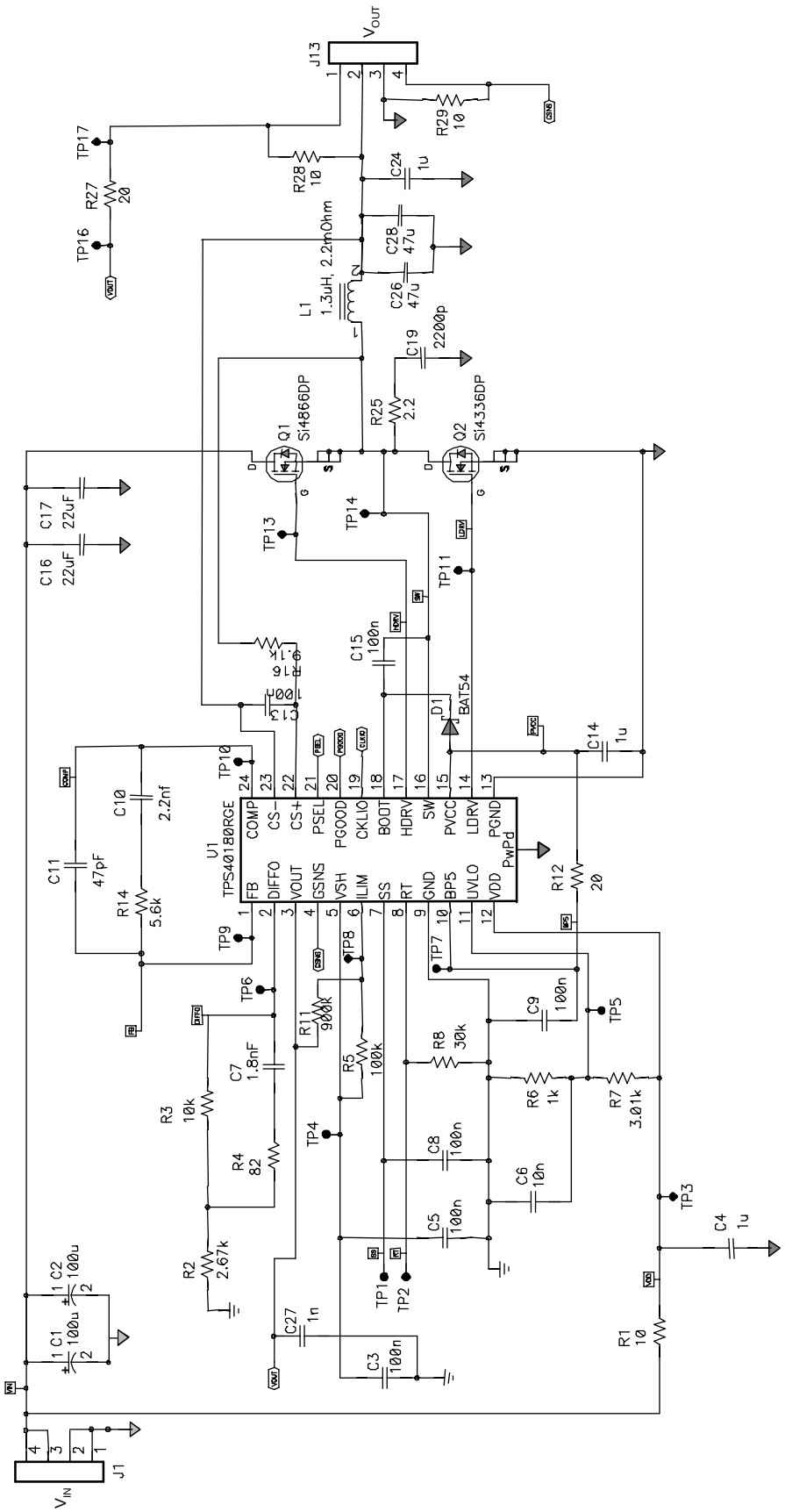

Fig. 16. 12-V to 3.3-V DC/DC converter.

APPENDIX B. DEFINITION OF SYMBOLS

C_s	Capacitor used to generate current equivalent ramp
D	Duty cycle of the converter
H_e	Sampling gain
I_{OUT}	Converter (average) DC output current
K_{CS}	Current sense amplifier gain
K_{EA}	Compensated error amplifier transfer function
K_{FB}	Output voltage divider gain
K_{PWM}	Pulse width modulator gain
L	Output filter inductor inductance
m_C	Slope of the modulator ramp, V_{RAMP}
m_f	Slope of current feedback waveform during the switch off time
m_n	Slope of current feedback waveform during the switch on time
$R_{DS(on\_sr)}$	On-resistance of synchronous rectifier MOSFET
$R_{DS(on\_sw)}$	On-resistance of upper switch MOSFET
R_L	Inductor DC resistance
R_s	Resistor used in RC sensing circuit
R_{SENSE}	Output current sense resistor
s	Frequency in radians
t_{DELAY}	Accumulated delay of modulator, drivers, and MOSFET turn-on
T_{DISCH}	PWM sawtooth discharge time
Ts	Switching period
T_i	Current loop gain
T_v	Voltage loop gain
V_C	Duty cycle control voltage (usually the output of the compensated error amplifier)
V_{IN}	Input voltage to converter
V_{ISENSE}	Voltage representation of the output current –feedback to the control loop
V_{OUT}	Converter output voltage
$V_{RAMPp\text{-}p}$	VMC modulator ramp amplitude for PWM
V_{SW}	Equivalent average voltage at the switching node (SW) of the converter
X_{CO}	Converter control-to-output transfer function
X_i	Current sense transfer function
X_{LC}	Output filter transfer function
Z_{IN}	Equivalent impedance of switching MOSFETs
Z_L	Impedance of the output filter inductor
Z_{LOAD}	Parallel impedance of the output capacitors and the load
Z_{OUT}	Impedance of the output capacitor(s) in parallel with the load

- The suffix (s) appended to a variable indicates it is a function of frequency.
- A Δ preceding a variable represents an incremental change in the variable's value.

APPENDIX C. DERIVATION OF R-C SENSING

By placing an R-C network across the inductor of an output filter, the voltage generated across the capacitor (C_S in Fig. 17.), will be a saw tooth waveform with a slope proportional to the input voltage. With proper selection of the values of the resistor and capacitor, the slope of the voltage across the capacitor will match the slope of the current through the inductor. Although this method does not measure output ripple current directly, the slope information developed is accurate enough for many feedback loop designs.

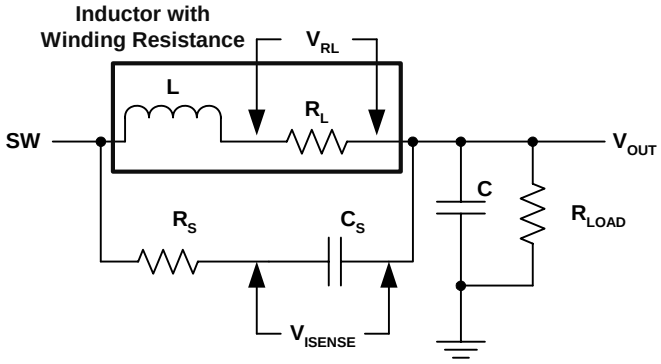

Fig. 17. R-C sensing.

Assuming the voltages V_{ISENSE} and V_{RL} are small compared to V_{SW} and V_{OUT}, the voltage across the equivalent inductor resistance equals:

$$V_{R_L} = (V_{SW} - V_{OUT}) \times \frac{R_L}{R_L + 2\pi Fs \times L} \tag{27}$$

and the capacitor voltage equals:

$$V_{ISENSE} = (V_{SW} - V_{OUT}) \times \frac{1}{2\pi Fs \times C_S \times R_S + 1} \tag{28}$$

Equating the two equations gives:

$$V_{ISENSE} = V_{R_L}; \frac{1}{2\pi Fs \times C_S \times R_S + 1} = \frac{R_L}{R_L + 2\pi Fs \times L} \tag{29}$$

Given the inductor (value and winding resistance) and arbitrarily selecting a value for C_S (0.1 µF is typical) the value of R_S equals:

$$R_S = \frac{L}{R_L} \times \frac{1}{C_S} \tag{30}$$

For the example,

$$R_S = \frac{1.3\,\mu F}{2.2\,m} \times \frac{1}{0.1\,\mu F} = 5.9\,k\Omega \tag{31}$$

Interestingly, an R_SC_S combination that *does not* match the L/R_L time constant can provide additional gain or attenuation of the current feedback signal. Exploration of equation (12) indicates that not only will the PWM gain be affected by a mismatch of time constants (via the adjustment of slope of the feedback signal) but also at low frequencies, there will be a gain shift where the low frequency dominance of the *Rl +sL* term is overshadowed by the series R_SC_S term. Fig. 18 illustrates an example of the effect when the R_SC_S time constant assumes a lower inductor resistance than is actually being used. This may occur if the sensing connection points include PCB trace resistance, or the resistance of the inductor increases with elevated temperature. This example assumes a 1.5-mΩ inductor resistance, resulting in a calculated R_S of 9.1 kΩ. The mismatch in time constants results in a low-frequency gain error.

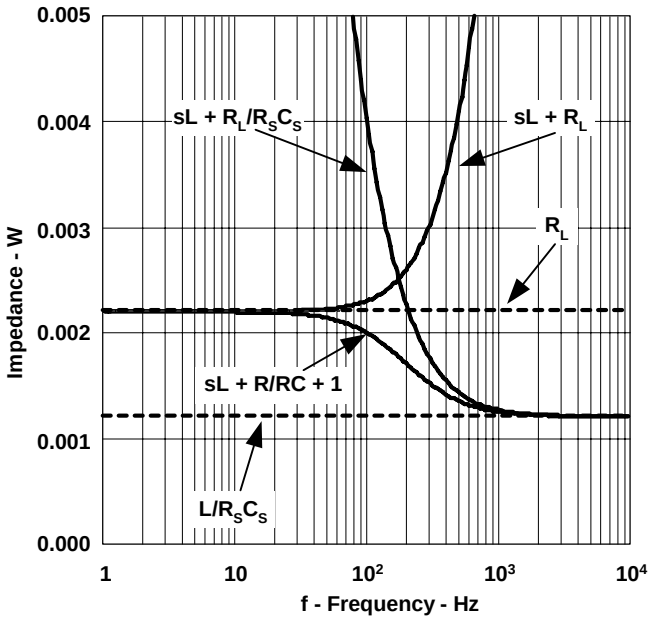

Fig. 18. RC mismatch to L/R.

At very low frequencies, the resistance of the inductor (2.2 mΩ) dominates the impedance. As the sweep frequency is increased, there is a transition to the impedance dominated by L/R_SC_S = 1.2 mΩ. The transition frequencies (at Rl/L = 318 Hz and $1/R_SC_S$ = 175 Hz) are low enough that the effect on closed loop performance is negligible. An understanding of the effect however, explains peculiar phenomena such as the increase in gain from 100 Hz to 1200 Hz as depicted in Fig. 15.