Topic 5

An Interleaved PFC Preregulator for High-Power Converters

Texas Instruments

An Interleaving PFC Pre-Regulator for High-Power Converters

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ABSTRACT

In higher power applications, to fully utilize the line, power factor correction (PFC) is a necessity. Passive solutions were developed first, which required bulky inductors and capacitors. To reduce the volume of these bulky solutions active PFC using a boost topology was developed. The active solutions had higher power densities than the passive solutions. Interleaving PFC pre-regulators is the next step in increasing PFC pre-regulator power densities, reducing the overall volume of the design. Interleaving will reduce magnetic volume and has the added benefit of reducing RMS current in the boost capacitor. This topic will evaluate the benefits of interleaving PFC pre-regulators.

I. SINGLE STAGE BOOST CONVERTER REVIEW

In PFC pre-regulators, the most popular topology used is a boost converter. This is because boost converters can have continuous input current that can be manipulated with average current mode control techniques to force input current to track changes in line voltage. Fig. 1 shows a traditional single stage boost. The inductor ripple current (ΔIL1) is directly seen at the converter's input and will require filtering to meet EMI specifications. The diode output current (I1) is discontinues and needs to be filtered out by the output capacitor (C_{OUT}). In this topology, the output capacitor ripple current (I_{COUT}) is very high and is the difference between I1 and the dc output current (I_{OUT}).

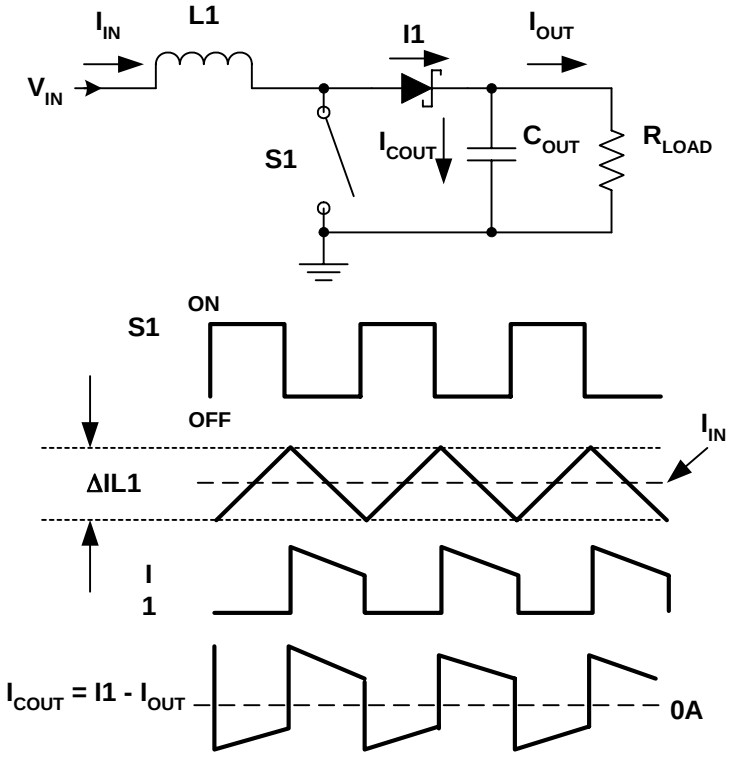

Fig. 1. Traditional boost stage.

II. BENEFITS OF TWO PHASE INTERLEAVING BOOST CONVERTERS

Fig. 2 shows the functional diagram of a two phase interleaved boost converter. The interleaved boost converter is simply two boost converters in parallel operating 180° out of phase. The input current is the sum of the two inductor currents IL1 and IL2. Because the inductor's ripple currents are out of phase, they tend to cancel each other and reduce the input ripple current caused by the boost inductors. The best input inductor ripple current cancellation occurs at 50 percent duty cycle. The output capacitor current is the sum of the two diode currents (I1 + I2) less the dc output current. Interleaving reduces the output capacitor ripple current (I_{OUT}) as a function of duty cycle. As the duty cycle approaches 0 percent, 50 percent and 100 percent duty cycle, the sum of the two diode currents approaches dc. At these points, the output capacitor only has to filter the inductor ripple current.

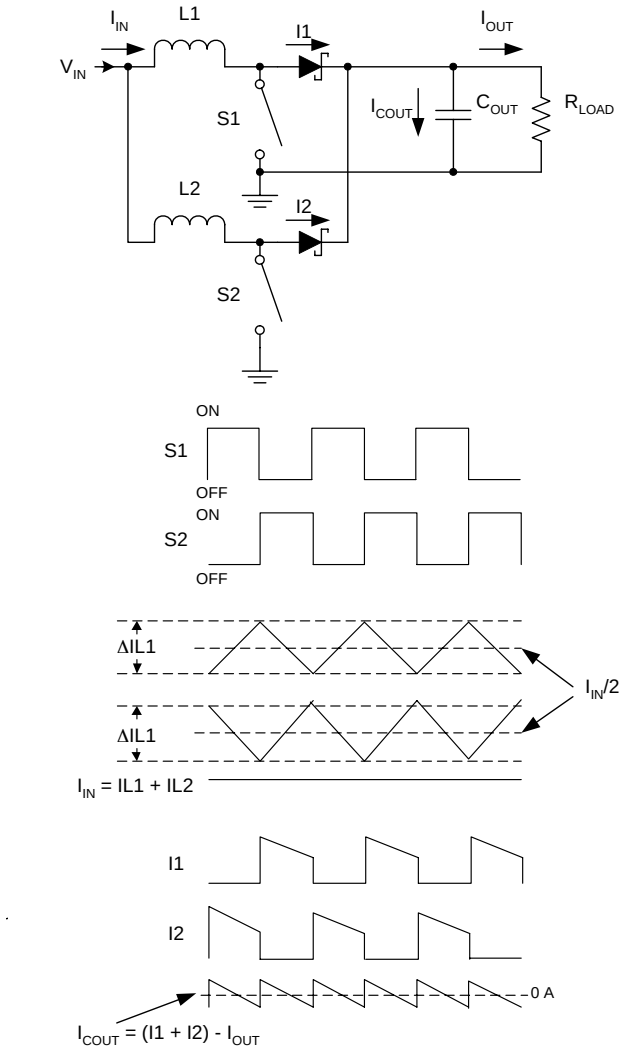

Fig. 2. Interleaved boost stage.

III. Input Ripple Current Reduction as a Function of Duty Cycle

The following equations show how the ratio of input ripple current to the inductor ripple current (K(D)) vary with changes in duty cycle. Fig. 3 shows how K(D) varies with changes in duty cycle.

$$K(D) = \frac{\Delta I_{IN}}{\Delta I_{L1}}$$

$$K(D) = \frac{1 - 2D}{1 - D} \text{ if } D \le 0.5$$

$$K(D) = \frac{2D - 1}{D} \text{ if } D > 0.5$$

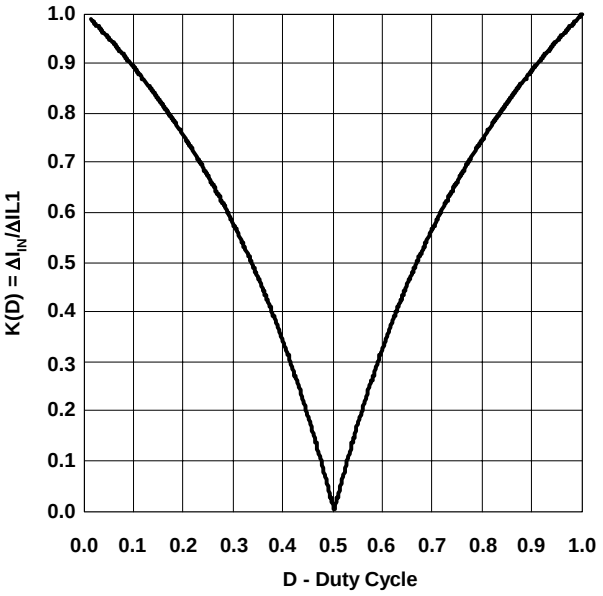

Fig. 3. Input ripple current reduction.

In PFC pre-regulators the duty cycle (D(θ)) is not constant and will varies with changes in line phase angle (θ) and input voltage ($V_{IN}(\theta)$). The amount of duty cycle variation for universal applications can be quite large. This variation in duty cycle can be observed by evaluating a converter that was designed for a universal input of 85 V to 265 V RMS with a regulated 385 V dc output. At low line the duty cycle (D1(θ)) will vary from 100% to 69% and at high line the duty cycle (D2(θ)) will vary from 100% down to 2%. The inductor ripple current cancellation will not be 100% throughout the line cycle. However, it is good enough to drastically reduce the input ripple current for a given inductance. The highest ripple current in this example would occur at the peak of low line with a duty cycle of 69%. The input ripple current at this duty cycle will be 55% of the individual inductor ripple current. When the converter is operating at 2% and 100% duty cycle there is very little inductor ripple current cancellation. However, at these duty cycles the interleaved PFC pre-regulator has very little inductor ripple current. Overall, the input ripple current of the PFC boost will be 55% of what it would have been in a single phase PFC designed for the same power level and inductance. This can be found by evaluating Fig. 3.

$$V_{IN}(\theta) = V_{IN(rms)} \times \sqrt{2} sin(\theta)$$

$$D(\theta) = \frac{V_{OUT} - V_{IN}(\theta)}{V_{OUT}}$$

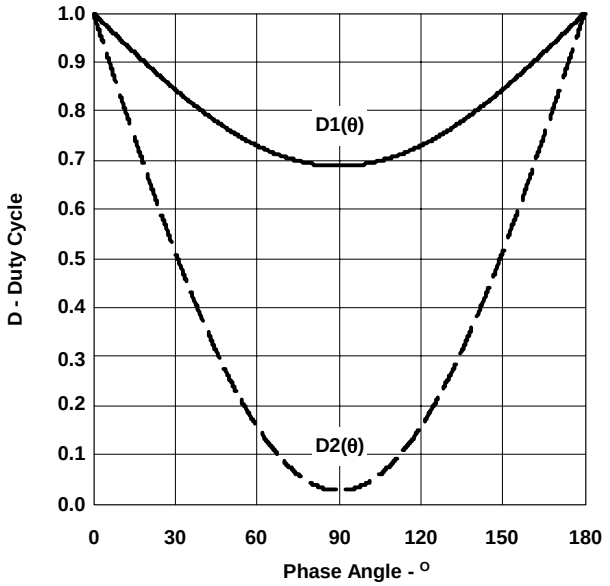

Fig. 4. Duty cycle variation in universal PFC pre-regulator.

IV. Input Ripple Current Cancellation Can Reduce Boost Magnetic Volume

The inductor ripple current cancellation allows the designer to reduce boost inductor magnetic volume. This is due to the energy storage requirement of the two interleaved inductors being half that of single stage pre-regulator designed for the same power level, switching frequency and inductance.

Single stage inductor energy (E_{Single}):

$$E_{SINGLE} = \frac{1}{2} LI^2$$

Two phase total inductor energy ($E_{Interleaved}$):

$$E_{INTERLEAVED} = \frac{1}{2} L\left(\frac{I}{2}\right)^2 + \frac{1}{2} L\left(\frac{I}{2}\right)^2 = \frac{1}{4} LI^2$$

The reduction in energy storage does not directly translate into magnetic volume reduction. A designer could expect to see up to a 25% reduction in magnetic volume going from a single phase PFC pre-regulator to a dual phase interleaved PFC. This will be discussed later in the paper with actual design examples.

Interleaving PFC pre-regulators if done in this fashion will not increase the size of the EMI filter. A common design practice is to select the switching frequency of the power converter below the EMI lower limit of 150 kHz. The second harmonic of switching frequency would be twice the fundamental and will most likely be in the EMI band and would need to be filtered to meet specifications. Interleaving two pre-regulators will cause the input to see a switching frequency that is twice the switching frequency of a single phase. This means the fundamental switching frequency of the converter will most likely be pushed into the EMI band and will be at the second harmonic of an individual stage's switching frequency. However, the input ripple current at this frequency will be reduced by a factor of two. This should not put any additional constraints on the EMI filter.

V. The EMI Filter Can Also be Reduced

Depending on the design parameters just interleaving PFC pre-regulators could reduce the size of the EMI filter. For example in European designs and boost follower applications where the boost voltage is just above the peak of the input line voltage the highest inductor ripple current occurs at 50% duty cycle. From the graph in Fig. 3 it can be observed when the converter is operating at 50% duty cycle the inductor ripple currents would cancel each other out. In this case the EMI filter would be drastically reduced just by interleaving.

The designer also has the option of running the interleaved pre-regulator at a lower switching frequency and increase the boost inductance slightly to reduce input ripple current. If this is done correctly the designer could decrease the size of the EMI filter without increasing the size of the boost inductor volume compared to a single stage pre-regulator approach. The designer may be able to reduce both the EMI filter; as well as, the boost inductor if the converter's switching frequency is not reduced too much.

VI. Output Capacitor Ripple Current Reductions as a Function of Duty Cycle

Interleaving PFC pre-regulator stages has the added benefit of reducing the output capacitor RMS current. Fig. 5 shows the normalized output capacitor RMS current in a single stage boost ($I_{COUT1}(D)$) and in a two stage interleaved boost converter ($I_{COUT2}(D)$) as a function of duty cycle. Knowing that the duty cycle in universal PFC pre-regulator applications varies from 100% to 2% and studying Fig. 5 it can be observed that interleaving will drastically reduce output capacitor RMS current. In this example the RMS current would be cut in half. This reduction in RMS current will reduce electrical stress in the output capacitor and improve the converter's reliability.

$$I_{COUT1}(D) = \sqrt{(1-D)\times(1-D)^2}$$

$$I_{COUT2}(D) = \frac{1}{2}\sqrt{(1-2D)\times(1-2D)^2} \quad \text{if } D \le 0.5$$

$$I_{COUTI2}(D) = \frac{1}{2}\sqrt{(2-2D)\times(2-2D)^2} \quad \text{if } D > 0.5$$

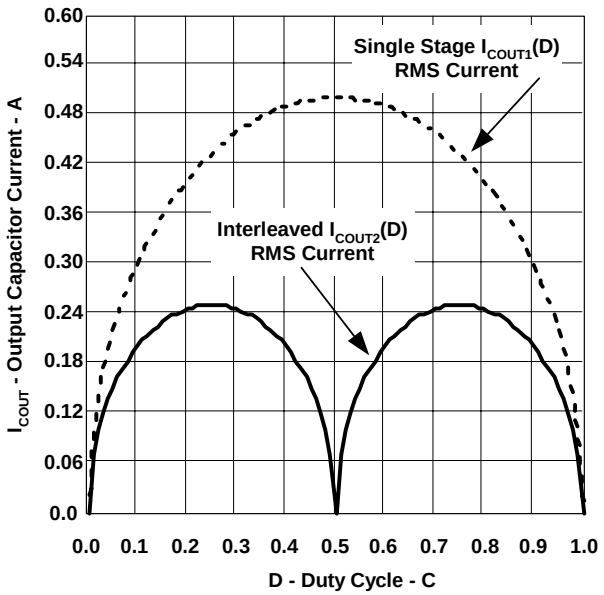

Fig. 5. Normalized output capacitor RMS currents as a function of D.

VII. 350-W, Two Phase Interleave PFC Prototype

To evaluate some of the benefits of interleaving a 350-W two phase interleaved PFC pre-regulator was constructed. This prototype was designed for a universal input of 85 V to 265 V RMS. The boost output voltage (V_{OUT}) for the design was 385 V_{DC}. The circuit was designed for a switching frequency (f_S) of 100 kHz to limit switching losses. The prototype used 600-µH inductors for L1 and L2. The output capacitor (C_{OUT}) needed for the design was a 220-µF electrolytic capacitor. A functional schematic of the circuit is presented in Fig. 6.

VIII. Lab Results

The largest inductor ripple current occurs when the converter operates at low line input at the peak of line. The oscilloscope plot in Fig. 7 shows the inductor ripple current cancellation at the peak of line when the input is 85 V_{RMS}. CH1 is L1 inductor current, CH2 is L2 inductor current. M1 is the input current which is the sum of inductor currents L1 and L2. The current probes were set with 2 A/Div. ratio. From this plot it can observed that the input ripple current is 55% of the individual inductor current. The reduction in input ripple current agrees with the graph of Fig. 3 for 69% duty cycle.

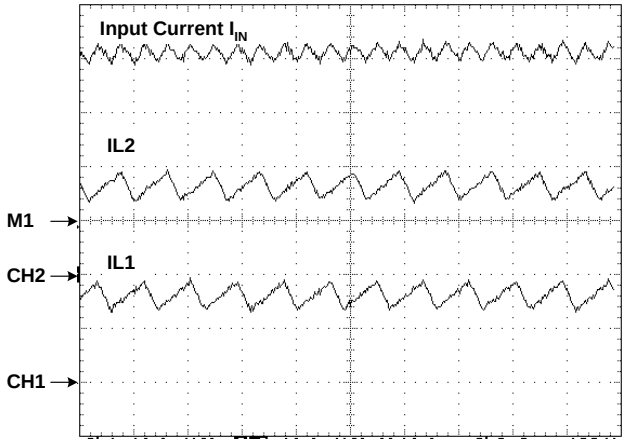

Fig. 7. Inductor ripple current, P_{OUT} = 350 W.

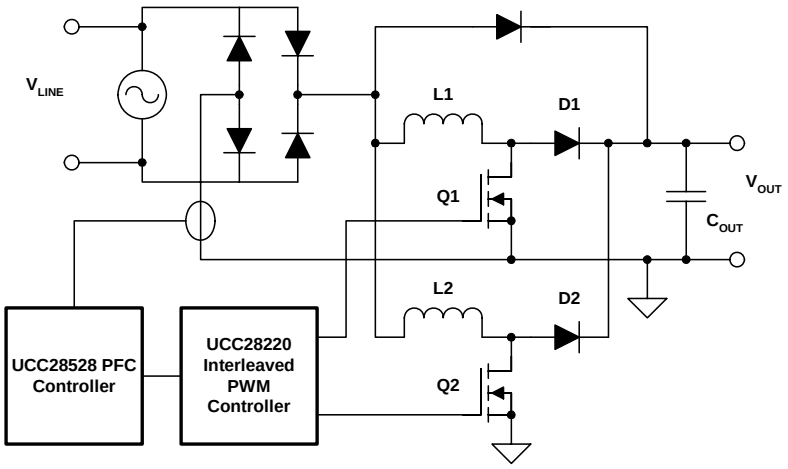

Fig. 6. Dual interleaved PFC.

Figs. 8 and 9 show the input and inductor ripple currents at maximum load at minimum and maximum line voltage. CH1 and CH2 are inductor current L1 and L2. M1 is the input current to the converter and is the sum of L1 and L2. The current probe was set with 2 A/Div. ratio. From these waveforms, it can be observed that high frequency input ripple current is much less than the individual phase's boost inductor current. If this was a single stage topology the full inductor ripple current would be seen at the input of the converter.

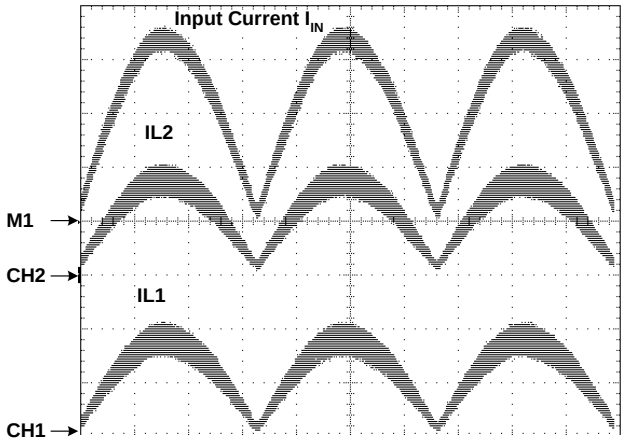

Fig. 8. Input current at V_{IN} = 85 V, 2 A/Div.

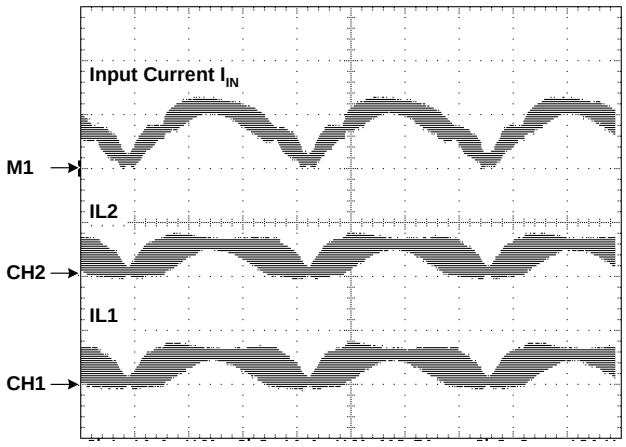

Fig. 9. Input current at V_{IN} = 265 V, 2 A/Div.

The following equations was used to calculate the highest RMS current in the output capacitor. The highest ripple current occurs at the minimum input ($V_{IN(min)}$) of 85 V RMS. The calculation is based on half a line cycle of the 50 Hz line (f_{LINE}). The duty cycle of each boost stage (D1(t)) at low line varies from 100% to 69%. The estimated output capacitor RMS current ($I_{COUT(rms)}$) was 1 A.

$$Iterations = \frac{f_S}{2 \times f_{LINE}}$$

$$Step = \frac{\frac{1}{2 \times f_{LINE}}}{Iterations}$$

$$I_{IN}(t) = \frac{P_{OUT} \times \sqrt{2}}{V_{IN(min)}} \times sin(\omega \times t)$$

The RMS current in the boost capacitor was measured at 1 A, which is less than half of what it would be in a single stage PFC pre-regulator with the same power requirements.

$$I_{Cout\_rms} = \sqrt{\frac{\sum_{n=1}^{Iterations} I_{IN}(n \times Step)^2 \times \sqrt{\frac{1}{2}\sqrt{(2 - 2D1(\omega \times n \times Step)) \times (2 - 2D1(\omega \times n \times Step))^2}}}{Iterations}} \approx 1\ A$$

IX. Evaluate Inductor Ripple Current Cancellation in Three and Four Phase Interleaved PFC Pre-regulators

The following equations and the graph in Fig. 10 show how the ratio of input ripple current to inductor ripple current vary with changes in duty cycle for two, three and four phase interleaved PFC pre-regulators. Note these equations are based on the boost converters operating in continues conduction mode (CCM).

Two phase input current to inductor current ratio as a function of D (K2(D)):

$$k2(D) = \begin{cases} \dfrac{1-2D}{1-D} \; if \; D \le \dfrac{1}{2} \\ \dfrac{1-2\times(1-D)}{1-(1-D)} \; if \; D > \dfrac{1}{2} \end{cases}$$

Three phase input current to inductor current ratio as a function of D (K3(D)):

$$k3(D) = \begin{cases} \dfrac{1-3D}{1-D} \; if \; D \le \dfrac{1}{3} \\ \dfrac{1}{3}\times\dfrac{-9\times D+9\times D^2+2}{(-1+D)\times D} \; if \; \dfrac{1}{3} < D < \dfrac{2}{3} \\ \dfrac{3\times D-2}{D} \; if \; D \ge \dfrac{2}{3} \end{cases}$$

Four phase input current to inductor current ratio as a function of D (K4(D)):

$$k4(D) = \begin{cases} \dfrac{1-4\times D}{1-D} \; if \; D \le \dfrac{1}{4} \\ \dfrac{1}{2}\times\dfrac{-6\times D+8\times D^2+1}{(-1+D)\times D} \; if \; \dfrac{1}{4} < D < \dfrac{2}{4} \\ \dfrac{1}{2}\times\dfrac{-10\times D+8\times D^2+3}{(-1+D)\times D} \; if \; \dfrac{2}{4} < D < \dfrac{3}{4} \\ \dfrac{4\times D-3}{D} \; if \; D \ge \dfrac{3}{4} \end{cases}$$

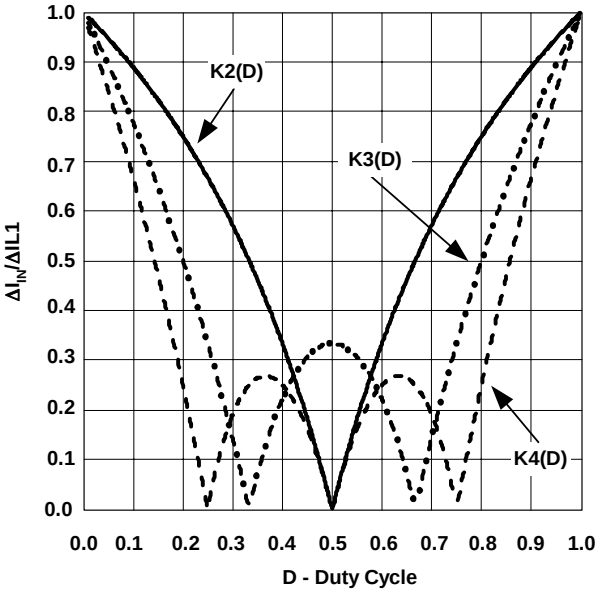

Fig. 10. Ratio of input ripple current/inductor ripple vs. duty cycle (D).

X. The Total Inductor Energy is Reduced for each Additional Phase

For each additional interleaved phase added will reduce the total inductor energy required by the design, when compared to a single stage PFC pre-regulator and a n phase interleaved pre-regulator. The graph in Fig. 11 shows the percent reduction in total inductor energy (%_Energy_Reduction) required in the design going from a single phase boost to 4 phase interleaved pre-regulator. From this graph it can be observed that the total energy going from a single phase to a two phase interleaved power converter will be reduced by 50%. A three phase interleaved pre-regulator will take roughly 67% less total inductor energy compared to a single phase approach. A four phase interleaved PFC pre-regulator will reduce the total inductor energy required by the design by 75%. Interleaving reduces the total energy required by the design which will allow the total boost inductor volume to be reduced. However, there is not an easy mathematical calculation to show the reduction in boost magnetic volume by interleaving. The reduction in magnetic volume will vary depending on the magnetic cores that are selected. The best way to evaluate the reduction in boost magnetic volume is by going through a theoretical design using similar magnetic cores.

In the following equations that calculate energy and energy reduction n represents the total number of interleaved phases in the pre-regulator.

Total multiple phase inductor energy ($E_{Interleaved}(n)$).

$$E_{Interleaved}(n) = \sum_{k=1}^{n} \frac{1}{2} L \left(\frac{I}{n} \right)^2$$

$$\%\_Energy\_Reduction(n) = \left(\frac{1 - \sum_{k=1}^{n} \left(\frac{1}{n} \right)^2}{1} \right) \times 100$$

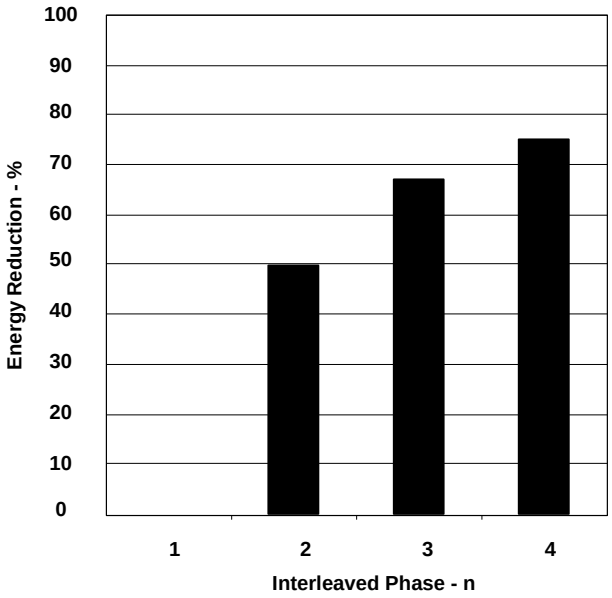

Fig. 11. Percent of total inductor energy reduction.

XI. MAGNETIC VOLUME REDUCTION

To show how interleaving PFC pre-regulators can reduce magnetic volume a theoretical design of boost inductors was conducted for a universal 500-W PFC pre-regulator for a single phase to a four phase PFC pre-regulator. The output of the converters was set at 385 V. The inductance (L) was chosen based on the inductance for a four phase design. This would ensure the inductance would work for 1- through 4-phase interleaved PFC applications. Also the amount of boost inductor ripple chosen was small enough that the ac portion of the inductor ripple current would be negligible. The following equations were used to select the area products required for the inductors for the four different designs. In the following equations n represents the number of interleaved phases in the pre-regulators.

$$I_{PEAK} = \frac{P_{OUT(max)} \times \sqrt{2}}{V_{IN(min)}}, \text{ peak input current}$$

$$L = \frac{\frac{V_{OUT}}{2} \times 0.5}{\frac{I_{PEAK}}{4} \times 0.3 \times 100\ kHz}$$

$\Delta B = 0.2\ T$, change in flux density

$$Cd = \frac{3.95 \times 10^6\ A}{m^2}, \text{ current density}$$

$Ku = 0.4$, winding factor

$$WaAc(n) = \frac{L \times \frac{I_{PEAK}}{n}}{\Delta B} \times \frac{I_{RMS}}{Ku \times Cd}$$

$$WaAc(n) = \frac{L \times \frac{I_{PEAK}}{n}}{\Delta B} \times \frac{\frac{I_{PEAK}}{n \times \sqrt{2}}}{Ku \times Cd}$$

To do a true comparison of inductor volume reduction required using the same magnetic core type. One of the more efficient core sets to wind is an EE core set. For this example EE cores from Mag-Inc were selected for the individual designs. Fig. 12 shows the mechanical drawing of the EE cores used for this example.

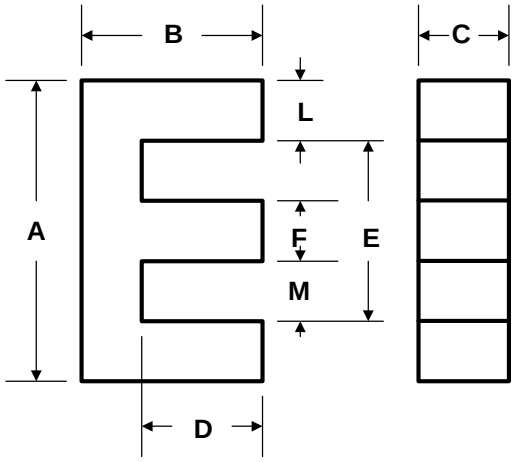

Fig. 12. Mechanical drawing of Mag-Inc EE core.

The estimated volume of the boost inductor ($V_{INDUCTOR}$) will be based on magnetic core (V_{CORE}) volume and exposed copper winding volume (V_{COPPER}.) This evaluation will not take into account bobbin size and was also based on dimension B of the E core being trimmed to get the area product as close to calculated as possible.

$$V_{CORE} = A \times (2 \times B) \times C$$

$$V_{COPPER} = 2 \times (2 \times D \times M) \times (A - 2 \times L)$$

$$V_{INDUCTOR} = V_{CORE} + V_{COPPER}$$

To show the reduction in boost inductor volume Table I. was constructed for a single phase through a four phase interleaved PFC pre-regulator. The following equation was used to calculate the reduction in total inductor magnetic volume (% Reduction in Inductor Volume) as compared to a single phase PFC inductor. $V_{INDUCTOR}$ (1) is the volume of a tradition single phase pre-regulators boost inductor. Variable $V_{INDUCTOR}(n)$ is the volume of a single inductor in a multiphase boost pre-regulator where n is the total number of phases in the pre-regulator used in the reduction comparison. This exercise showed that the reduction in total magnetic volume was much less than the total energy reduction that was calculated previously. However, interleaving reduced the magnetic volume by 32% to 51% depending on the number of phases that were used in the design.

XII. EMI FILTER REDUCTION FOR 3RD AND 4TH PHASE

Form Fig. 10 it can be observed that the three phase inductor ripple current is completely cancelled at 33% and 66% duty cycle. In universal designs a three phase system would reduce the size of the EMI filter. This is because the inductor ripple current in a universal design is at its maximum at the peak of low line which has a duty cycle around 69%. At this point the input ripple current would be 10% of the inductor ripple current. The reduction in input ripple current should result in a reduction of the size of the EMI filter.

The four phase system has almost no ripple current when the converter is operating at 25%, 50%, 75% duty cycle. In European and boost follower pre-regulators interleaving with four phases will also reduce the size of the EMI filter just by interleaving. This is due to the maximum inductor ripple that occurs at 50% duty cycle being 100% cancelled at the input of the converter. Also the 4-phase inductor ripple current cancellation curves show that overall input ripple current should be much less than a two phase interleaved converter for these applications.

$$\%\ reduction\ in\ inductor\ volume = \left(\frac{V_{INDUCTOR}(1) - n \times V_{INDUCTOR}(n)}{V_{INDUCTOR}(1)} \right) \times 100$$

TABLE I. BOOST INDUCTOR MAGNETIC VOLUME REDUCTION

	WaAc	Mag-Inc. EE Core Set	A	B	C	D	E	F	L	M	A_C	$V_{INDUCTOR}$ (h)	% Reduction In Inductor Volume
Units	cm^4		mm	mm	mm	mm	mm	mm	mm	mm	cm^2	cm^3	%
# of Phases													
1	23.228	48020-EC	80.00	24.862	19.80	14.962	59.30	19.80	9.90	19.80	3.920	150.099	0
2	5.807	45528-EC	54.90	16.941	20.60	7.841	37.50	16.80	8.38	10.70	3.461	51.118	32
3	2.581	44020-EC	42.80	13.481	15.40	7.381	30.40	11.90	5.94	9.54	1.833	26.480	47
4	1.452	44016-EC	42.80	13.204	9.00	7.104	30.40	11.90	5.94	9.54	1.071	18.554	51

XIII. Output Capacitor Ripple Current Cancellation in Three and Four Phase Interleaved PFC Pre-Regulators

Each individual added phase will continue to reduce the RMS current in the boost capacitor. However, the amount of reduction decreases with each additional phase. Please refer to Fig. 13 for a normalized output capacitor RMS current for a single phase boost through 4 phase interleaved boost converter.

The equations below gives the normalized output capacitor RMS current ($I_{COUT1}(D)$) converter in a single stage PFC pre-regulator as a function of duty cycle (D).

$I_{COUT1}(D)$ is the normalized output capacitor RMS current as a function of D.

$$I_{COUT1}(D) = 1\sqrt{(1-D)-(1-D)^2}$$

$I_{COUT2}(D)$ is the normalized output capacitor RMS current as a function of D.

$$I_{COUT2}(D) = \begin{cases} \frac{1}{2}\sqrt{(1-2D)-(1-2D)^2} \ if \ D < \frac{1}{2} \\ \frac{1}{2}\sqrt{(2-2D)-(2-2D)^2} \ if \ D \geq \frac{1}{2} \end{cases}$$

$I_{COUT3}(D)$ is the normalized output capacitor RMS current as a function of D.

$$I_{COUT3}(D) = \begin{cases} \frac{1}{3}\sqrt{(1-2D)-(1-3D)^2} \ if \ D \leq \frac{1}{3} \\ \frac{1}{3}\sqrt{(2-2D)-(2-3D)^2} \ if \ \frac{1}{3} < D < \frac{2}{3} \\ \frac{1}{3}\sqrt{(3-2D)-(3-3D)^2} \ if \ D \geq \frac{2}{3} \end{cases}$$

$I_{COUT4}(D)$ is the normalized output capacitor RMS current as a function of D.

$$I_{COUT4}(D) = \begin{cases} \frac{1}{4}\sqrt{(1-4D)-(1-4D)^2} \ if \ D \leq \frac{1}{4} \\ \frac{1}{4}\sqrt{(2-4D)-(2-4D)^2} \ if \ \frac{1}{4} < D < \frac{2}{4} \\ \frac{1}{4}\sqrt{(3-4D)-(3-4D)^2} \ if \ \frac{2}{4} < D < \frac{3}{4} \\ \frac{1}{4}\sqrt{(4-4D)-(4-4D)^2} \ if \ D \geq \frac{3}{4} \end{cases}$$

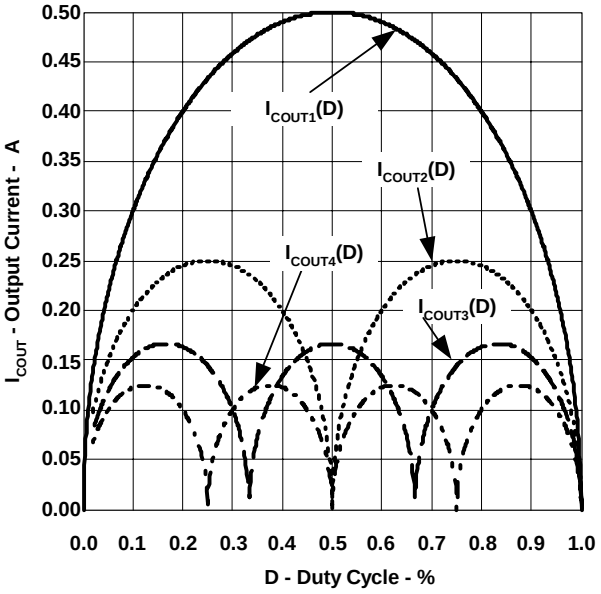

Fig. 13. Output capacitor RMS current.

XIV. EFFICIENCY

Interleaving and paralleling power converters can increase the efficiency of the power converter; as long as, the inductor ripple currents are kept within reason. The semiconductor switching losses will remain roughly the same. The I^2R losses should be reduced with each additional phase. However, if the inductor currents have excessive inductor ripple the higher RMS currents will cause greater conduction losses driving down efficiency. Also at lower power levels where the switching losses dominate interleaving will not show a drastic improvement in efficiency.

Single phase conduction losses:

$$P_{SINGLE} = I^2R$$

Two phase conduction losses:

$$P_{2\_PHASE} = \left(\frac{I}{2}\right)^2 R + \left(\frac{I}{2}\right)^2 R = \frac{I^2}{2} R$$

Three phase conduction losses:

$$P_{3\_PHASE} = \left(\frac{I}{3}\right)^2 R + \left(\frac{I}{3}\right)^2 R + \left(\frac{I}{3}\right)^2 R = \frac{I^2}{3} R$$

Four phase conduction losses:

$$P_{4\_PHASE} = \left(\frac{I}{4}\right)^2 R + \left(\frac{I}{4}\right)^2 R + \left(\frac{I}{4}\right)^2 R + \left(\frac{I}{4}\right)^2 R = \frac{I^2}{4} R$$

The 350-W prototype had greater than 91% efficiency over line and load.

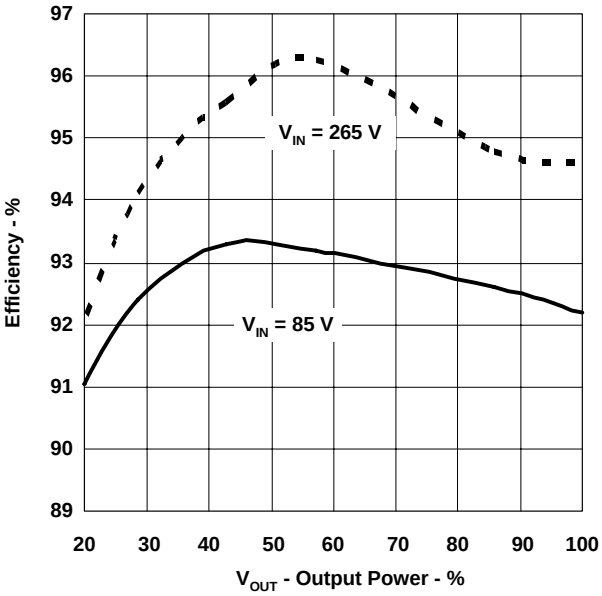

Fig. 14. Prototype efficiency.

XV. Conclusion

Interleaving PFC pre-regulators has many benefits. It can reduce EMI and boost inductor magnetic volume. The amount of reduction varies and depends on the design requirements and design tradeoffs. The designer may choose to reduce either the boost inductor magnetic volume or cut back the switching frequency to reduce the size of the EMI filter. In some cases just adding an additional phase will reduce the size of the EMI filter. Interleaving also reduces the RMS current in the boost capacitor greatly reducing electrical over stress on the capacitor. However, the complexity and cost of the design will increase with each additional phase.

XVI. Acknowledgements

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