High Power Factor and High Efficiency—You *Can* Have Both

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ABSTRACT

Although improving the power-supply power factor (PF) can offer significant and necessary reductions in distribution losses, it is usually assumed that adding an active power-factor correction (PFC) stage will reduce the supply's internal efficiency. It doesn't have to be this way. This topic shows that several new system architectures are possible that can minimize system losses, accommodate a wide range of AC line voltages, and meet power-quality requirements.

I. INTRODUCTION

Active power-factor correction (PFC) circuits are presently used in virtually all power supplies intended for professional use and are starting to appear in very cost-sensitive consumer applications, such as power supplies for personal computers. The widespread use of PFC circuits is a result of regulatory activity that started in Europe over a decade ago, culminating in the IEC standard EN61000-2-3. By limiting the harmonic content injected into the AC utility line, EN61000-2-3 indirectly imposes a high power-factor (PF) requirement on nonlinear loads such as power supplies. This topic discusses the benefits (and some potentially negative effects) of PFC and its effect on conversion losses, and investigates ways to improve the overall efficiency.

II. REVIEW OF THE PF CONCEPT

The PF is the ratio of the real power (average power in watts) absorbed by a load from a voltage or current source to the apparent power (the product of RMS voltage appearing across the load and the RMS current flowing in it).

$$PF = \frac{\frac{1}{T}\int_0^T vi\,dt}{\sqrt{\frac{1}{T}\int_0^T v^2\,dt \times \frac{1}{T}\int_0^T i^2\,dt}} \qquad (1)$$

It must be emphasized that this definition is valid for any arbitrary load-and-source combination and includes sinusoidal-voltage sources feeding linear loads. In the special case of linear loads (consisting of linear resistors, capacitors, and inductors) driven by a sinusoidal source, the PF is numerically equal to the cosine of the angle between the load voltage and the current phase:

$$PF = \cos(\Phi) \qquad (2)$$

The PF resulting from an other-than-zero phase angle between the voltage and current is called displacement PF. From Equation (2), it follows that a linear resistor load will have unity PF, and linear capacitors and inductors will have a PF of zero.

Nonlinear loads will absorb nonsinusoidal current from a sinusoidal voltage source, and because only the fundamental component of the current that is in phase with the source voltage delivers power to the load, the product of the RMS voltage and current will always be larger than the average power absorbed, resulting in a PF of less than unity.

III. COMPARISON OF THE APPLICABLE STANDARDS

EN61000-3-2 and Energy Star® are most frequently mentioned standards that regulate the quality of the current drawn by loads connected to the utility lines. However, these two standards focus on different aspects of the current quality. EN61000-3-2 limits the harmonic content of current. Presumably, these limitations are driven by the harmful effect of harmonics on various

Energy Star is a registered trademark of the Environmental Protection Agency.

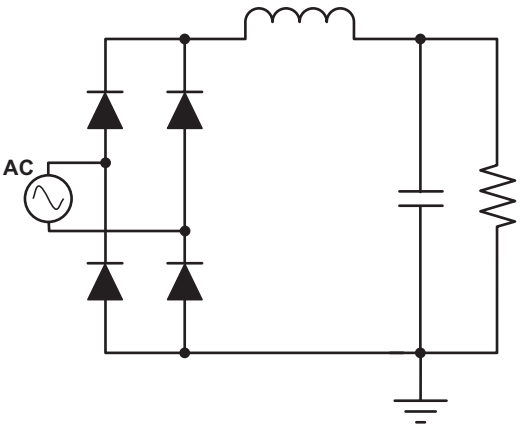
elements of the power-distribution system (the build up of triplen harmonics in the neutral wire being one significant concern).

On the other hand, Energy Star requires power supplies with greater than or equal to 100-W input power must have a true power factor of 0.9 or greater at 100% of rated load when tested at 115 V at 60 Hz. Universal-input power supplies will have to comply to both standards. It is interesting to examine the relationship between these two standards: Is one standard stricter than the other one? Does a power supply passing one standard automatically qualify for the other one?

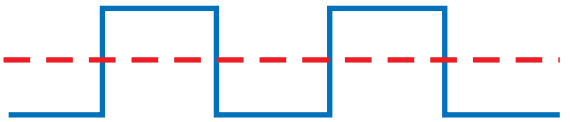
First we will calculate the power factor associated with an input current that has a harmonic content equal to the maximum permitted by EN61000-3-2, class D (most power supplies of interest fall into this category). According the power-factor definition, the power factor is determined by both the displacement (cos(Φ)) and distortions (ratio of the fundamental to RMS of the input current). Generally, displacement of the input current is caused by the net reactive current of the EMI filter. At full-load condition, the effect of the filter's net reactive current is negligible, so the power factor reduces to:

$$PF = \frac{I_1}{\sqrt{\sum_{n=1,3}^{39} I_n^2}} = \frac{\frac{P}{230\ V}}{\sqrt{\left(\frac{P}{230\ V}\right)^2 + \sum_{n=3,5}^{39} I_n^2}} = 0.726 \quad (3)$$

This value is significantly lower than the Energy Star 0.9 power-factor requirement, so a circuit that just meets EN61000-3-2 will fail Energy Star. Conversely, a power supply may be designed to absorb a square wave of current from the line to meet the Energy Star requirement by emulating an inductive-input filter with a large inductance value (see Fig. 1). The square-wave current shown yields a power factor >0.9 and meets the Energy Star requirement. However, the spectral analysis shows that all harmonics above the 11th exceeds the EN61000-3-2 limits. From the above it may appear that a potential problem is looming, but, fortuitously, all the commonly used active-PFC circuits draw input-current waveforms that can easily comply to both standards.



a. Rectifier with 0.9 power factor.



b. Input current waveform

Fig. 1. Current waveform with PF = 0.9.

IV. Benefits of Active PFC

The following benefits can result from PFC:

- Reduces RMS input current. For instance, a power circuit with a 115-V/12.5-A rating is limited to about 719 W of available power with a PF of 0.5. Increasing the PF to 0.9 will double the deliverable power to 1294 W, allowing higher-power devices to be operated.
- Facilitates power-supply holdup. The active PFC circuit maintains a fixed intermediate DC bus voltage that is independent of the input voltage, so the energy stored in the system does not decrease as the input voltage decreases. This allows use of smaller, less expensive bulk capacitors.
- Enables universal input voltage capability by providing a constant 400-V bus voltage for the entire 85- to 265-VAC voltage range.
- Improves efficiency of downstream converters. PFC reduces the dynamic voltage range applied to the downstream DC/DC converters. As a result, voltage ratings of rectifiers can be reduced, resulting in lower forward drops; and operating duty-cycle/transformer turns ratios can be increased, resulting in lower current in switches and windings.

- Increases the efficiency of the power-distribution system. Lower RMS current reduces distribution wiring losses. See Appendix for details.
- Reduces the VA rating of standby power generators.
- Reduces stresses on neutral conductors. Reducing harmonics eliminates the risk of triplen harmonics (the third and multiples thereof) that can add up to dangerous levels in the neutral conductor of Y-connected 3-phase systems.

V. Effect of Active PFC on Power-Supply Efficiency

It follows from the above benefits that having active PFC at power levels above 75 W are self-evident. At the same time, we should remember that the PFC stage is an additional power-processing stage that inevitably adds losses to the system. It is instructive to quantify these losses in order to develop ways to minimize them.

Because the typical PFC stage is a boost converter, the converter has to boost the instantaneous line-input voltage to a value equal to the output voltage in order to transfer power from the line-input voltage to the output. Note that if the input voltage is equal to the output voltage, the converter does not have to process any power since power can pass directly from the input to the output. Under this condition, the losses are only caused by the DC drops on the output rectifier. These losses will add to less than 1% of the output power. Consequently, the power processed by the boost converter at any given moment is a function of the difference between the input and output voltages; the higher the difference, the more power the converter has to process and when more power is processed, more power is dissipated. This means that the difference between the input and output voltages of the PFC stage affects both the efficiency of the stage and the ratings of its components. The following analysis quantifies this effect.

To facilitate the analysis, we could visualize a converter model (referred to as "the ΔV converter") that is fed from the rectified line voltage and has a floating output connected in series with the rectified line voltage. By controlling the output voltage of the ΔV converter so it is equal to the difference between the momentary line voltage and the required output voltage of the PFC, we obtain a system that is equivalent to the boost converter. The ΔV converter processes only the power transferred indirectly to the output, so the model allows separation between the power transmitted directly to the output (with nearly 100% efficiency) and the power processed by the PFC converter. By assuming a practically achievable efficiency for the ΔV converter, we can estimate the efficiency of an equivalent boost PFC stage under various operating conditions.

The proposed model is not just a theoretical abstraction. As shown in Fig. 2, connecting the output of a flyback converter in series with its input yields a system equivalent to a boost converter.

The DC transfer function of the ΔV flyback converter can be calculated as follows:

$$\Delta V = V_{in} \times \frac{D}{1-D} \tag{4}$$

$$V_{out} = V_{in} + \Delta V \tag{5}$$

$$V_{out} = V_{in} + V_{in} \times \frac{D}{1-D} \tag{6}$$

$$V_{out} = \frac{V_{in}}{1-D} \tag{7}$$

Equation 7 is exactly the DC transfer function of a boost converter.

For the purpose of the analysis, we will define a boost factor (BF) as the ratio of the boost-converter output voltage to the peak value of the

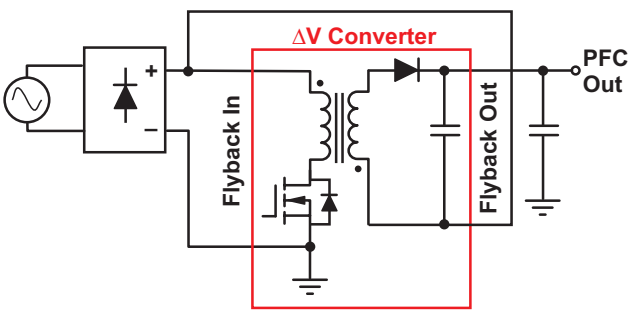


Fig. 2. Simplified block diagram of a flyback ΔV converter.

input voltage. The BF is a measure of the amount of boosting that the PFC stage has to perform as a function of the line-input voltage.

$$BF = \frac{V_{out}}{V_{in(pk)}} \tag{8}$$

Now we will examine how the variation of the BF affects the efficiency of the PFC stage. Normalizing the average input power and RMS input voltage to unity, and the output voltage of the PFC to the square root of 2 (equal to the peak of the input voltage), we have

$$P_{in(ave)} = 1 \tag{9}$$

and

$$V_{out} = \sqrt{2}. \tag{10}$$

The instantaneous value of the input power is given by

$$P_{in(\omega t)} = 2 \times \sin^2(\omega t), \tag{11}$$

where ω is the angular velocity, 2πf, of the line voltage, and t is the time. The instantaneous value of the input voltage is given by

$$V_{in} = \frac{V_{out}}{BF} \times \left|\sin(\omega t)\right|. \tag{12}$$

For the interval $0 < \omega t < \pi$, the output voltage of the ΔV converter will be

$$\Delta V = V_{out} - V_{in}. \tag{13}$$

Substituting Equations (11) and (2) into Equation (13) yields

$$\Delta V = \sqrt{2} - \frac{\sqrt{2}}{BF} \times \left|\sin(\omega t)\right|. \tag{14}$$

Since the converter efficiency is high, the output power is nearly equal to the input power:

$$P_{out(ave)} = P_{in(ave)} \tag{15}$$

The output current of the ΔV converter stage is also equal to the output current of the entire PFC stage and is given by

$$I_{out} = \frac{P_{in}}{V_{out}} \tag{16}$$

and

$$I_{out} = \frac{2 \times \sin^2(\omega t)}{\sqrt{2}}. \tag{17}$$

The output power of the ΔV converter is the product of Equations (14) and (17):

$$P_{\Delta V} = \left(\sqrt{2} - \frac{\sqrt{2}}{BF} \times \left|\sin(\omega t)\right| \right) \times \frac{2 \times \sin^2(\omega t)}{\sqrt{2}} \tag{18}$$

Let's compare the peak and average power ratings of the ΔV converter for two practical cases: one with a single input-voltage range of 187 to 265 VAC, and one with a universal input-voltage range of 85 to 265 VAC. Both cases assume the PFC output voltage is peak value of 265 VAC. In the first case,

$$BF = \frac{265 \times \sqrt{2}}{187 \times \sqrt{2}} = 1.417.$$

In the second case,

$$BF = \frac{265 \times \sqrt{2}}{85 \times \sqrt{2}} = 3.118.$$

The peak power (normalized) of the ΔV converter occurs at $\omega t = \pi/2$ for BFs of 3.118 and 1.417, and at $\pi/4$ for a BF of 1 (see Fig. 3):

$$P_{\Delta V}\left(\omega t = \frac{\pi}{2},\ BF = 3.118 \right) = 1.359 \tag{19}$$

$$P_{\Delta V}\left(\omega t = \frac{\pi}{2},\ BF = 1.417 \right) = 0.589 \tag{20}$$

$$P_{\Delta V}\left(\omega t = \frac{\pi}{4},\ BF = 1 \right) = 0.293 \tag{21}$$

The average power (normalized) that the ΔV converter can deliver is a function of the BF and is obtained by averaging Equation (18) over a half cycle of the line-input voltage:

$$P_{\Delta V(ave)} = \frac{1}{\pi} \times \int_0^{\pi} P_{\Delta V} d\omega t \tag{22}$$

$$P_{\Delta V(ave)} = \frac{1}{\pi} \times \int_0^{\pi} \left[V_{out} - \frac{V_{out}}{BF} \times \left|\sin(\omega t)\right| \right] \times \frac{2 \times \sin^2(\omega t)}{\sqrt{2}} d(\omega t) \tag{23}$$

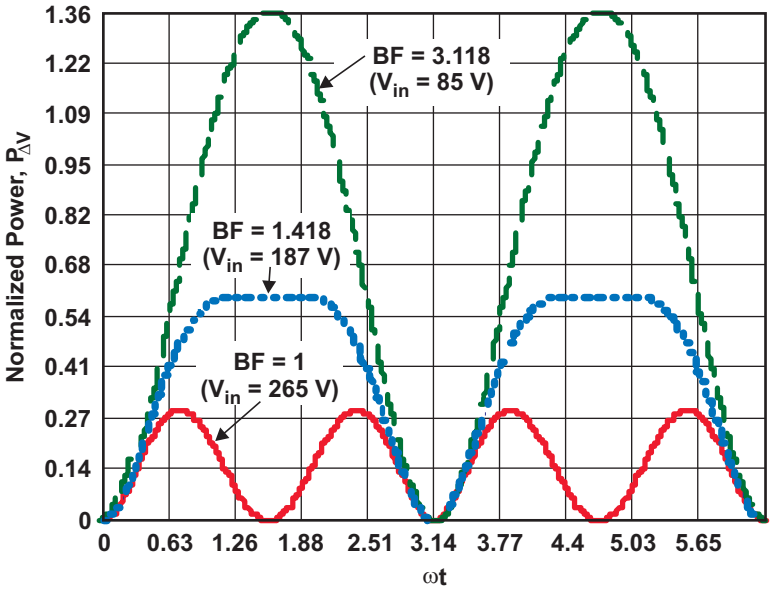


Fig. 3. Points where peak power occurs.

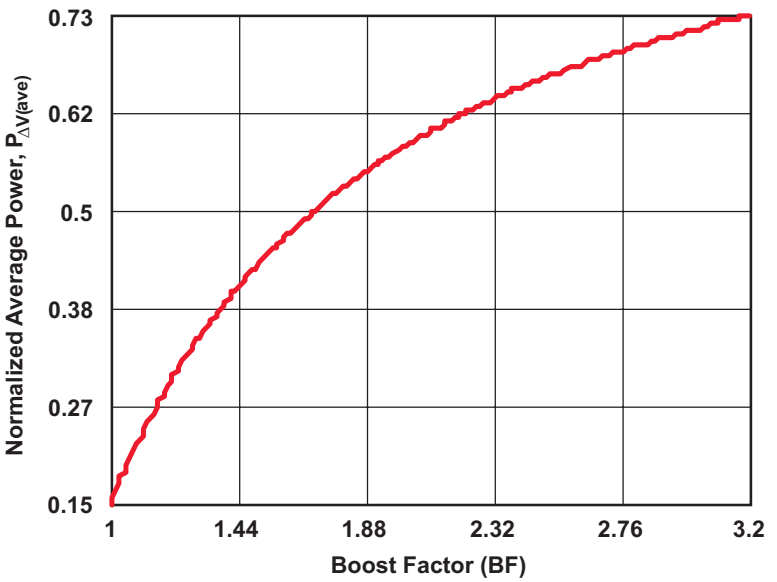


Fig. 4. Plot of average input power for a ΔV converter.

Figs. 3 and 4 illustrate the impact of the BF on the peak and average power ratings of the ΔV converter (the case of unity BF is also added for completeness). At a BF of unity, the ΔV converter has to handle an average of only 15% and a peak of 29% of the output power, increasing to 40% and 59% for a BF of 1.417, or 73% and 136% for a BF of 3.118. These figures provide an insight to the effect that a high BF has on the size and cost of the PFC converter. A converter designed for universal input voltage (BF = 3.118) will be rated to a peak power that is 2.3 times higher than the power of a converter designed for an input range of only 187- to 265-VAC input (BF = 1.417).

In the proposed model, all the losses are generated by the ΔV converter. For a ΔV converter's efficiency of η_Δ = 90% (a reasonable value for a flyback converter), the average losses will be

$$P_{loss} = \frac{P_{\Delta V(ave)}}{\eta_\Delta} - P_{\Delta V(ave)}. \qquad (24)$$

Since a good portion of the power goes directly to the output, the PFC-stage efficiency will be

$$\eta = 1 - P_{loss}. \qquad (25)$$

Fig. 5 illustrates the effect of the BF on PFC efficiency. An efficiency of 98.3% for a BF of unity decreases to 91.9% for a BF of 3.118 (with a universal input-voltage range). In addition, we assumed a constant 90% efficiency for the ΔV converter, when in reality the efficiency is even lower at higher BFs. The primary contributors to a decrease in efficiency are: the resistance of the windings, the $R_{DS(on)}$ of the MOSFETs. These factors all represent power losses that can increase with higher temperatures caused by the higher power dissipation.

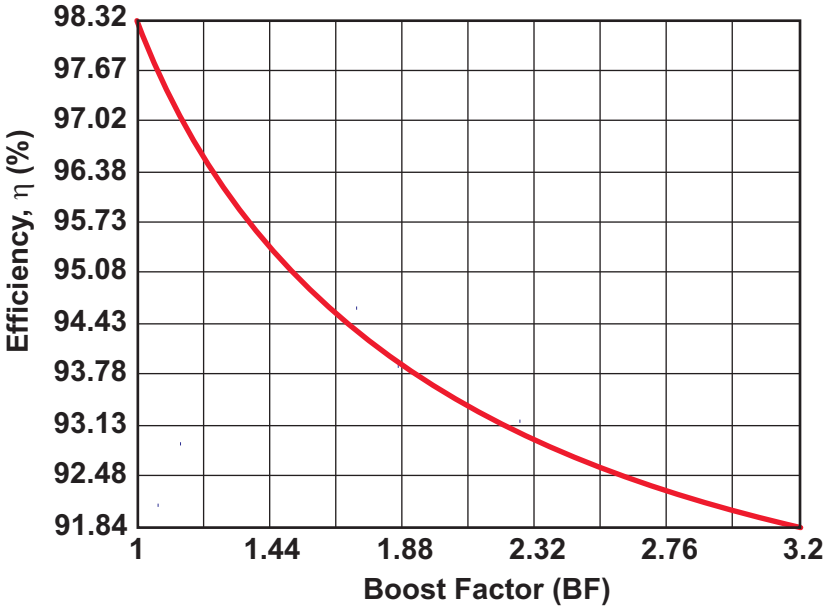


Fig. 5. PFC efficiency versus BF for a ΔV converter.

This analysis suggests that a converter's ability to handle a wide input-voltage range (a high BF) has significant penalties, while a low BF improves not only the efficiency but also the cost and/or power density of the system (the components of the boost converter have to be rated for only a relatively small percentage of the output power). For these reasons, a boost follower concept has been proposed in the literature. A boost follower is a boost converter that produces a variable output voltage that is only slightly higher than the peak value of the input voltage. Consequently, the BF is near unity over the full range of the input voltage, and the efficiency of the PFC stage is maximized.

A boost follower can be easily implemented using any standard PFC control IC. An application circuit using the Texas Instruments (TI) UCC3817 PFC controller [1] is shown in Fig. 6. The output voltage of the boost follower at different line

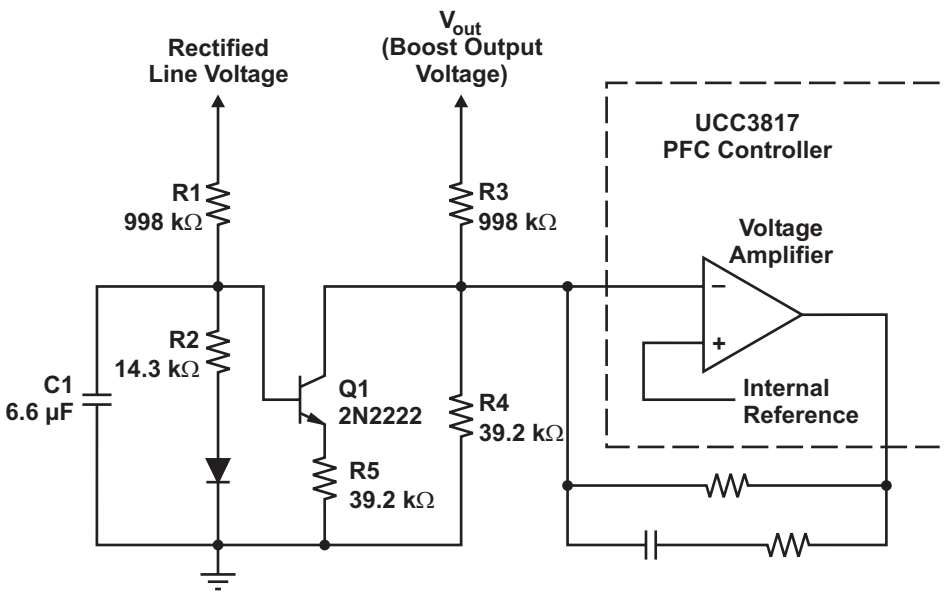
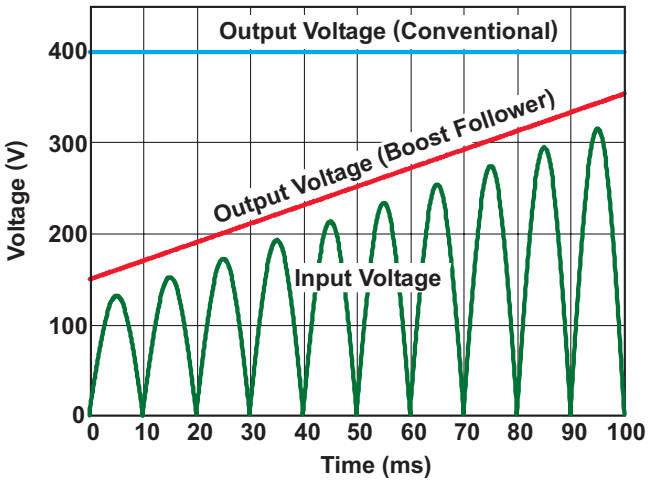
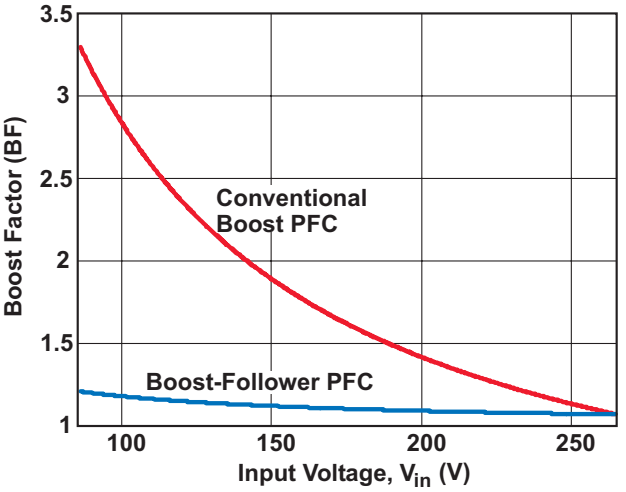


Fig. 6. Application circuit to implement boost follower.



a. Output voltage at different line voltages.



b. BF at different line voltages.

Fig. 7. Boost follower operation over a range of line voltages.

voltages is shown in Fig. 7a. With this data, BFs at different line voltages can be calculated and are shown in Fig. 7b. Because the output voltage is much closer to the input voltage, the BF of the boost follower is only 1.2 at an 85-V input. The reduced BF leads to efficiency improvement for all the line voltages.

Unfortunately, the boost follower solution is beneficial only if the dynamic range of the AC input voltage is relatively low and there is little or no requirement for holdup. If the AC line voltage varies widely (universal input voltage), the voltage applied to the downstream converter will vary from approximately 120 to 375 VDC. This large variation will force compromises in the design of the converter that will result in significant degradation of the system efficiency.

The larger input-voltage range will impose a lower transformer turns ratio and reflect a higher current to the primary circuit, increasing the RMS current in the primary windings and switching transistors as well as generating higher differential-mode EMI. The low transformer turns ratio causes an increase in the voltage-blocking requirements of the secondary rectifiers; and the higher voltage rating will result in higher conduction drop (or higher $R_{DS(on)}$ in the case of synchronous rectifiers) and poorer reverse-recovery performance. In addition, the increased secondary voltage will require a larger filter inductance, resulting in higher losses in the output inductor. Since the energy stored in the PFC capacitor at low input voltages will be low, very large capacitance will be required to support the output voltage for the customary 10- to 20-ms holdup time required in many applications. All in all, the power dissipation increase in the downstream converter may equal or exceed the power savings provided by the increased efficiency of the boost follower.

A. Universal Input: Is it a Must?

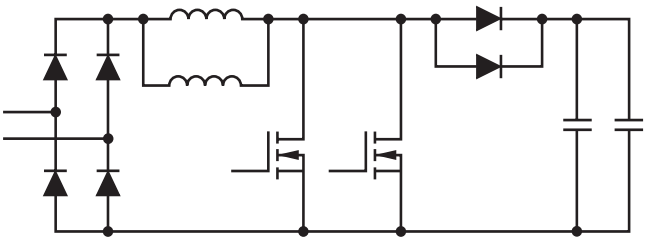
Considering the significant impact that a wide input-voltage range has on the cost and efficiency of the PFC converter's front end, it is important to look at the benefits and penalties associated with universal input-voltage designs.

While portable products must operate with universal input voltages, other products will always be operated at a local-power voltage of 100 V, 115 V, or 230 VAC. For instance, TV receivers are designed for regional use and are operated throughout their entire service life from a single line voltage of 100 V for Japan and the U.S., and of 230 V for the European Union and other countries. When these products are designed for universal input voltage, the efficiency will be several percentage points lower when operated at the 100-V input range. Consequently, in addition to the loss of power, costs will be incurred for more expensive components and/or extra thermal management that are not necessary if the equipment is operated at the 100-V input range. As previously shown, separate designs for 100 V and 230 V will

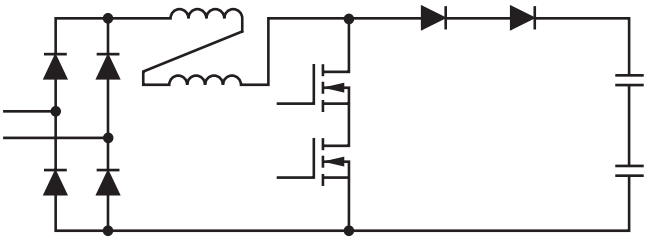
yield nearly equal efficiencies when operated with nearly the same BFs. (The 100-V design will have an intermediate 200-VDC bus, and the 230-V design will have a 400-VDC bus.)

Although separate designs for local voltage will yield higher efficiency, better power density, and lower cost, they have one major disadvantage—different bills of material not only for the PFC stage but also for the downstream converters, which will have to be designed for different voltages. This disadvantage may overshadow the benefits and is probably the major reason why virtually all applications are designed for universal input voltage.

With efficiency becoming an ever more critical parameter, a different approach may be considered: a PFC converter whose internal connections between the components are configured on the assembly line so that the BF is roughly the same for both high and low input-voltage ranges.



a. Configuration for low line-input voltage.



b. Configuration for high line-input voltage.

Fig. 8. Ideal configurable PFC converter.

B. Ideal Configurable PFC Converter

An ideal configurable PFC converters is shown in Fig. 8. If the devices are configured in parallel as shown in Fig. 8a, a low line-input voltage will generate a 200-V output. If these devices are reconfigured in series as shown in Fig. 8b, a high line-input voltage will generate a 400-V output. Fig. 9 compares the BF of these converters with that of a conventional boost PFC converter. The BF is reduced to half at low line-input voltages, which significantly improves efficiency.

In the ideal configurable PFC circuit, all the components are active, operating at both high and low line-input voltages, which maximizes their utilization and lowers design cost. However, because there are different output voltages at different input lines, the downstream DC/DC converter has to be configurable as well. Otherwise, the configurable PFC converter only moves the design stress from the PFC stage to the downstream DC/DC stage instead of really solving the problem. One simple example of configuring a downstream DC/DC converter is to use a full bridge at the 200-V PFC output and a half bridge at the 400-V PFC output. Because of the inherent doubling effect that occurs when the topology changes from full-bridge to half-bridge, the transformer and secondary-side designs can stay the same. Nevertheless, using a configurable converter in both the PFC and the DC/DC stage is complicated compared with the original design and may not be attractive enough for commercial applications.

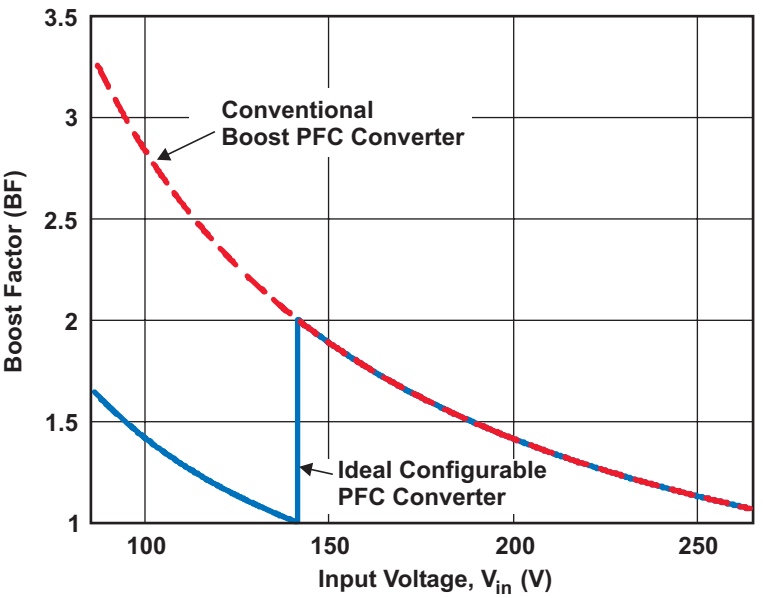


Fig. 9. BF for boost PFC and ideal configurable PFC converters.

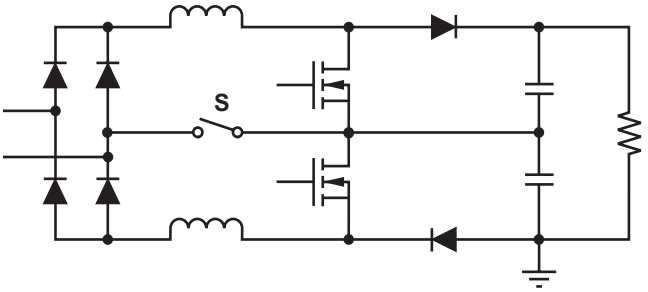


Fig. 10. Configurable three-level boost converter.

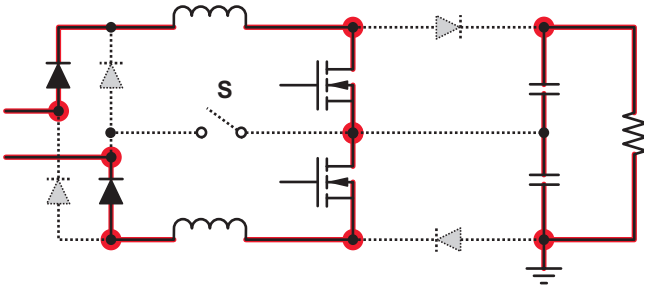
C. Configurable Three-Level PFC Converter

A more practical solution, a configurable three-level PFC converter (also know as a three-level converter), uses the same PFC-stage components as the ideal configurable PFC converter, but it uses jumpers to implement different topologies for high and low line-input voltages. Because of the reconfigurable structure, the output-bus voltage does not change, and the DC/DC stage is not affected.

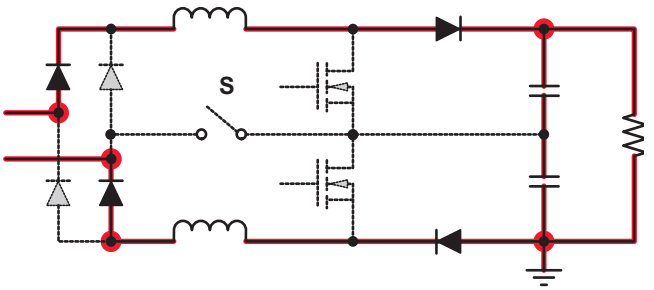
A configurable three-level boost converter is shown in Fig. 10, with two boost converters in series to generate the output voltage. Because of the three-level structure, the voltage stresses on the MOSFETs and diodes are only half of the output voltage, so low-voltage devices can be used to achieve better performance [2].

At high line-input voltages, the range switch, S, is open (see Fig. 11). The whole converter operates as a single boost converter with an output voltage of 400 V. It has two MOSFETs in series and two diodes in series, all of which increases the conduction loss. However, at high line-input voltages, the boost PFC converter is highly efficient because of the low current stress and the lower BF. The increased conduction loss still results in very high efficiency.

At low line-input voltages, the range switch, S, is closed to construct a voltage doubler. On each half cycle of the line-input voltage, only one boost converter is operating, as shown in Fig. 12, generating 200 V on one of the two series-connected output capacitors. The other boost converter operates during the subsequent line half cycle, generating 200 V on the other output capacitor. The output voltage of the PFC stage is the sum of the voltages on the two capacitors, i.e. 400 V. The reduced voltage delivered by each

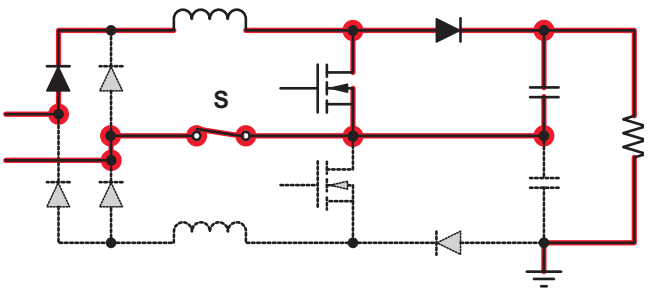


a. Charging inductor.

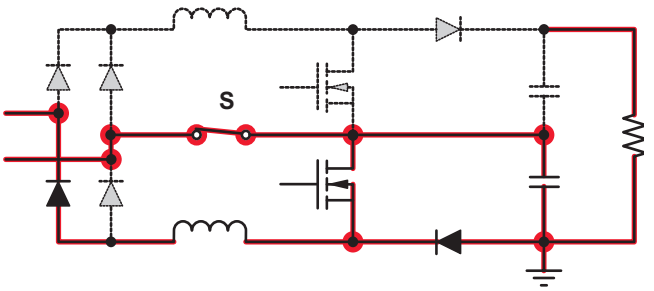


b. Discharging inductor.

Fig. 11. Equivalent circuit with high line-input voltage.



a. Positive half cycle.



b. Negative half cycle.

Fig. 12. Equivalent circuit with low line-input voltage.

converter greatly reduces the duty cycle and also reduces conduction loss, switching loss, and diode reverse-recovery loss. Since each MOSFET and diode see only half of the output voltage, low-voltage devices can be used to easily achieve better conduction loss and switching loss and further increase the overall system efficiency.

Since the configurable three-level PFC converter has a 200-V output voltage for each converter at low line-input voltages and 400 V at high line-input voltages, it has the same BF as the ideal configurable PFC circuit. The reduced BF helps to improve the PFC-stage efficiency at low line-input voltages.

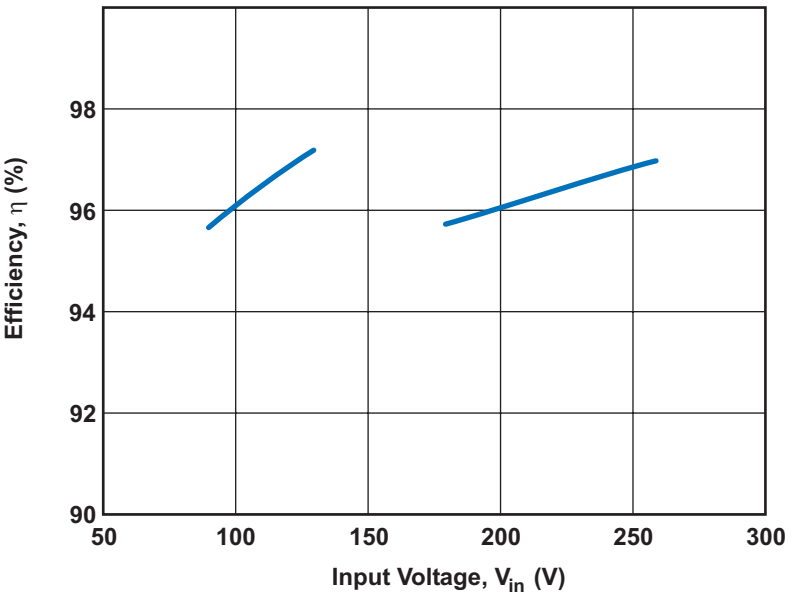


Fig. 13. Efficiency of configurable three-level PFC converter.

Another major source of efficiency loss is the input diode bridge. The voltage drop on the diode bridge stays relatively constant regardless of the level of current flowing through it. For a conventional boost PFC converter, there are two diodes in the diode bridge conducting current at any time. The total voltage drop on those two diodes is about 2 V. At a high line-input voltage of 220 V, this 2-V drop causes a less than 1% drop in efficiency. However, at a low line-input voltage of 100 V, the same 2-V drop causes a 2.2% drop in efficiency. Efficiency can drop even further when the input voltage is lower.

In a configurable three-level PFC converter at low line-input voltages, the voltage-doubler structure has only one diode of the diode bridge in the conduction path. This removes a diode voltage drop of 1 V, which can be easily translated into a 1% increase in efficiency with a 100-V input.

An efficiency plot combining all the benefits of the configurable three-level PFC converter is shown in Fig. 13. At a high line-input voltage, the efficiency is about the same as with a conventional boost PFC converter; but at a low line-input voltage, the efficiency improves dramatically.

Although this configurable three-level PFC converter improves overall system efficiency, it also presents many challenges.

The three-level structure requires a high-side driver. if a drive transformer is to be used, the maximum duty cycle may have to be limited to perhaps 80%. An integrated half-bridge driver IC could simplify the driver design but would increase the overall system cost as compared to the simple driver of a conventional PFC circuit. Besides, to simplify the driving scheme, the control ground would have to be set at the source of the bottom switch. Because of the boost diode, the output voltage is not directly connected to the control ground, and isolation would be required for the voltage-feedback loop.

Voltage balancing on the output capacitors is another concern. For series capacitors, voltage balancing is determined by the capacitance tolerances and the leakage difference. However, in a configurable three-level PFC converter at a high line-input voltage, both MOSFETs turn on and off at the same time. A slight difference in the switching speed will cause current to flow through the middle point, where two capacitors are in series together. Voltage balancing can be realized by placing an equalizing resistor parallel to each capacitor, which causes extra loss, or by adding a dedicated control loop to slightly adjust the ON time of each MOSFET.

The designer using a configurable three-level PFC converter also faces the difficulty of implementing current sensing. Although using four current transformers can reconstruct the inductor current, the system implementation becomes much more complicated.

Furthermore, at low line-input voltages, only one of the boost converters is operating during

each line half cycle, which means that component utilization is not optimal at this operation mode. As the demand for higher efficiency increases, a point may be reached where the potential efficiency improvement may justify the effort and expense associated with the solution of these problems.

D. The Buck PFC

It is interesting to note that a buck converter can also be used to shape the input current and provide power-factor correction. Since the output voltage of a buck converter can only be equal to or lower than its input voltage, the buck PFC, as shown in Fig. 14, will draw current from the input during only a fraction of line-voltage cycle, leading to the buck's incapability to yield very low harmonic distortions or correct the PF to close to unity. Nevertheless, as it will be shown below, the buck PFC can be a valuable circuit in some applications.

A quantitative analysis of the buck-PFC efficiency is outside the scope of this topic, but it is intuitively clear that the efficiency will be higher at lower input voltages where the switching and inductor losses will be lower.

Similarly to the boost-PFC case, a buck factor can be defined as:

$$\text{Buck Factor} = \frac{V_{in}}{V_{out}} \qquad (26)$$

Decreasing the buck factor (i.e. increasing the output voltage of the buck PFC for a given voltage) improves the efficiency, but, at the same time, decreases the input-current conduction angle that causes a deterioration of both the PF and the harmonic distortion. Increasing the buck Factor improves PFC and harmonic distortions, but reduces efficiency. Also, reducing the output voltage reduces the energy storage capability of the PFC output capacitors. At the correct balance between these parameters, the buck PFC becomes an effective solution for meeting the Energy Star efficiency goals when converters are intended for universal voltage. For instance, if the PFC output voltage is set to 80 V, the buck factor at 115 VAC will be 2 and the conduction angle will be approximately 120° (see Fig. 15). The result is a PF of 0.97 (well above the Energy Star minimum) and a THD of 24.7%.

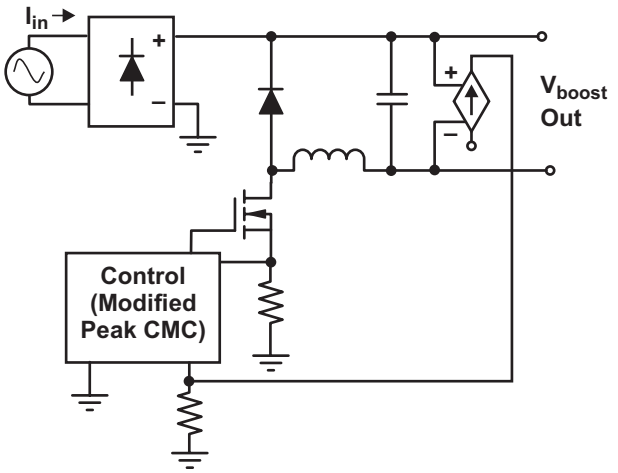
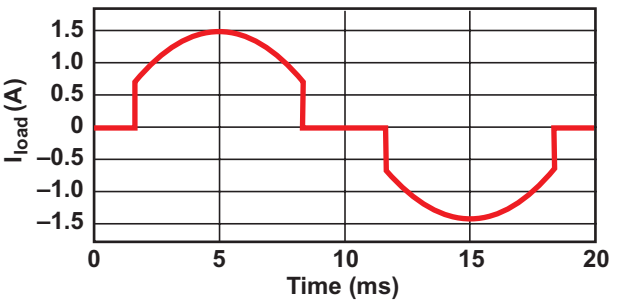
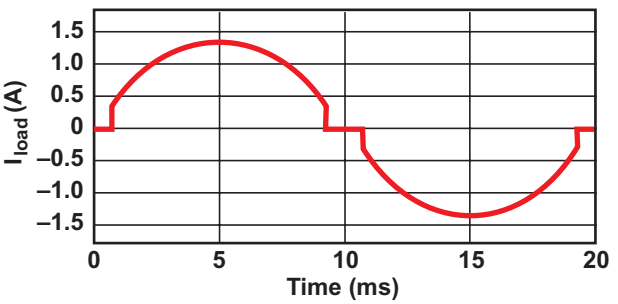


Fig. 14. Buck PFC.



a. Buck factor = 2.



b. Buck factor = 4.

Fig. 15. Buck PFC normalized input current.

As the input voltage increases to 260 V, the buck factor will increase to 4 and both the PF and THD will improve, reaching 0.997 and 7.3% respectively. The spectral analysis of the current waveform shows that all harmonics are just a fraction of the maximum allowed by EN61000-3-2.

Although a buck-PFC output voltage has an adverse effect on energy-storage and holdup capability, there are applications, such as laptop AC adapters, where the holdup requirements are minimal and an 80-V bus voltage allows use of

100-V MOSFETs in the second-stage converter. These MOSFETs are inexpensive with extremely low drain-to-source capacitance and low $R_{DS(on)}$, which results in a highly-efficient, cost-effective power train.

The increased low-line efficiency of the buck converter balances the increase of losses in the EMI filter and input rectifier. Fig. 16 shows the full-load efficiency of the 80-V buck PFC stage used in a high-performance, 90-W laptop adapter. In this design, the efficiency exceeds 96% over the full 90- to 270-V input-voltage range.

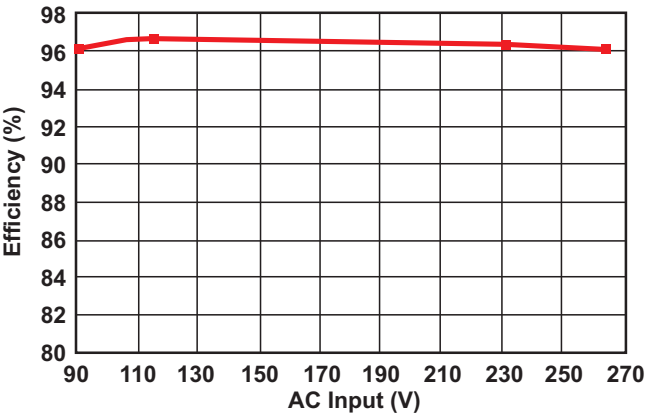


Fig. 16. Efficiency of a 80-V, 90-W buck PFC stage as a function of the AC input voltage.

VI. Conclusion

Active PFC can improve the efficiency of AC-to-DC conversion. The improvement may be curtailed and the PFC-stage size and cost will be adversely affected if the system is designed to accommodate a wide range of input voltages. These problems may be mitigated by the use of different PFC circuits that reduce the BF and minimize the power processed by the PFC stage.

VII. References

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APPENDIX: EFFECT OF PFC ON POWER-DISTRIBUTION LOSSES

Because increasing the power factor (PF) reduces the RMS input current drawn by a load, it should be expected that a low PF will increase the conduction losses in the transmission and distribution wiring that connects the load to the power station. This appendix presents a simplified correlation to the PF for loads, load currents, power losses, and system efficiency.

We first assume that the total load-related transmission power loss at a PF of unity is 5%. With the variables normalized such that $P_{load} = V_{load} = I_{load} = 1$ at PF = 1, and where P_{d1} is the wiring power loss at PF = 1 and R_w is the wiring resistance, the following equations show the basic relationship between the PF and the primary system variables:

$$P_{d1} = 0.05$$
$$P_{d1} = I_{load}^2 \times R_w \quad (27)$$
$$P_{d1} = R_w$$

The load current as a function of the PF is

$$I_{load} = \frac{1}{PF}. \quad (28)$$

The generalized wiring power loss, P_w, as a function of the PF is

$$P_d = P_{w1} \times I_{load}^2$$

and (29)

$$P_d = P_{d1} \times \left(\frac{1}{PF}\right)^2.$$

The system efficiency as a function of the PF is

$$\eta_{d(PF)} = \frac{1}{1+P_d}. \quad (30)$$

The losses in the PFC circuit will degrade the improvement in the distribution efficiency if the efficiency of the PFC circuit is low, so correcting the PF may actually decrease rather than increase the overall system efficiency. For instance, if we assume a PF of 0.7 for a supply without PFC, the system efficiency will be

$$\eta_{d(0.7)} = 0.907. \quad (31)$$

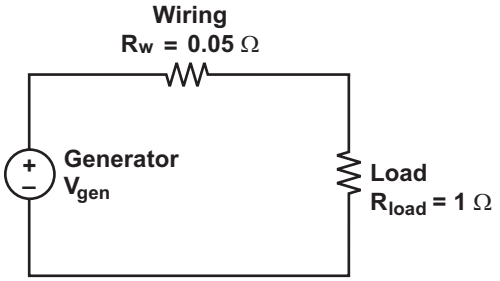

Fig. 17. Simplified equivalent circuit of a power-distribution system.

If the PF is corrected to unity, the distribution efficiency will be

$$\eta_d(1) = 0.952. \quad (32)$$

The overall system efficiency, η_{do}, including the distribution and the PFC efficiency, η_{PFC}, will be as follows:

$$\eta_{do} = \eta_d(1) \times \eta_{PFC} \quad (34)$$

Note that if the PFC-stage efficiency, η_{PFC}, is equal to 0.953, correcting the power factor will not provide any efficiency enhancement.

$$\eta_{do} = 0.953 \times 0.952 = 0.907$$

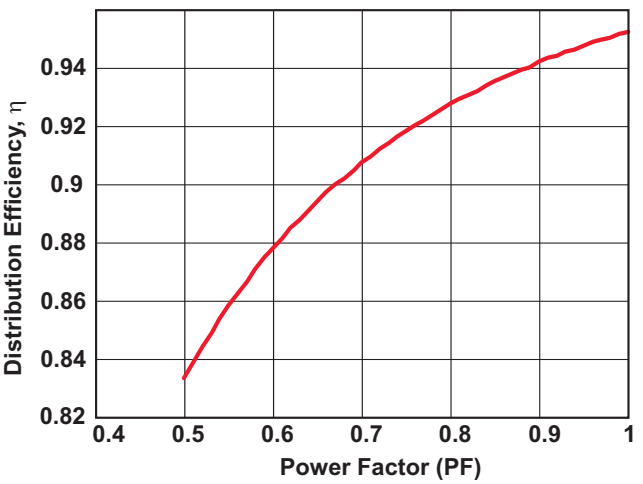

Fig. 18. Effect of the power factor on power-distribution efficiency.