Using Integrated Analog with the MSP430
Mike Mitchell

Agenda

- ADC12
- ADC10
- Oversampling
- SD16 (_A)
- DAC12
- OA
ADC12

- 200ksps+
- Single Sequence
  Repeat-single
  Repeat-sequence
- Int/ext reference
- TA/TB SOC triggers
- Configuration memory/buffer
- DMA enabled

Timer Triggers - Accuracy

Automatic SOC trigger eliminates phase error
Timer Triggers – Low-Power

// Interrupt CPU cycles
; MSP430 ISR to start conversion
BIS #ADC12SC,&ADC12CTL0 ; Start conversion
RETI ; Return

ADC12 Reference Decoupling

- Power Supply
- Any used VRef

Any used reference must be decoupled with > 5uf
ADC12 Reference - No Decoupling

3mA surge

200µA for 2 LSBs

ADC12 Reference - Settling

- ADC12 Reference Settling Time:

| REF/OUT | Settling time of internal reference voltage (see figure 38 and Note 2) | | | 17 ms |
|---------|---------------------------------------------------------------------|------------------|----------|
| VREF+ = 0.5 mV, CREF+ = 10 µF, VREF- = 1.5 V, VADC = 2.2 V | |

- Use timer trigger for ULP periodic measurements:

Initialize System

Timer_A ISR

REF/ADC On
Clear TAIFG

LPM3

ADC12 ISR

Read ADC Value
REF + ADC Off
Timer Trigger for Reference Settling

TA ISR: Ref/ADC on
TACCR1: output triggers ADC
ADC12 ISR: Read Value, Ref/ADC Off

Active Mode

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DMA
- Edge/level triggers
- Single Block Burst-block
- Byte/word or mixed transfer
- Requires two MCLK cycles

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Why Is DMA Important?

Why Is DMA Important?

// Interrupt
; ADC12 ISR
MOV &ADC12MEMx,LOCx ; Move one value
RETI ; Return

<table>
<thead>
<tr>
<th>CPU cycles</th>
<th>DMA clocks</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>17</td>
<td>2</td>
</tr>
</tbody>
</table>

ADC12 ENOB Vs. Frequency

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Effective Number of Bits vs Input Frequency

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MSP430 Advanced Technical Conference
Real World Low Voltage Performance

• Three devices from different lots tested on bench:

<table>
<thead>
<tr>
<th>Vcc</th>
<th>.5V Input</th>
<th>1V Input</th>
<th>1.25V Input</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Dev. 1</td>
<td>Dev. 2</td>
<td>Dev. 3</td>
</tr>
<tr>
<td>3</td>
<td>1364</td>
<td>1406</td>
<td>1387</td>
</tr>
<tr>
<td>2.5</td>
<td>1368</td>
<td>1407</td>
<td>1390</td>
</tr>
<tr>
<td>1.8</td>
<td>1369</td>
<td>1411</td>
<td>1390</td>
</tr>
<tr>
<td>1.7</td>
<td>1367</td>
<td>1413</td>
<td>1395</td>
</tr>
<tr>
<td>1.6</td>
<td>1367</td>
<td>1412</td>
<td>1397</td>
</tr>
</tbody>
</table>

< .5% degradation for low voltage operation
New Calibration Values – TLV

• Newer MSP430’s have extra calibration values:

<table>
<thead>
<tr>
<th>LABEL</th>
<th>CONDITION AT CALIBRATION</th>
<th>DESCRIPTION</th>
<th>SIZE</th>
<th>ADDRESS OFFSET</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAL_ADC_25T85</td>
<td>INCHs = 0x1010; REF2.5 = 1; Tss = 85°C</td>
<td>word</td>
<td>0x000E</td>
<td></td>
</tr>
<tr>
<td>CAL_ADC_25T90</td>
<td>INCHs = 0x1010; REF2.5 = 1; Tss = 90°C</td>
<td>word</td>
<td>0x000C</td>
<td></td>
</tr>
<tr>
<td>CAL_ADC_25VREF_FACTOR</td>
<td>REF2.5 = 1; Tss = 30°C; I_VREF = 1.0 mA</td>
<td>word</td>
<td>0x000A</td>
<td></td>
</tr>
<tr>
<td>CAL_ADC_15T85</td>
<td>INCHs = 0x1010; REF1.5 = 0; Tss = 85°C</td>
<td>word</td>
<td>0x0368</td>
<td></td>
</tr>
<tr>
<td>CAL_ADC_15T90</td>
<td>INCHs = 0x1010; REF1.5 = 0; Tss = 90°C</td>
<td>word</td>
<td>0x0366</td>
<td></td>
</tr>
<tr>
<td>CAL_ADC_15VREF_FACTOR</td>
<td>REF1.5 = 0; Tss = 30°C; I_VREF = 0.5 mA</td>
<td>word</td>
<td>0x0364</td>
<td></td>
</tr>
<tr>
<td>CAL_ADC_OFFSET</td>
<td>External Vref = 1.5 V; fc = 80MHz = 5 MHz</td>
<td>word</td>
<td>0x0362</td>
<td></td>
</tr>
<tr>
<td>CAL_ADC_GAIN_FACTOR</td>
<td>External Vref = 1.5 V; fc = 80MHz = 5 MHz</td>
<td>word</td>
<td>0x0360</td>
<td></td>
</tr>
</tbody>
</table>

Using the Calibration Values

• To correct for reference calibration:

$$ADC\text{(corrected)} = ADC\text{(raw)} \times CAL\_ADC\_15VREF\_FACTOR \times \frac{1}{2^{15}}$$

• To correct for gain error:

$$ADC\text{(gain\_corrected)} = ADC\text{(raw)} \times CAL\_ADC\__GAIN\_FACTOR \times \frac{1}{2^{15}}$$

• To correct for offset:

$$ADC\text{(offset\_corrected)} = ADC\text{(raw)} + CAL\_ADC\_OFFSET$$
5xx ADC12_A Enhanced Features

- Lower power
- Selectable speed vs power for reference
- Larger clock dividers for faster system clocks
- Selectable resolution

5xx ADC12_A Improvements

ADC Current Consumption:

<table>
<thead>
<tr>
<th>ADC12</th>
<th>Operating supply current into AVCC terminal (see Note 3)</th>
<th>5xx DCUX = 5.0 MHz</th>
<th>5xx DCUX = 5.0 MHz</th>
<th>2.2 V</th>
<th>6.65</th>
<th>1.3</th>
<th>mA</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ADC1ON = 0, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12ONi = 0</td>
<td>3 V</td>
<td>0.8</td>
<td>1.8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADC1LA</td>
<td>Operating supply current into AVCC terminal (see Note 4)</td>
<td>5xx DCUX = 5.0 MHz</td>
<td>ADC1ON = 0, REFON = 1, REF2, SV = 1</td>
<td>3 V</td>
<td>6.5</td>
<td>0.3</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>2.2 V</td>
<td>6.5</td>
<td>0.3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3 V</td>
<td>6.5</td>
<td>0.3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Reference Current Consumption:

<table>
<thead>
<tr>
<th>REFB+</th>
<th>Operating supply current into AVCC terminal (see Note 3)</th>
<th>5xx DCUX = 5.0 MHz</th>
<th>5xx DCUX = 5.0 MHz</th>
<th>3 V</th>
<th>100</th>
<th>TBD</th>
<th>µA</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ADC1ON = 0, REFON = 1, REF2, SV = 1</td>
<td>3 V</td>
<td>100</td>
<td>TBD</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.2 V</td>
<td>3 V</td>
<td>100</td>
<td>TBD</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
5xx ADC12_A Improvements (cont.)

**Decoupling:**

<table>
<thead>
<tr>
<th>$C_{\text{REF}^+}$ Capacitance at pin $V_{\text{REF}^+}$ (see Note 1)</th>
<th>REFON = 1, $5 \text{ mA} \leq I_{\text{REF}^+}, I_{\text{REF}^-}, I_{\text{REF}^\text{min}}$</th>
<th>2.2 V/3 V</th>
<th>5</th>
<th>10</th>
<th>$\mu$F</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{\text{REF}^-}$ Capacitance at $V_{\text{REF}^-}$ terminal</td>
<td>REFON = REFOUT = 1, $0 \text{ mA} \leq I_{\text{REF}^+}, I_{\text{REF}^-}, I_{\text{REF}^\text{min}}$</td>
<td>2.2 V/3 V</td>
<td>20</td>
<td>100</td>
<td>$\mu$F</td>
</tr>
</tbody>
</table>

**Reference Settling Time:**

<table>
<thead>
<tr>
<th>$I_{\text{REF}^+}$ Settlement time of internal reference voltage (see Figure 16 and Note 2)</th>
<th>$I_{\text{REF}^+} = 0.5 \text{ mA}, C_{\text{REF}^+} = 10 \mu$F, $V_{\text{REF}^+} = 1.5 \text{ V}, V_{\text{AVCC}} = 2.0 \text{ V}$</th>
<th>17</th>
<th>ms</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{\text{REF}^-}$ Settlement time of reference voltage$^{(3)}$</td>
<td>$V_{\text{REF}^+} = 1.5 \text{ V}, V_{\text{AVCC}} = 2.2 \text{ V}$, REFOUT = 0, REFON = 0 ... 1</td>
<td>30</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>$V_{\text{REF}^+} = 1.5 \text{ V}, V_{\text{AVCC}} = 2.2 \text{ V}$, Grade = $V_{\text{AVDD}}$ (max)</td>
<td>50</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>$V_{\text{REF}^+} = 1.5 \text{ V}, V_{\text{AVCC}} = 2.2 \text{ V}$, REFOUT = 1, REFON = 0 ... 1</td>
<td>50</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>$V_{\text{REF}^+} = 2.5 \text{ V}, V_{\text{AVCC}} = 2.8 \text{ V}$, Grade = $V_{\text{AVDD}}$ (max)</td>
<td>50</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>$V_{\text{REF}^+} = 2.5 \text{ V}, V_{\text{AVCC}} = 2.8 \text{ V}$, REFOUT = 1, REFON = 0 ... 1</td>
<td>50</td>
<td>ms</td>
</tr>
</tbody>
</table>

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- ADC12
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- DAC12
- OA

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*Texas Instruments*
ADC10

- 200ksps+
- Autoscan
- Single Sequence
- Repeat-single
- Repeat-sequence
- Int/ext reference
- TA SOC triggers
- Data transfer controller
- 30us ref settling, No decoupling required

Autoscan + DTC Performance Boost

```c
// Software
Res[pRes++] = ADC10MEM;
ADC10CTL0 &= ~ENC;
if (pRes < NR_CONV)
{
  CurrINCH++;
  if (CurrINCH == 3)
  {
    CurrINCH = 0;
    ADC10CTL1 &= ~INCH_3;
    ADC10CTL1 |= CurrINCH;
    ADC10CTL0 |= ENC+ADC10SC;
  }
}
// Autoscan + DTC
_BIS_SR(CPUOFF);```

Fully Automatic
For an n-bit ADC Sine wave input:

\[ SNR = 6.02n + 1.76 \]

Oversampling by k times:

\[ SNR = 6.02n + 1.76 + 10 \log_{10} \left( \frac{F_s}{2F_{\text{max}}} \right) \]

Same total noise, but spread over more frequencies
Oversampling an ADC

- Oversample, filter, decimate
- Common principle to increase resolution
- Can be combined with dithering
- ½ bit for doubling of sampling rate

**Oversampling for Low Power?**

<table>
<thead>
<tr>
<th>Task</th>
<th>ADC10</th>
<th>ADC12</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC + REF on</td>
<td>1.35mA * 30us = 40.5nA-s</td>
<td>.5mA * 17ms = 8.5uA-s</td>
</tr>
<tr>
<td>Convert 16x</td>
<td>1.95mA * 3.4us * 16 = 106.08nA-s</td>
<td>-</td>
</tr>
<tr>
<td>Average (37 cycles)</td>
<td>2.31us * 390uA *16(MHz) = 14.43nA-s</td>
<td>-</td>
</tr>
</tbody>
</table>

161.01nA-s 8.5uA-s

**Oversampling ADC10 for 12-bit resolution is > 50x more efficient!**
Agenda

- ADC12
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- SD16 (_A)
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SD16

- 'F42x, 'FE42x, 'F47x3, 'F47x4
- Multiple converters (channels)
- Single external differential input per converter
- Up to 256 OSR
- 1MHz $f_M$
**SD16_A**

- ‘F42x0 & ‘F20x3
- Single channel
- Multiple differential input pairs
- Input buffer
- AV<sub>CC</sub> measure
- 30kHz to 1.1MHz
- f<sub>M</sub> divider
- Up to 1024 OSR

**Internal Reference**

- Internal 1.2V reference
- 20ppm temperature coefficient
- V<sub>REF</sub> Options:
  - External ref
  - Internal ref
  - Internal ref w/ buffered output
- For temperature (A6): use internal reference
Internal Reference Settling Time

- CVREF = 470nF
- Ref buffer gives > 100x faster settling for ~200uA
- Disable once settled

**Agenda**

- ADC12
- ADC10
- Oversampling
- SD16 (_A)
- DAC12
- OA
DAC12

- 12-bit monotonic
- 8/12-bit voltage output
- Programmable settling time versus power
- Int/ext reference
- Binary or 2’s compliment
- Self-calibration
- Group sync load
- DMA enabled

Intelligent Peripheral Performance

- Increased system flexibility
- No code execution required
- Lower power
- Higher efficiency
Updating DAC12 Output Values

- Immediate
- Rising edge of TA1 or TB2
- Grouped

**Importance Of Timer Triggered DAC**

- Uncertainty less important with more samples
- More overhead
- Limited bandwidth
Importance Of Timer Triggered DAC

• Fewer samples - uncertainty critical
• But higher bandwidth

 Timer trigger allows fewer samples – more bandwidth

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Why Is DMA Important?

![Diagram showing DMA process]

<table>
<thead>
<tr>
<th>// Interrupt</th>
<th>CPU cycles</th>
<th>DMA clocks</th>
</tr>
</thead>
<tbody>
<tr>
<td>; MSP430 ISR for one output waveform</td>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>MOV @R5+,&amp;DAC12_0DAT ; Update DAC0</td>
<td>5</td>
<td>2</td>
</tr>
<tr>
<td>AND #1F,R5 ; Modulo pointer</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>RETI ; Return</td>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>;</td>
<td>18</td>
<td>2</td>
</tr>
</tbody>
</table>

| ; MSP430 ISR for two output waveforms | 6 | 0 |
| MOV @R5+,&DAC12_0DAT ; Update DAC0 | 5 | 2 |
| MOV @R5+,&DAC12_1DAT ; Update DAC1 | 5 | 2 |
| AND #3F,R5 ; Modulo pointer | 2 | 0 |
| RETI ; Return | 5 | 0 |
| ; | 23 | 4 |

Agenda

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Texas Instruments
OA Module Key Features

- Two independent OA modules on-chip
- Selectable GBW products (500kHz, 1.4MHz, 2.2MHz)
- Low current/low speed mode (~50uA: GBW = 500kHz)
- User-configurable feedback network for PGA without external components

OA Module

- Two independent OAs
- Selectable GBW products (500kHz, 1.4MHz, 2.2MHz)
- ~50uA: GBW = 500kHz
- Modes
  - GP mode
  - Unity Gain
  - Comparator
  - Cascade NI PGA
  - Inverting PGA
  - Diff amp
OA: General Purpose Mode

OA: Unity Gain Mode
Summary

- The MSP430 has great integrated analog peripherals and features.
- Diligent examination of specifications and usage of features will provide increased performance and lower power consumption.
- Using somewhat non-traditional solutions like oversampling may provide surprising benefits!
Thank you