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1. Abstract

This application note investigates the implementation of peak current mode control with slope compensation using an single TMS320F28027 (Piccolo A) MCU from Texas Instruments. This MCU is ideal for peak current mode implementation due to its dedicated internal circuitry which enables a fully digital slope compensation scheme. The theory of operation, mathematical modeling and all relevant equations are presented along with a detailed step-by-step design procedure in both analog and digital domains.

A design example and associated experimental results are also presented with two methods of implementation; one using TI's ControlSUITE and one using Biricha’s Chip Support Library (CSL).

Further information with regards to the CSL and digital power design workshops can be found at www.biricha.com/workshops/

2. Introduction

The operation of a digital peak current mode converter is similar to its analog counterpart as shown in Figure 1. However, the compensation network, error amplifier, slope compensation and PWM generator are all replaced by a single microprocessor in the digital converter shown in Figure 2. This application note describes the processes involved in setting up a Piccolo MCU for use within a digital peak current mode power supply.

A complete design example and two complete implementations are given; the first method uses TI’s ControlSUITE whilst the second method uses Biricha’s Chip Support Library (CSL).

The Biricha Digital Chip Support Library provides a fast and simple method of configuring Texas Instruments C2000 MCUs for use in digital power applications. In-depth knowledge of the MCU’s internal registers and associated configuration bits are not required; in place of this, simple function calls are used.

The Biricha Digital CSL documentation contains full descriptions and examples of all of the functions used in the implementation presented here. The user guides and an evaluation copy of CSL can be downloaded from www.biricha.com/resources/

Referring to Figure 2, the operation of the peak current mode controlled power supply is as follows. Initially, the duty is set to 100% and the...
PWM is driven high. The output voltage of the converter is applied to a sampling divider network which is connected to the Piccolo’s ADC. The voltage is sampled and converted to a digital value. A digital reference (REF) is subtracted from the digital value and the resulting error value is used as an input to the digital controller (2p2z Controller). This represents the error amplifier and compensation network of the analog equivalent. A full design procedure for this controller will be given later on in this paper.

The output of the controller is then multiplied by a gain term $K$. This gain scales the output of the controller to a digital value that is suitable for use with the DAC of the comparator module, counteracting the effects of the various gains within the closed loop system. The value of this gain term can be calculated to obtain the correct crossover frequency; details are given in the design example.

This scaled output is then used as an input to the DAC connected to the comparator’s inverting input. The non-inverting input is connected to the current sense transformer; the gain of this is represented by the $R_i$ block. The current spike associated with turning the MOSFET switch on is ignored through the use of leading edge blanking within the Piccolo’s blanking block. The output of the comparator will change state when the inductor current reaches the level of the voltage on the DAC output. This causes a cycle-by-cycle trip event to occur within the digital compare submodule of the PWM module. The PWM signal will be low for the remainder of the switching period. Therefore, as with the analog equivalent, the duty is determined by the peak of the inductor current in the power stage of the converter. The digital implementation of peak current mode control achieves the desirable cycle-by-cycle peak current limiting effect of the analog equivalent. Full experimental results will be given shortly.
3. Peak Current Mode Model

The Buck converter in Figure 3 is used to describe the peak current mode model used in this application note. However the same procedure can be applied to other topologies.

![Figure 3. A typical Buck converter](image)

In order to design a stable compensator, we first need a mathematical model of the Buck converter plant. According to [3], this can be described by three terms:

1. \( F_H(s) \), a high frequency transfer function.
2. \( H_{DC} \), a DC gain.
3. \( H_B(s) \), a power stage small signal model.

The complete control-to-output transfer function for a Buck converter under peak current mode control, as described in [1], is a combination of these three terms:

\[
H_{CO}(s) = \frac{V_{OUT}(s)}{V_{ERR}(s)} = F_H(s) \times H_B(s) \times H_{DC}
\]

(1)

**High Frequency Transfer Function**

The high frequency transfer function, \( F_H(s) \), has a double pole at half the switching frequency, \( F_s/2 \). Inevitably this will result in a resonant peak occurring at this frequency. Therefore this peak needs to be damped in order to avoid the gain Bode plot crossing the 0dB axis at resonance and causing instability.

A compensating ramp is added to the system to effectively damp resonant peak; this called “slope compensation”. This is achieved by setting the Q of this double pole system to 1. A low Q forces a damped this resonant peak and reduces the gain at \( F_s/2 \).

For a Buck converter, the required peak-to-peak value of the external compensation ramp has been calculated in [2] and is given in Equation (2). This compensating ramp reduces the Q of the high frequency transfer function to 1.

\[
V_{PP} = -\frac{(0.18 - D)R_TsV_{IN}}{L_0}
\]

(2)

Where:

- Current-sense transformer gain: \( R_i \)
- Switching period: \( T_s \)
- Input voltage: \( V_{IN} \)
- Output inductor: \( L_0 \)

The duty, \( D \), is:

\[
D = \frac{V_O}{V_{IN}}
\]

Where \( V_O \) is the output voltage.

With Q set to 1 \( F_H(s) \) simplifies to that given in Equation (3).

\[
F_H(s) = \frac{1}{1 + \frac{s}{\omega_N} + \frac{s^2}{\omega_N^2}}
\]

(3)

Where:

\[
\omega_N = \pi F_s \text{ in rad/s} \Rightarrow \left( i.e. \frac{1}{2} F_s \text{ in Hz} \right)
\]
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