



# TI Data Converter Guide

Analog Drives Digital



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### TECHNOLOGY REVIEW

Data acquisition and conversion systems are used to acquire analog signals from one or more sources and convert these signals into digital form for analysis or transmission by end devices. The analog signal inputs to data acquisition systems are most often generated from sensors and transducers which convert real-world parameters such as pressure, temperature, stress or strain, flow, etc., into equivalent electrical signals. These signals are then converted by the data acquisition system and are then utilised by the end devices in digital form. Depending on system requirements, data conversion functions may be discrete components or they may be integrated with the DSP. Integration decisions depend on which technologies can be combined cost-efficiently without sacrificing performance or power consumption. In a cell phone low power and low cost are critical, whereas a base station demands top performance for greater channel density. Analog process development provides the manufacturing technologies that make those products possible. Requirements vary enormously among the different analog functions and various systems where they are used. To support a specific application in System on Chip (SoC) designs, a strategy of integrating all critical analog and digital functions is required. This approach requires that the same advanced CMOS processes used to create high-performance DSPs, microcontrollers and ASICs also support some analog components. But many analog functions are not optimised for integration with high-speed digital logic. In these cases, analog product development teams focus on analog-only integration, with optimised components for precision, speed and power.

#### BiCom3 High-Speed BiCMOS Process

Speed-critical applications in telecommunications and other areas demand extremely high switching speeds that can only be achieved by adding bipolar transistors to a high-performance analog CMOS process. The BiCom3 High-Speed BiCMOS process is designed for high-frequency operation in signal conditioning and data conversion. Adding the speed of Silicon-Germanium (SiGe) bipolar transistors to 5 V, 0.35 micron CMOS logic, the BiCom3 process is designed

with the best high performance component set. As the industry's first production process to feature complementary SiGe PNP and NPN transistors, BiCom3 offers high voltage, high transistor gain, high  $f_T$ , low capacitance for low Total Harmonic Distortion (THD) and low power consumption. All of these features are critical to wireless, as well as other communications equipment. Other features include MIM capacitors, trench isolation for circuit protection and Nickel-Chromium-Aluminum (NiCrAl) thin-film resistors with low Sheet Resistance (RS) to handle high currents. Silicon-On-Insulator (SOI) techniques provide low, highly linear capacitance and improve isolation and speed.

#### HPA07 Precision Analog CMOS Process

One of TI's core analog technologies is the HPA07 precision analog CMOS process, which offers extremely low-noise performance for communications and other systems where analog and high-speed digital functions must co-exist with minimal signal interference. Incorporating the logic and memory of its fundamental 5 V, 0.3 micron digital CMOS process, the HPA07 process then adds specialised transistors and passive components for analog functionality. Isolation shields analog signals from the high-frequency interference of digital circuits and exceptional component matching promotes precision.

Key components include low-noise transistors with extremely low THD characteristics. The transistors are created using a buried-channel PMOS technique, which allows tighter noise characteristics control to give the best gain bandwidth/noise ratio for this class of device. Silicon-Chromium (SiCr) thin film resistors with very low temperature coefficients provide stability over the entire working temperature range. Metal-Insulator-Metal (MIM) capacitors with tight alignment and low parasitics reduce size while providing a 4X improvement in voltage coefficients over previous processes. Drain extended CMOS transistors that handle up to 30 V for driving signals enable the process to extend to higher voltage applications.

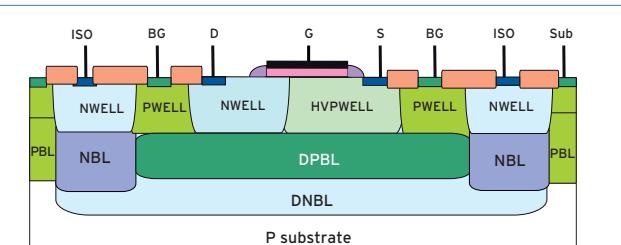


Figure 1: Isolated 36 V Asymmetric DeNMOS

#### Transistor Performances for BiCom3

NPN Performance		PNP Performance	
$\beta$	200	$\beta$	140
$V_A$	100 V	$V_A$	200 V
$BV_{CEO}$	6.4 V	$BV_{CEO}$	5.9 V
$f_T$	26 GHz	$f_T$	26 GHz
FOM	3.2E6	FOM	4.1E6

## ADC ARCHITECTURES

Many circuit designs have been tried in the development of ADCs. The field has been narrowed to four basic topologies: flash, Successive-Approximation (SAR), pipeline, and  $\Delta\Sigma$ -converters. The optimum device for a particular system depends on what needs to be done with the data. The speed-resolution comparison between the four most popular converter types is shown in Figure 2. As new circuit techniques are developed, the performance boundaries between them have become somewhat blurred.

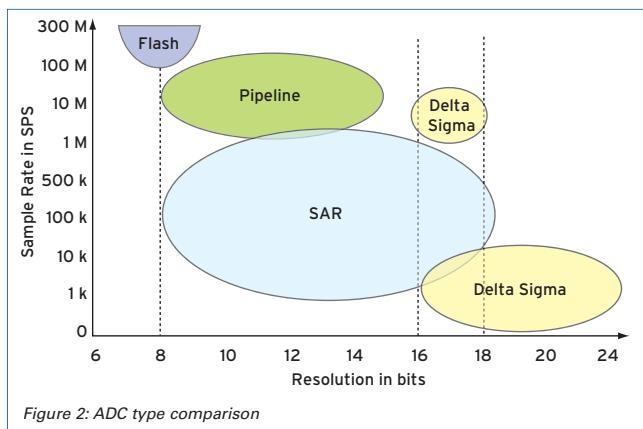


Figure 2: ADC type comparison

Beyond the speed-resolution distinction, the next performance point is time-of-reading. The flash converter is a very high-speed device and time synchronisation usually is not an issue. In contrast, the SAR converter uses a start-convert signal. With this capability, two or more devices can be synchronised to an external event. The data appears several clock cycles following the convert command.

Both the pipeline and  $\Delta\Sigma$ -topology converters are continuous-conversion devices. This makes it nearly impossible to synchronise multiple devices for simultaneous reading, or to obtain a snapshot reading at a defined moment. There will be a data latency between an event at the analog input and the appearance of that event in the digital data stream.

$\Delta\Sigma$ -converters can be compared to performing a running average. The pipeline converter, however, can be compared to an assembly line. After a station contributes to the final result, the signal moves on, making way for that station to process the next sample. One result of this difference is that  $\Delta\Sigma$ -converters effectively transpose noise energy to frequency bands above the frequencies of interest. Pipeline-style converters accomplish high data rates with moderate-to-high resolution.

### Pipeline ADCs

The pipeline converter is a clocked topology where every action happens on a clock timing cycle. On the first clock, the applied signal,  $V_{IN}$ , is captured in a sample-and-hold block (S/H1). This voltage ( $V_1$ ) is applied to comparator B1. If  $V_1 < V_{REF}$ , then SW1A is closed,  $V_1$  is amplified by two, and the result is applied to the next stage. If  $V_1 > V_{REF}$ , then SW1B is closed, the value ( $V_1 - V_{REF}$ ) is amplified by two

and that result is applied to the next stage. When SW1A is closed, a binary zero is recorded for the Most Significant Bit (MSB). This is because the applied voltage is less than one-half the full-scale voltage ( $V_{fs}/2$ ).

When SW1B is closed, a binary one is recorded for the MSB because the applied voltage is greater than  $V_{fs}/2$ . On the next clock cycle, this process is repeated at the second stage to determine the value of MSB – 1. Since the first stage is now vacant, it will process the next analog-input value.

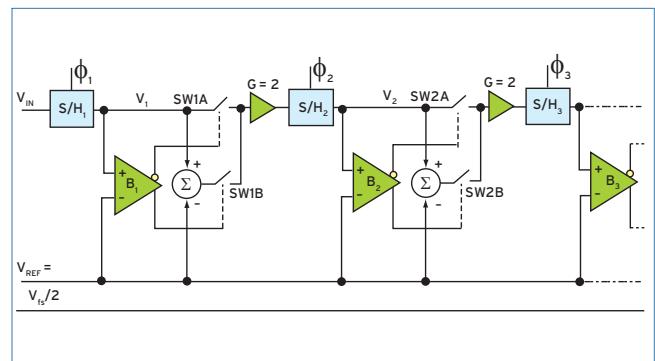


Figure 3: Simplified pipeline converter

### SAR ADCs

The SAR converter is a hardware realisation of a binary-search tree. In concept, a logic circuit takes a guess at a digital value, stores that in a latch and applies it to a DAC. A comparator determines if the guess, as reported by the DAC, is high or low and then reports to the logic, to guide the next guess. The first guess is established mid-way between zero and full scale, done by setting the MSB to one. If  $V_{IN}$  is greater than the DAC output, the bit is left on. If less than one, it is reset to zero. This binary-search tree procedure continues, on each successive clock cycle, to test the next-lower significant bit. The D/A converter of Figure 4 is built from a resistor ladder.

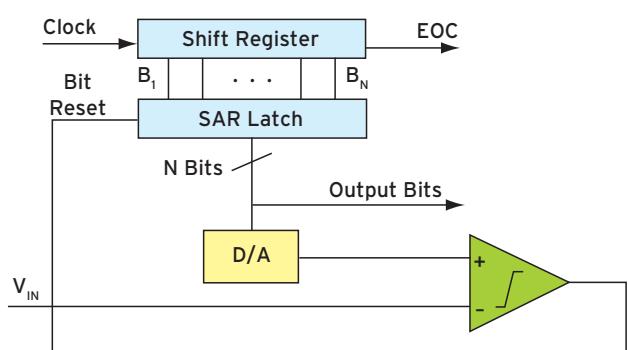


Figure 4: SAR block diagram

The value of  $V_{IN}$  must not change during the entire conversion procedure. Therefore, this circuit requires an external Sample-and-Hold (S/H) function. In place of the resistive-ladder DAC, most modern devices use a capacitive DAC (C-DAC), Figure 5, which inherently provides the S/H function, by nature of its design.

The C-DAC has the advantage that capacitors are smaller in silicon area than resistors, so the chip cost is lower. Thus, the capacitor structure provides a built in S/H function while also reducing cost and complexity for the user.

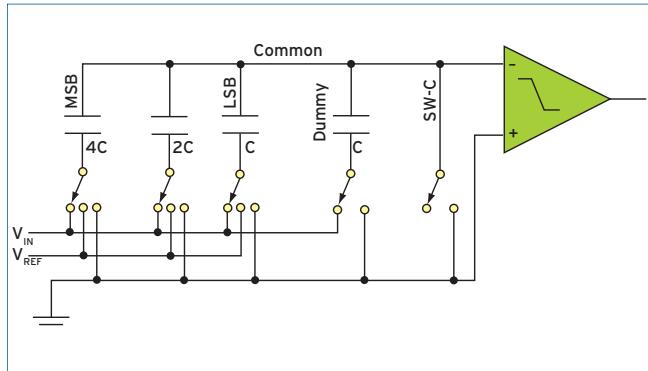


Figure 5: Three-bit C-DAC circuit

### Delta-Sigma ( $\Delta\Sigma$ ) ADCs

The  $\Delta\Sigma$ -converter is a primitive, one-bit ADC operating at a very high sample rate which averages the results over a large sample, to obtain a high-resolution result. The digital representation of the input signal is determined by the percentage of ones in the high-speed bit stream. This is accomplished by a decimation filter to determine the final conversion value. The heart of this converter is the modulator (Figure 6).

All of the converters previously discussed have been open-loop systems. The  $\Delta\Sigma$ -modulator is a closed-loop system which maintains the average number of digital ones at the output equal to the input signal's percentage of full scale. If  $V_{IN}$  equals half the  $V_{fs}$ , the bit stream will contain an equal number of ones and zeros. In other applications this output

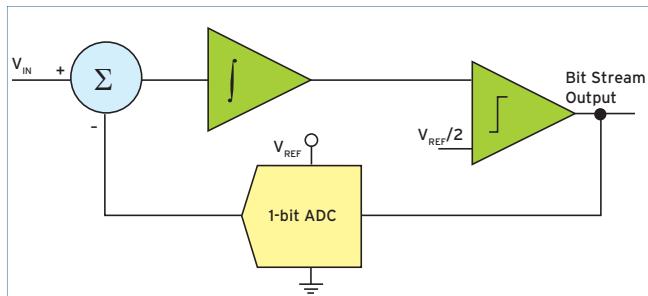


Figure 6:  $\Delta\Sigma$ -modulator

stream encoding is known as Pulse Proportion Modulation (PPM). Deviation from an ideal PPM sequence is a form of noise in the modulator output. An integrator is a single pole, low-pass filter. Thus, the noise level can be reduced by adding a second integrator. The following digital low-pass and decimation filters establish the output data rate, which will be greatly different from the rate at which the input signal is sampled. The way these filters are designed determines the data latency. The time from a step change in the input signal to a stable digital output, reflecting that change, will always be at least one data cycle. Different filter designs require various numbers of data cycles to reach a stable output. This technique shapes the conversion noise

to the high input-sample frequency band, away from the frequency band of interest.

## DAC ARCHITECTURES

### String

The string architecture is as the name implies, a series of resistors placed in series to build a string. In theory, one would need 256 resistors to build an 8-bit DAC. Increasing the resolution means also increasing the number of resistors needed to build a string DAC. And, for a 16-bit DAC, one would need a total of 65,536 resistors to generate all the possible voltages/digital steps. However, in the real world of design it is impractical to implement nearly 66 thousand resistors on a single chip. Hence, designers came up with additional smaller circuitry such as interpolating amplifiers that reduce the necessary amount of resistors and tapping points on the resistor string, allowing a more power-efficient and less space-consuming design. The interpolating amplifier is used as an output buffer. Some of today's string architectures have a pin available for the amplifier's external feedback loop.

### R-2R DACs

These DACs are used to achieve the best Integral Linearity (INL) performance. In an R-2R DAC, a current is generated by a reference voltage, which flows through the R-2R resistor network based on the digital input, which divides the current by two at each R2R node. The advantage of an R-2R type DAC is that it relies on the matching of the R and 2R resistor segments and not the absolute value of the resistors thus allowing trim techniques to be used to adjust the integral linearity (INL) and differential linearity (DNL). With a basic R-2R architecture, it is possible to either generate a current output or a voltage output.

### High-Speed DACs

Modern high-speed DACs, fabricated on submicron CMOS or BiCMOS processes, have reached new performance levels with update rates of 1 GSPS and resolutions of 16 bits. In order to realise such high update rates and resolutions, the DACs employ a current-steering architecture with segmented current sources. The core element within the monolithic DAC is the current source array designed to deliver the full-scale output current, typically 20 mA. An internal decoder addresses the differential current switches each time the DAC is updated. Steering the currents from all current sources to either of the differential outputs forms a corresponding signal output current. Differential signaling is used to improve the dynamic performance while reducing the output voltage swing that is developed across the load resistors. Ideally, this signal voltage amplitude should be as small as possible to maintain optimum linearity of the DAC. The upper limit of this signal voltage and consequently the load resistance, is defined by the output voltage compliance specification. The segmented current-steering architecture provides a significant reduction in circuit complexity and consequently in reduced glitch energy. This translates into an overall improvement of the DAC's linearity and ac performance.

## ADC INPUT DRIVERS

Data acquisition systems generally require an amplifier preceding the ADC to buffer the input signal. Most modern ADCs possess complex input characteristics due to the capacitive charging and switching that occurs during sampling and conversion. This behavior causes transient currents on the ADC's input that can disturb or distort a precision analog input signal. The input amplifier serves to provide a stable, accurate signal in the presence of these current transients. It can also provide gain (or attenuation), level shifting, filtering and other signal conditioning functions.

### THS452x

The THS452x family of devices are very low-power, fully differential op-amps with rail-to-rail output and an input common-mode range that includes the negative rail. These amplifiers are designed for low-power data acquisition systems and high-density applications where power dissipation is a critical parameter. The family includes single (THS4521), dual (THS4522), and quad (THS4524) versions. These fully differential op-amps feature accurate output common-mode control that allows for DC-coupling when driving ADCs. The devices are ideally suited for driving both SAR and  $\Delta\Sigma$ -ADCs. The THS4521, THS4522 and THS4524 family of fully differential op-amps is characterised for operation over the full industrial temperature range from -40...+85 °C.

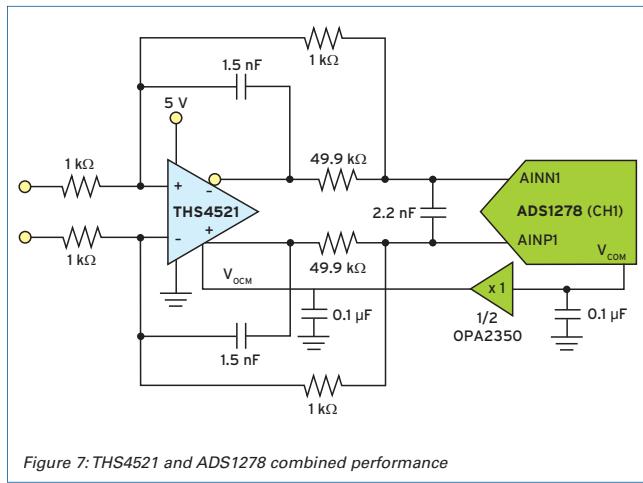


Figure 7: THS4521 and ADS1278 combined performance

### OPA2695

The OPA2695 is a dual, very high bandwidth, current-feedback op-amp that combines exceptional 2900 V/ $\mu$ s slew rate and low input voltage noise to deliver a precision, low-cost, high dynamic range Intermediate Frequency (IF) amplifier. The OPA2695 is an ideal choice as a differential driver, such as for a high-speed ADC. The OPA2695 low 12.9 mA/channel supply current is precisely trimmed at +25 °C. This trim, along with a low temperature drift, gives low system power over temperature. System power may be further reduced with the optional disable control pin. If pulled low, the OPA2695 supply current drops to less than 200  $\mu$ A/channel. This power-saving feature, along with exceptional single +5 V operation, makes the OPA2695 ideal for portable applications. The OPA2695 is available in an SO-8 (without disable) package or QFN-16 package (with disable).

### OPA211

The OPA211 series of precision operational amplifiers achieves very low 1.1 nV/ $\sqrt{\text{Hz}}$  noise density with a supply current of only 3.6 mA. This series also offers rail-to-rail output swing, which maximises dynamic range. The extremely low voltage and low current noise, high speed and wide output swing of the OPA211 series make these devices an excellent choice as a loop filter amplifier in PLL applications. In precision data acquisition applications, the OPA211 series of op-amps provides 700 ns settling time to 16-bit accuracy throughout 10 V output swings. This AC-performance, combined with only 125  $\mu$ V of offset and 0.35  $\mu$ V/ $^{\circ}$ C of drift over temperature, makes the OPA211 ideal for driving high-precision 16-bit ADCs or buffering the output of high-resolution DACs. The OPA211 series is specified over a wide dual-power supply range of  $\pm 2.25\ldots\pm 18$  V, or for single-supply operation from 4.5...36 V. The OPA211 is available in the small DFN-8 ( $3 \times 3$  mm $^2$ ), MSOP-8 and SO-8 packages. A dual version, the OPA2211, is available in the DFN-8 ( $3 \times 3$  mm $^2$ ) or an SO-8 PowerPAD package. This series of op amps is specified from -40...+125 °C.

### OPA827

The OPA827 series of JFET op-amps combine outstanding DC-precision with excellent AC-performance. These amplifiers offer low offset voltage (150  $\mu$ V, max), very low drift over temperature (1.5  $\mu$ V/ $^{\circ}$ C, typ), low bias current (15 pA, typ), and very low 0.1...10 Hz noise (250 nV<sub>pp</sub>, typ). The device operates over a wide supply voltage range,  $\pm 4\ldots\pm 18$  V on a low supply current (4.8 mA/Ch, typ). AC-characteristics, such as a 22 MHz gain bandwidth product, a slew rate of 28 V/ $\mu$ s and precision DC-characteristics make the OPA827 series well-suited for a wide range of applications including 16...18-bit mixed signal systems, transimpedance (I/V-conversion) amplifiers, filters, precision  $\pm 10$  V front ends and professional audio applications. The OPA827 is available in both SO-8 and MSOP-8 surface-mount packages and is specified from -40...+125 °C.

### OPA2614

The OPA2614 offers very low 1.8 nV/ $\sqrt{\text{Hz}}$  input noise in a wideband, high gain bandwidth, voltage-feedback architecture. Intended for xDSL driver applications, the OPA2614 also supports this low input noise with exceptionally low harmonic distortion, particularly in differential configurations. Adequate output current is provided to drive the potentially heavy load of a twisted-pair line. Harmonic distortion for a 2VPP differential output operating from 5...12 V supplies is  $\leq -80$  dBc through 1 MHz input frequencies. Operating on a low 6.0 mA/ch supply current, the OPA2614 can satisfy most xDSL driver requirements over a wide range of possible supply voltage – from a single +5 condition, to  $\pm 5$  V, on up to a single +12 V design. General-purpose applications on a single +5 V supply will benefit from the high input and output voltage swing available on this reduced supply voltage. Baseband I/Q receiver channels can achieve almost perfect channel match with noise and distortion to support signals through 5 MHz with >14-bit dynamic range.

## Pipeline ADCs

### ADS614x (612x)

ADS614X (ADS612X) is a family of 14-bit (12-bit) ADCs with sampling rates up to 250 MSPS. It combines high dynamic performance and low power consumption in a compact 48-QFN package. ADS614X/2X has fine gain options that can be used to improve SFDR performance at lower full-scale input ranges. It includes a DC offset correction loop that can be used to cancel the ADC offset. Derivatives for both DDR LVDS (Double Data Rate) and parallel CMOS digital output interfaces are available. At lower sampling rates, the ADC automatically operates at scaled down power with no loss in performance.

It includes internal references while the traditional reference pins and associated decoupling capacitors have been eliminated. Nevertheless, the device can also be driven with an external reference. The device is specified over the industrial temperature range (-40...+85 °C).

### ADS556x

ADS556X is a high performance 16-bit ADC family with sampling rates up to 80 MSPS. It supports very high SNR for input frequencies in the first Nyquist zone. The device includes a low frequency noise suppression mode that improves the noise from DC to about 1 MHz. Innovative techniques, such as DDR LVDS and an internal reference that does not require external decoupling capacitors, have been used to achieve significant savings in pin-count. This results in a compact 7 x 7 mm<sup>2</sup> 48-pin QFN package.

The device can be put in an external reference mode, where the V<sub>CM</sub> pin behaves as the external reference input. For applications where power is important, ADS556X offers power down modes and automatic power scaling at lower

sample rates. It is specified over the industrial temperature range (-40...+85 °C).

### ADS548x

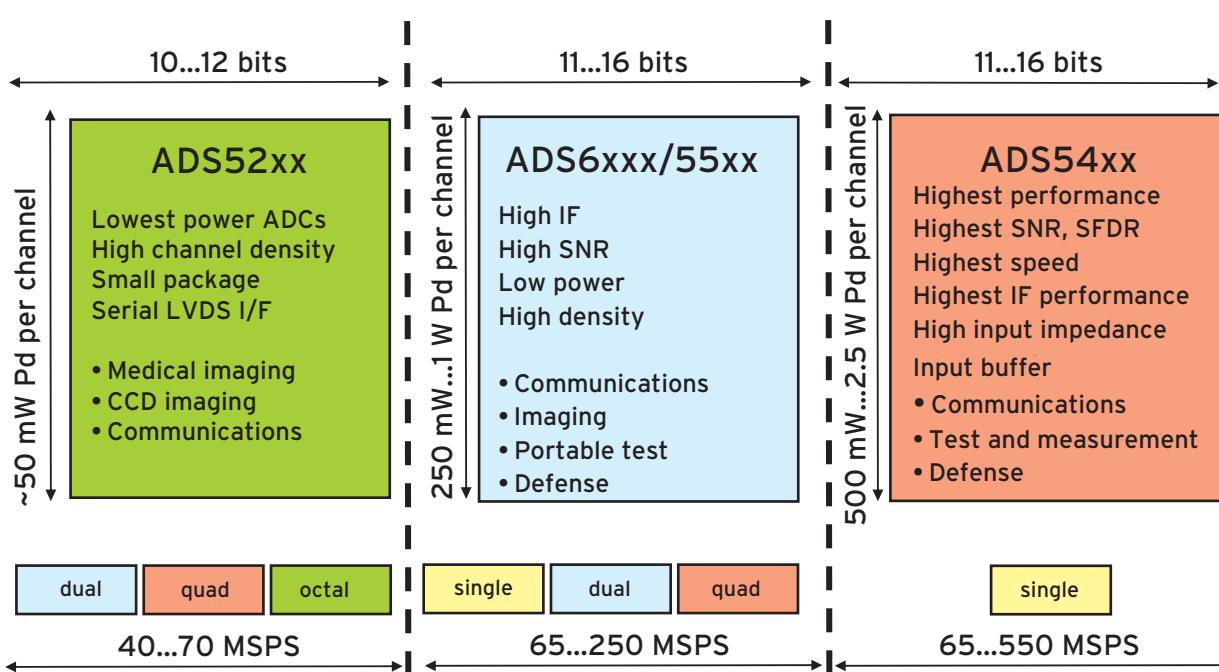
The ADS548x is a 16-bit family of Analog-to-Digital Converters (ADCs) that operate from both a 5 V supply and 3.3 V supply while providing LVDS-compatible digital outputs. The ADS548x integrated analog input buffer isolates the internal switching of the onboard Track and Hold (T&H) from disturbing the signal source while providing a high-impedance input. An internal reference generator is also provided to simplify the system design. Designed for highest total ENOB, the ADS548x family has outstanding low noise performance and spurious-free dynamic range.

The ADS548x is available in a QFN-64 PowerPAD package. The device is built on Texas Instruments complementary bipolar process (BiCom3) and is specified over the full industrial temperature range (-40...+85 °C).

### ADS5474

The ADS5474 is a 14-bit, 400 MSPS ADC that operates from both a 5 V supply and 3.3 V supply while providing LVDS-compatible digital outputs. This ADC is one of a family of 12/13/14-bit ADCs that operate from 210...550 MSPS with an input bandwidth of up to 2.3 GHz. The ADS5474 input buffer isolates the internal switching of the onboard Track and Hold (T&H) from disturbing the signal source while providing a high-impedance input. An internal reference generator is also provided to simplify the system design.

The ADS5474 is available in an TQFP-80 PowerPAD package. The device is built on Texas Instruments complementary bipolar process (BiCom3) and is specified over the full industrial temperature range (-40...+85 °C).



## SAR ADCs

### ADS8517

The ADS8517 is a complete low-power, single 5 V supply, 16-bit sampling ADC. It contains a complete, 16-bit, capacitor-based, SAR ADC with sample-and-hold, clock, reference and data interface.

The converter can be configured for a variety of input ranges including  $\pm 10/4$  and 5 V. For most input ranges, the input voltage can swing to 25 V or -25 V without damage to the device. An SPI-compatible serial interface allows data to be synchronised to an internal or external clock. A full parallel interface using the selectable BYTE pin is also provided to allow the maximum system design flexibility.

The ADS8517 is specified at a 200 kHz sampling rate over the industrial -40...+85 °C temperature range.

### ADS7865

The ADS7865 is a dual, 12-bit, 2 MSPS ADC with four fully differential or six pseudo-differential input channels grouped into two pairs for high-speed, simultaneous signal acquisition. Inputs to the Sample-and-Hold (S/H) amplifiers are fully differential and are maintained differentially to the input of the ADC.

This architecture provides excellent common-mode rejection of 72 dB at 100 kHz, which is a critical performance characteristic in noisy environments. The ADS7865 is pin-compatible with the ADS7862, but offers additional features. The ADS7865 is offered in a TQFP-32 package. It is specified over the extended operating temperature range of -40... +125 °C.

### ADS7882

The ADS7882 is a 12-bit 3 MSPS ADC with 2.5 V internal reference. The device includes a capacitor based SAR ADC with inherent sample and hold.

The device offers a 12-bit parallel interface with an additional byte mode that provides easy interface with 8-bit processors. The device has a pseudo-differential input stage. The -IN swing of  $\pm 200$  mV is useful to compensate for ground voltage mismatch between the ADC and sensor and also to cancel common-mode noise.

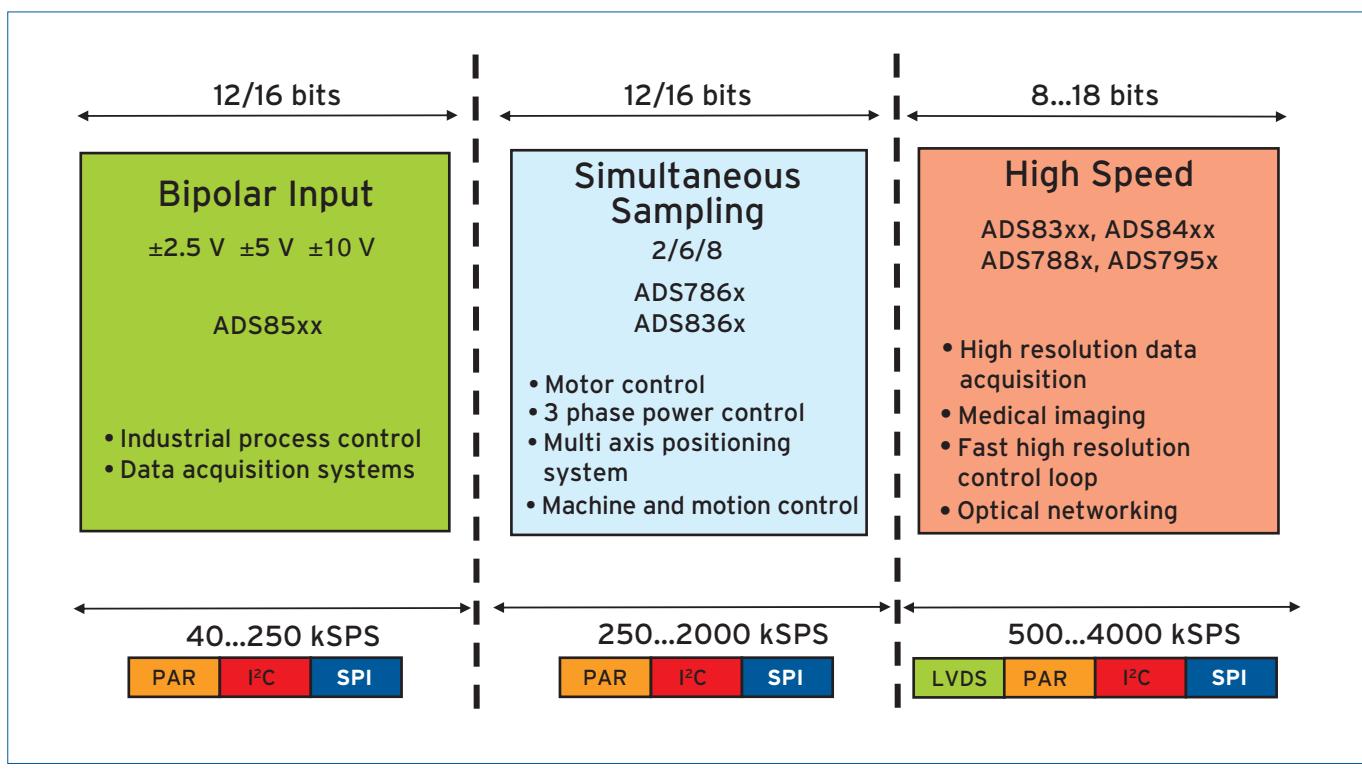
With nap mode enabled, the device operates at lower power when used at lower conversion rates. The device is available in 48-pin TQFP package.

### ADS8329/30

The ADS8329 is a low-power, 16-bit, 1 MSPS ADC with a unipolar input. The device includes a 16-bit capacitor-based SAR ADC with inherent sample-and-hold.

The ADS8330 is based on the same core and includes a 2-to-1 input MUX with programmable option of TAG bit output. Both the ADS8329 and ADS8330 offer a high-speed, wide voltage serial interface and are capable of chain mode operation when multiple converters are used.

These converters are available in 4 x 4 QFN and 16-pin TSSOP packages and are fully specified for operation over the industrial -40...+85 °C temperature range.



## DELTA SIGMA ADCs

### ADS1675

The ADS1675 is a high-speed, high-precision ADC. Using an advanced  $\Delta\Sigma$ -architecture, it operates at speeds up to 4 MSPS. The ADS1675 is comprised of a low-drift modulator with out-of-range detection and a dual-path programmable digital filter. The dual filter path allows the user to select between two post-processing filters: low-latency or wide-bandwidth. The low-latency filter settles quickly (as fast as 2.65  $\mu$ s), for applications with large instantaneous changes, such as a multiplexer. The wide-bandwidth path provides an optimised frequency response for AC measurements with a passband ripple of less than  $\pm 0.00002$  dB, stop band attenuation of 115 dB and a bandwidth of 1.7 MHz.

The device offers two speed modes with distinct interface, resolution and feature set. In the high-speed mode the device can be set to operate at either 4 MSPS or 2 MSPS. In the low-speed mode, it can be set to operate at either 1 MSPS, 500/250/125 kSPS.

The flexible serial interface supports data readback with either standard CMOS and LVDS logic levels, allowing the ADS1675 to directly connect to a wide range of microcontrollers, DSPs, FPGAs. The ADS1675 operates from an analog supply of 5 V and digital supply of 3 V and dissipates 575 mW of power. The device is fully specified over the industrial temperature range and is offered in a TQFP-64 package.

### ADS1174 / 1178

The ADS1174 (quad) and ADS1178 (octal) are multiple  $\Delta\Sigma$ -ADCs with data rates up to 52 kSPS, which allow synchronous sampling of four and eight channels. These devices are also compatible with the high-performance 24-bit ADS1274 and ADS1278, permitting drop-in upgrades.

The  $\Delta\Sigma$ -architecture offers near ideal 16-bit AC-performance (97 dB SNR, -105 dB THD, 1 LSB linearity) combined with 0.005 dB passband ripple and linear phase response.

The high-order, chopper-stabilised modulator achieves very low drift (2  $\mu$ V/ $^{\circ}$ C offset, 2 ppm/ $^{\circ}$ C gain) and low noise (1 LSBPP). The on-chip FIR filter provides a usable signal bandwidth up to 90% of the Nyquist rate with 100 dB of stop band attenuation while suppressing modulator and signal out-of-band noise. Two operating modes allow for optimisation of speed and power: high-speed mode (31 mW/Ch at 52 kSPS) and low-power mode (7 mW/Ch at 10 kSPS).

The devices are fully specified over the extended industrial range (-40...+105  $^{\circ}$ C) and are available in an HTQFP-64 PowerPAD package.

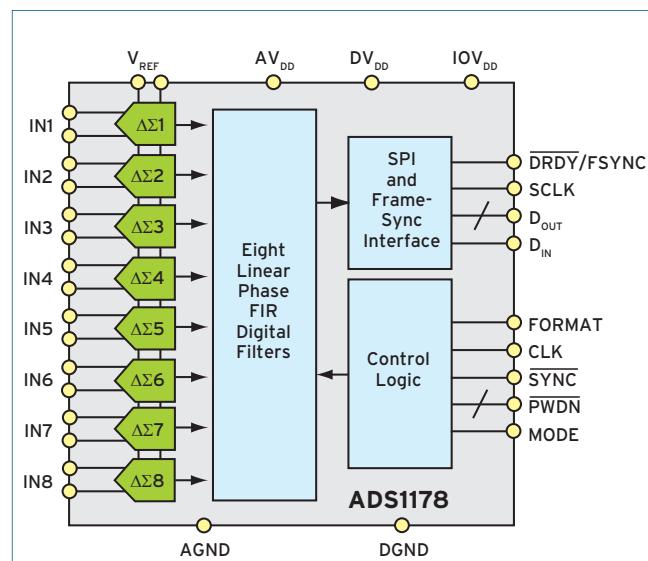
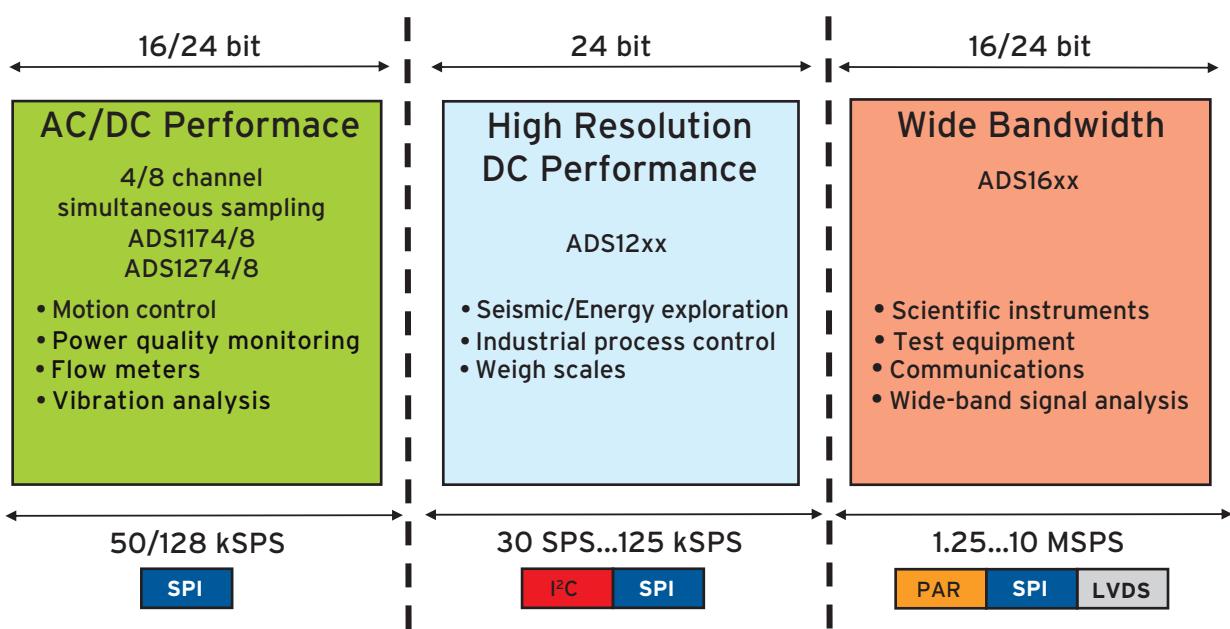


Figure 8: ADS1178



## C2000 PORTFOLIO WITH ON CHIP ADCs

TMS320C2000™ microcontrollers combine control peripheral integration with the processing power of a 32-bit architecture. All C28x™ microcontrollers are 100% software compatible and offer high-speed 12-bit ADCs and advanced PWM generators.

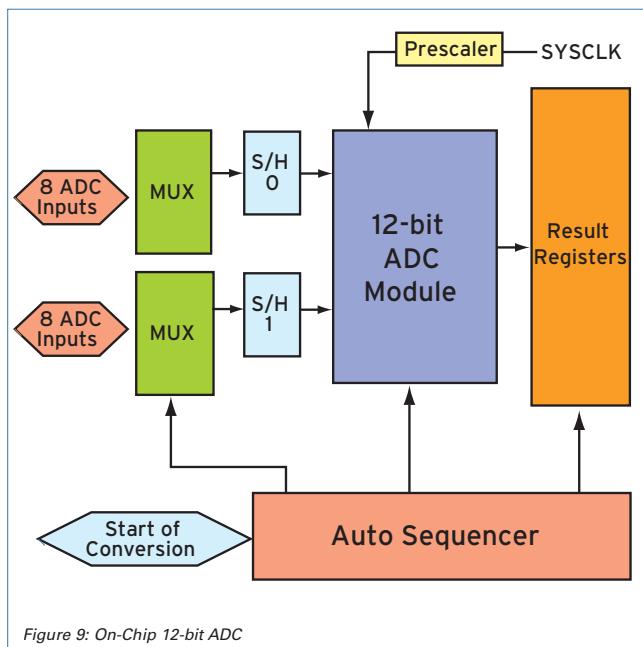


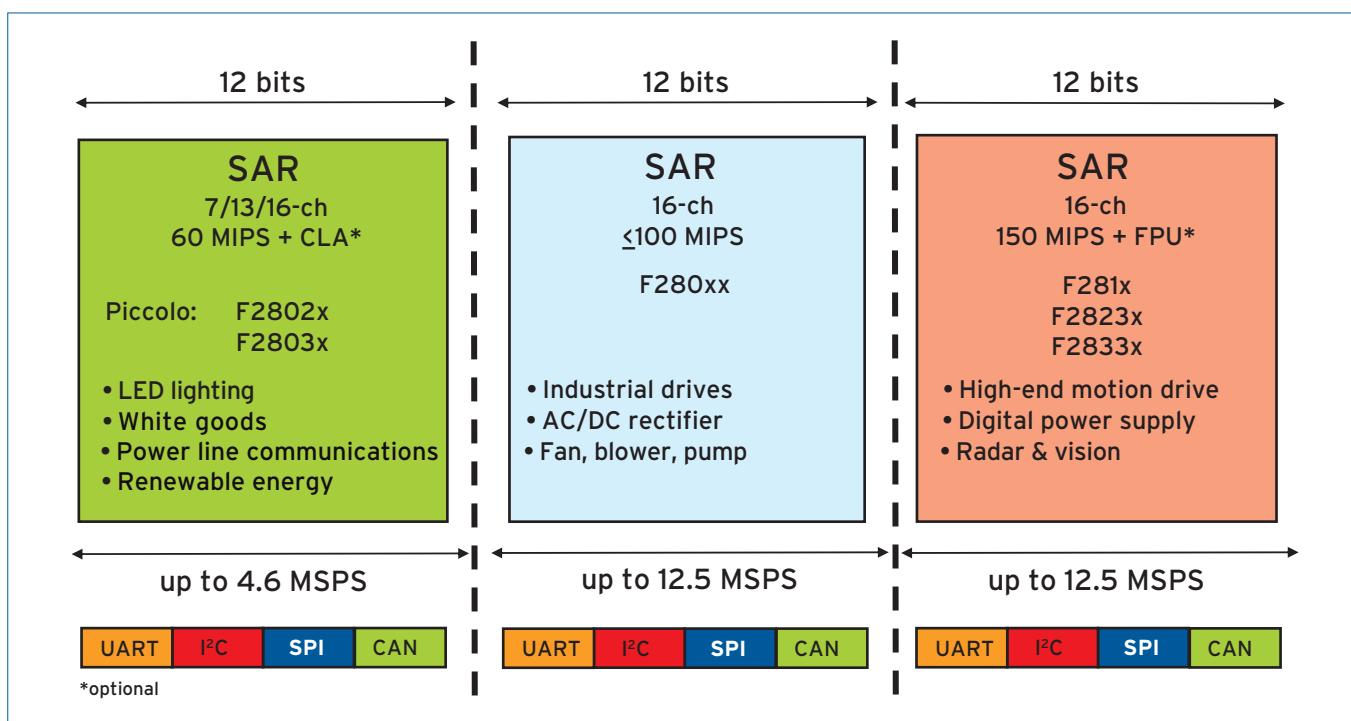
Figure 9: On-Chip 12-bit ADC

### Features

- Up to 12.5-MSPS throughput
- Number of channels dependent on package size:  
7/13/16 input channels

- Dual sample/hold enable simultaneous sampling or sequencing sampling modes
- Analog input: 0...3.3 V (ratiometric)
- Auto Sequencer supports up to 16 conversions without CPU intervention
- Sequencer can be operated as two independent 8-state sequencers or as one large 16-state sequencer
- 16 result registers (individually addressable) to store conversion values

The ADC module in the C2000™ family has been enhanced to provide flexible interface to ePWM peripherals. The ADC interface is built around a fast, 12-bit ADC module with a fast conversion rate of up to 80 ns at 25 MHz ADC clock. The ADC module has up to 16 channels, configurable as two independent 8-channel modules. The two independent 8-channel modules can be cascaded to form a 16-channel module. Although there are multiple input channels and two sequencers, there is only one converter in the ADC module. The two 8-channel modules have the capability to autosequence a series of conversions, each module has the choice of selecting any one of the respective eight channels available through an analog MUX. In the cascaded mode, the autosequencer functions as a single 16-channel sequencer. On each sequencer, once the conversion is complete, the selected channel value is stored in its respective RESULT register. Autosequencing allows the system to convert the same channel multiple times, allowing the user to perform oversampling algorithms. This gives increased resolution over traditional single-sampled conversion results.



## MSP430 PORTFOLIO WITH ON CHIP ADCs

16-bit RISC MSP430 MCUs are the industry's lowest power solution for 8...16-bit battery-powered measurement applications including metering, portable instrumentation and intelligent sensing. The product line offers a wide range of catalog devices as well as Application Specific Standard Products (ASSP).

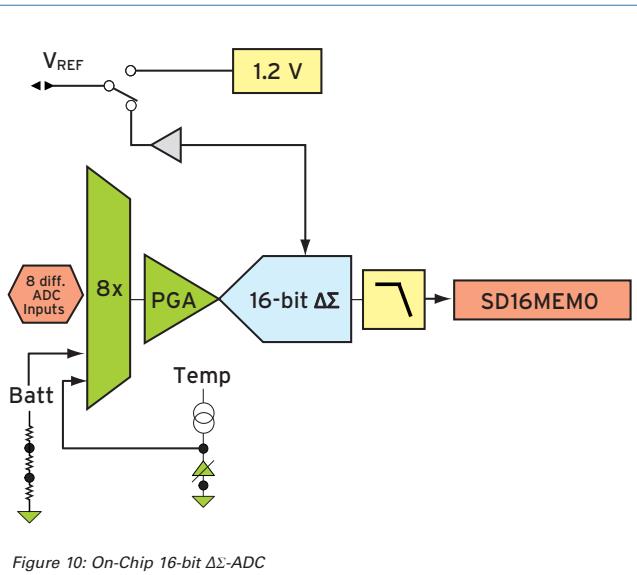


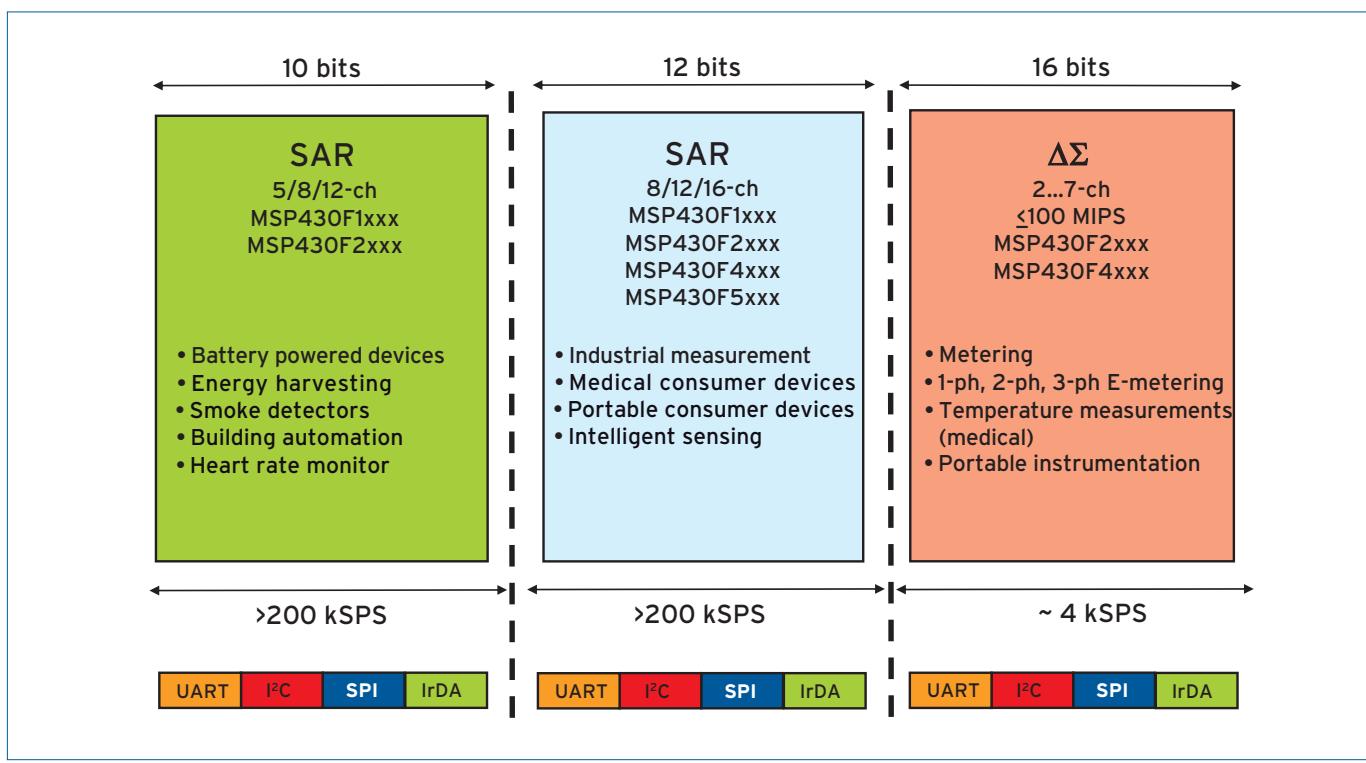
Figure 10: On-Chip 16-bit  $\Delta\Sigma$ -ADC

### Integrated High-Performance Analog Peripherals

- ADC10/ADC12: The ADC10/12 module supports fast, >200 ksp, 10 or 12-bit analog-to-digital conversions. The module features a 10 or 12-bit SAR core with 5/8/12 or 8/12/16 input channels respectively, sample select control, 1.5/2.5 V reference generator and internal temperature sensor. ADC10 features a data

transfer controller (DTC) and ADC12 features a 16-word conversion-and-control buffer. These added features allow samples to be converted and stored without CPU intervention.

- Comparator\_A/Comparator\_A+: The Comparator\_A/A+ module supports precision slope analog-to-digital conversions, supply voltage supervision and monitoring of external analog signals for accurate voltage and resistor value measurement. The module features a selectable reference voltage generator and input multiplexer. (Comp A+)
- DAC12: The DAC12 module is a 12-bit, voltage output DAC featuring internal or external reference selection, programmable settling time for optimal power consumption and can be configured in 8 or 12-bit mode. When multiple DAC12 modules are present, they may be grouped together for synchronous update operation.
- OA: The MSP430 integrated op-amps feature single-supply, low-current operation with rail-to-rail outputs and programmable settling times. Internal, programmable feedback resistors and connections between multiple op-amps allow for a variety of software-selectable configuration options including: unity gain mode, comparator mode, inverting PGA, non-inverting PGA, differential and instrumentation amplifier.
- SD16/SD16\_A: The SD16/SD16\_A module features up to three 16-bit  $\Delta\Sigma$  A/D converters with an internal 1.2 V reference. Each has up to seven fully differential multiplexed inputs including a built-in temperature sensor. The converters are second-order oversampling  $\Delta\Sigma$  modulators with selectable oversampling ratios of up to 1024 (SD16\_A) or 256 (SD16).



## PRECISION DACs

### DAC8565

The DAC8565 is a low-power, voltage-output, four-channel, 16-bit DAC. The device includes a 2.5 V, 2 ppm/°C internal reference, giving a full-scale output voltage range of 2.5 V. The internal reference has an initial accuracy of 0.004% and can source up to 20 mA at the  $V_{REFH}/V_{REFOUT}$  pin. The device is monotonic, provides very good linearity and minimises undesired code-to-code transient voltages. The DAC8565 uses a versatile 3-wire serial interface that operates at clock rates up to 50 MHz. It is compatible with the standard SPI™, QSPI™, Microwire™ and DSP interfaces. The power consumption is 2.9 mW at 3 V, reducing to 1.5 µW in power-down mode.

The DAC8565 is drop-in and functionally compatible with the DAC7564 and DAC8164 and functionally compatible with the DAC7565, DAC8165 and DAC8564. All these devices are available in a TSSOP-16 package.

### DAC9881

The DAC9881 is an 18-bit, single-channel, voltage-output DAC. It features 18-bit monotonicity, excellent linearity, very low-noise and fast settling time. The on-chip precision output amplifier allows rail-to-rail output swing to be achieved over the full supply range of 2.7...5.5 V. The device supports a standard SPI serial interface with input data clock frequencies of up to 50 MHz. The DAC9881 requires an external reference voltage to set the output range of the DAC channel. A programmable power-on reset circuit is also incorporated into the device.

The DAC9881 provides low-power operation. To further save energy, power-down mode can be achieved by accessing the PDN pin, thereby reducing the current consumption to 25 µA at 5 V. Power consumption is 4 mW at 5 V, reducing to 125 µW in power-down mode. The DAC9881 is available in a 4 × 4 mm<sup>2</sup> QFN-24 package with a specified temperature range of -40...+105 °C.

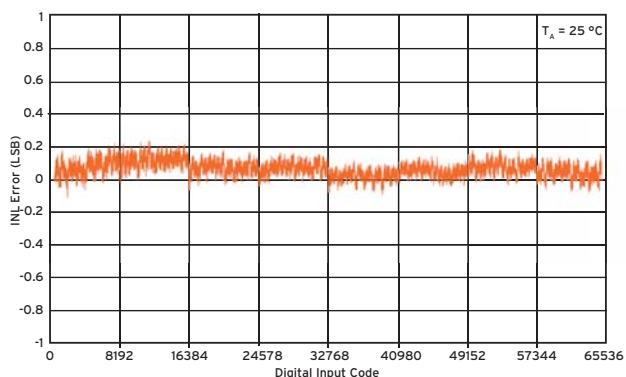


Figure 11: INL vs. Code for DAC9881

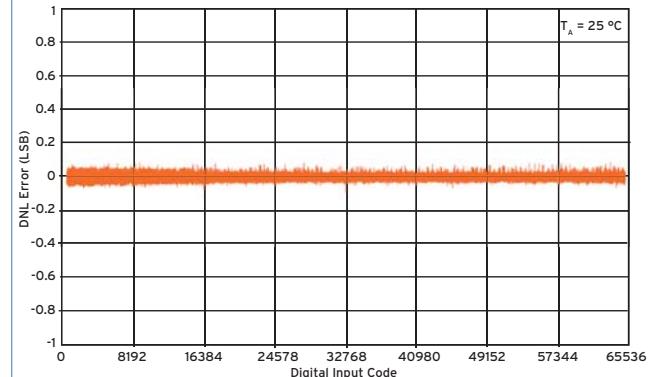
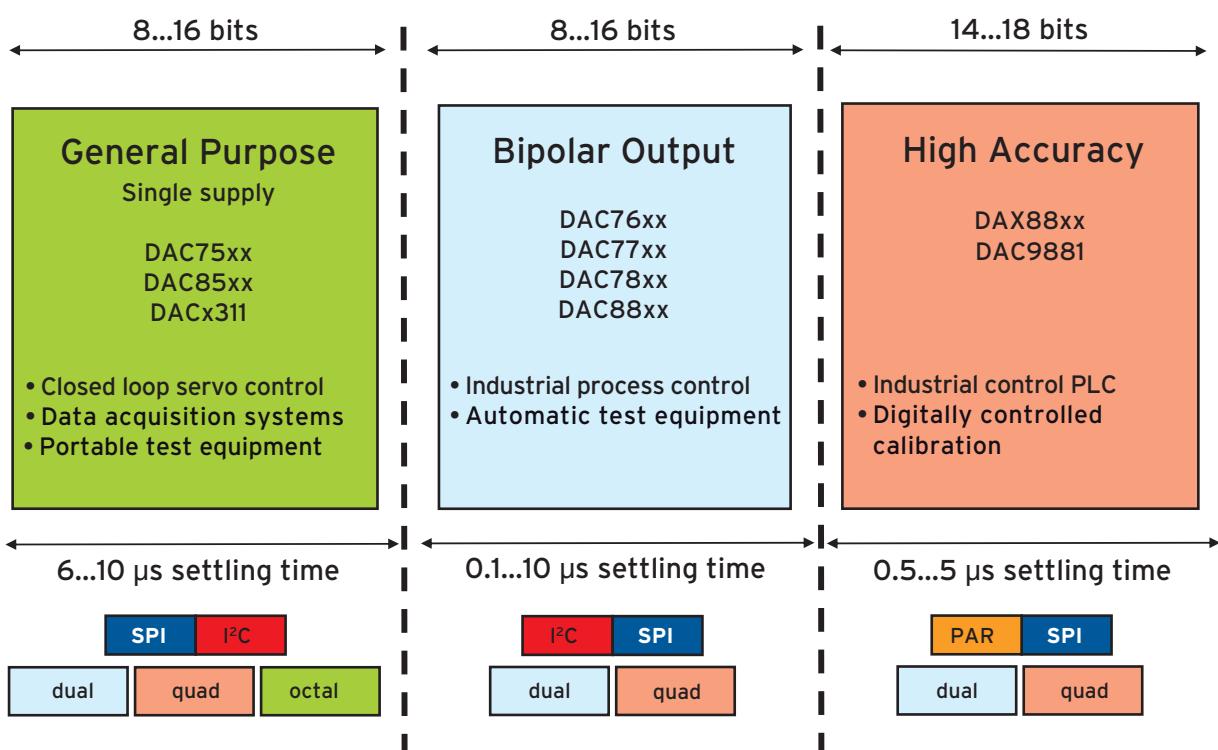


Figure 12: DNL vs. Code for DAC9881



## HIGH-SPEED DACS

### DAC5682Z

The DAC5682Z is a dual-channel 16-bit 1 GSPS DAC with wideband LVDS data input, integrated 2 x/4 x interpolation filters, on-board clock multiplier and internal voltage reference.

The DAC5682Z allows both complex or real output. An optional  $F_s/4$  coarse mixer in complex mode provides coarse frequency up conversion and the dual DAC output produces a complex Hilbert Transform pair. An external RF quadrature modulator then performs the final single sideband up-conversion.

The DAC5682Z is characterised for operation over the industrial temperature range of -40...+85 °C and is available in a 64-pin QFN package. Other single-channel members of the family include the interpolating DAC5681Z and non-interpolating DAC5681.

### DAC5688

The DAC5688 is a dual-channel 16-bit 800 MSPS DAC with dual CMOS digital data bus, integrated 2...8 x interpolation filters, a fine frequency mixer with 32-bit complex numerically controlled oscillator (NCO), on-board clock multiplier, IQ compensation and internal voltage reference.

The DAC5688 dual CMOS data bus provides 250 MSPS input data transfer per DAC channel. Input data can be interpolated 2 x, 4 x or 8 x by on-board digital interpolating FIR filters with over 80 dB of stop-band attenuation. The DAC5688 allows both complex or real output. An optional 32-bit NCO/mixer

in complex mode provides frequency upconversion and the dual DAC output produces a complex Hilbert transform pair. A digital Inverse SINC filter compensates for natural DAC  $\text{Sin}(X)/X$  frequency roll-off. The digital Quadrature Modulator Correction (QMC) feature allows IQ compensation of phase, gain and offset to maximise sideband rejection and minimise LO feed-through of an external quadrature modulator performing the final single sideband RF up-conversion.

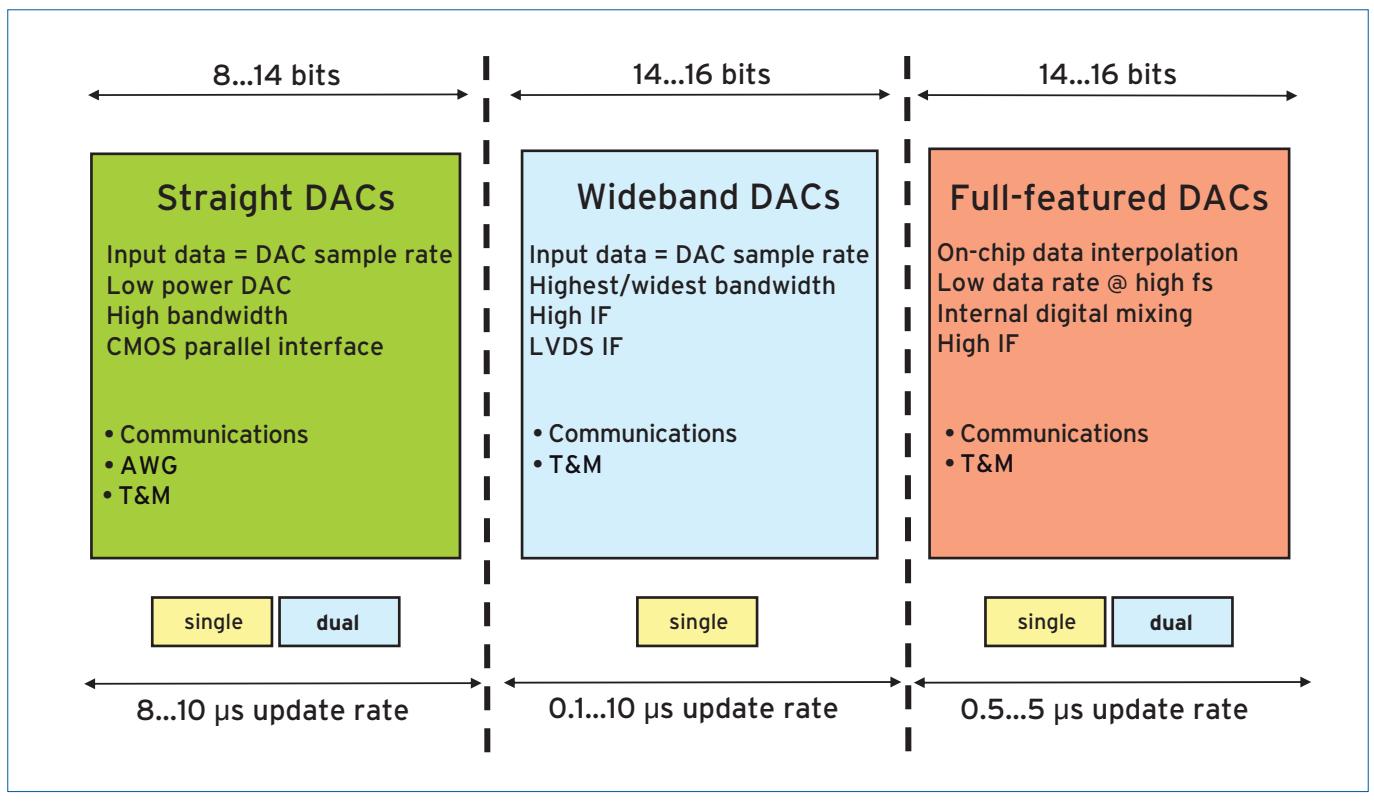
The DAC5688 is characterised for operation over the industrial temperature range of -40...+85 °C and is available in a 64-pin 9 x 9 mm QFN package.

### DAC5687

The DAC5687 is a dual-channel 16-bit high-speed DAC with integrated 2x, 4x and 8x interpolation filters, a complex Numerically Controlled Oscillator (NCO), onboard clock multiplier, IQ compensation and on-chip voltage reference. The DAC5687 is pin-compatible to the DAC5686, requiring only changes in register settings for most applications.

The coarse and fine mixers can be combined to span a wider range of frequencies with fine resolution. The DAC5687 allows both complex or real output. Combining the frequency upconversion and complex output produces a Hilbert transform pair that is output from the two DACs. An external RF quadrature modulator then performs the final single-sideband upconversion.

The IQ compensation feature allows optimisation of phase, gain and offset to maximise sideband rejection and minimise LO feedthrough for an analog quadrature modulator.



## ECODESIGN

The EcoDesign requirements for Energy using Products (EuP) directive came into force in August 2007 and provides a framework for setting EcoDesign requirements for any group of products which use energy. EcoDesign requirements for the first fifteen product groups are currently being drawn up, another five product groups are ongoing and the list of the next twenty five product groups to be targeted for action is currently being finalised. The first implementing measures are due in January 2008.

EcoDesign addresses the fundamental environmental impacts that a manufacturer has on society – the life cycle impacts of its products. It requires design teams to address how they can reduce environmental impacts and costs in materials selection, manufacture, packaging, use and end-of-life options. Companies that can demonstrate tangible improvements stand to gain marketing and reputational benefits with stakeholders.

EBV recognises it is not enough simply to comply with current laws and guidelines and aims to help customers remain one step ahead of them. Selected products from the different architectures on this page will not only meet your technical requirements but are especially up-to-date in terms of energy efficiency.



### ADS528x (Pipeline)

The ADS528x is a family of high-performance, low-power, octal channel ADCs. Available in either a  $9 \times 9 \text{ mm}^2$  QFN package or an HTQFP-80 package, with serialised LVDS outputs and a wide variety of programmable features, the ADS528x is highly customisable for a diversity of applications and offers an unprecedented level of system integration. The ADS528x family is specified over the industrial temperature range of -40...+85 °C.

### ADS8318 (SAR)

The ADS8318 is a 16-bit, 500-KSPS ADC. It operates with a 2.048...5.5 V external reference. The device includes a capacitor based, SAR ADC with inherent sample and hold. The devices include a 50 MHz SPI compatible serial interface. The interface is designed to support daisy chaining or cascading of multiple devices. The ADS8318 unipolar differential input

range supports a differential input swing of  $-V_{\text{REF}}$  to  $+V_{\text{REF}}$  with a common-mode of  $+V_{\text{REF}}/2$ . Device operation is optimised for very low-power operation and the power consumption directly scales with speed. This feature makes it attractive for lower speed applications. It is available in 10-pin MSOP and SON packages.

### ADS1281 ( $\Delta\Sigma$ )

The ADS1281 uses a fourth-order, inherently stable,  $\Delta\Sigma$ -modulator that provides outstanding noise and linearity performance. The modulator is used either in conjunction with the on-chip digital filter, or can be bypassed for use with post-processing filters. The digital filter consists of sinc and FIR low-pass stages followed by an IIR High-Pass Filter (HPF) stage. Selectable decimation provides data rates from 250...4000 Samples Per Second (SPS).

The FIR low-pass stage provides both linear and minimum phase response. The HPF features an adjustable corner frequency. On-chip gain and offset scaling registers support system calibration. Together, the modulator and filter dissipate only 12 mW. The ADS1281 is available in a compact TSSOP-24 package and is fully specified from -40...+85 °C, with a maximum operating range to +125 °C.

### DAC8311/8411

The DAC8311 (14-bit) and DAC8411 (16-bit) are low-power, single-channel, voltage output DACs. All devices use a versatile, 3-wire serial interface that operates at clock rates of up to 50 MHz and is compatible with standard SPI, QSPI, MICROWIRE and DSP interfaces.

The DAC8311 and DAC8411 contain a power-down feature, accessed over the serial interface that reduces current consumption of the device to 0.1  $\mu\text{A}$  at 1.8 V in power down mode. The low power consumption of this part in normal operation makes it ideally suited for portable, battery-operated equipment. The power consumption is 0.55 mW at 5 V, reducing to 2.5  $\mu\text{W}$  in power-down mode.

These devices are pin-compatible with the DAC5311, DAC6311, and DAC7311, offering an easy upgrade path from 8/10/12-bit resolution to 14/16-bit. All devices are available in a small, 6-pin, SC70 package. This package offers a flexible, pin-compatible and functionally-compatible drop-in solution within the family over an extended temperature range of -40...+125 °C.



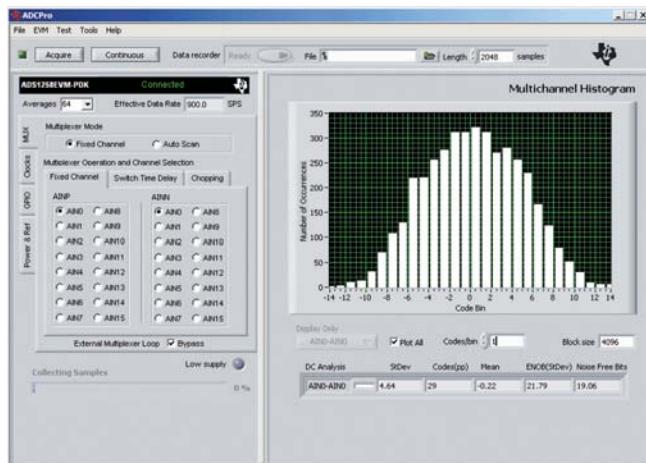
## TOOLS

### ADCPro™

ADCPro is a modular software system for evaluating ADCs without the need for expensive logic analysers and complex analysis routines. Used alone it is suitable for performing analysis on data sets captured from ADC testing; when paired with a Texas Instruments ADC Evaluation Module (EVM) and suitable data capture card, it becomes part of a powerful evaluation package.

There are DC and AC parameters for ADCs – and several different possible ways of testing these parameters. Following the IEEE1241-2000 standard, one can use a simple sine wave input and view collected time-domain, histogram, or FFT data. Using these three methods together will give a good indication of what the ADC transfer characteristics are.

Weblink: <http://www.ti.com/adcpro>



### Signal Chain Prototyping System

When you consider an ADC or DAC for your design, you can get a rapid assessment of the device with an Evaluation Module (EVM). With TI's modular EVM system, you can put together a complete data acquisition system, including signal conditioning and a processor, in just a few minutes. The modular EVM boards go together easily thanks to standardised connectors. You can also build your own modules to fit this system, if a standard TI EVM is not available.

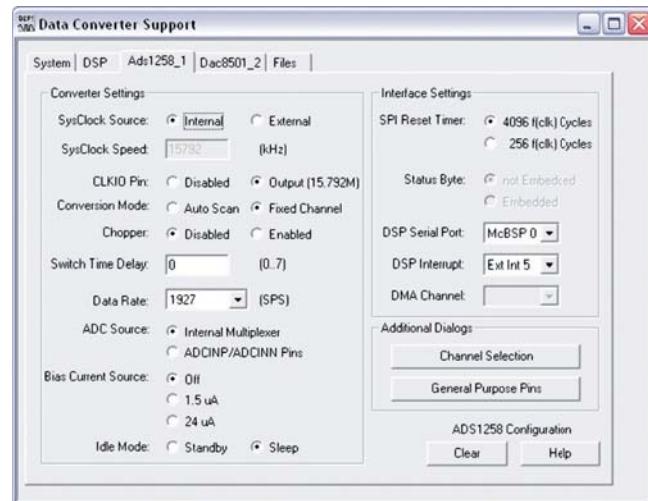
The signal chain prototyping system currently consists of several signal conditioning boards, tons of data converter EVMs and a couple of interface boards to connect the system to the DSP platforms of your choice.

### Data Converter Support Tool

The data converter support tool is a free development tool that allows the easy creation of initialisation data and interface software for TI data converters from within the IDE of code composer studio. It allows fast and easy 'point and click' data converter configuration and interface software generation, preventing illegal combinations of settings, as only valid entries are shown and any numerical inputs are checked against the data sheet parameters.

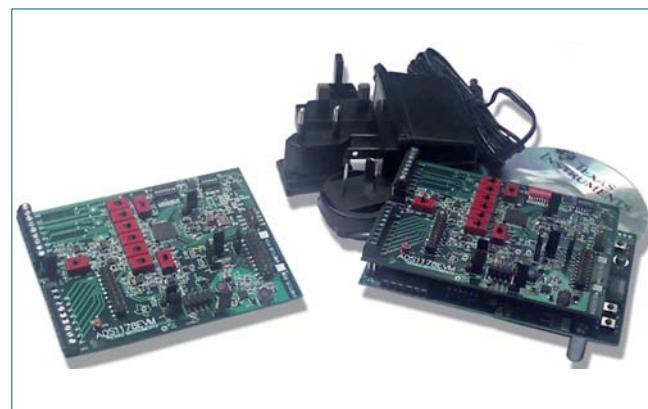
This well-documented C-source code contains all the functions necessary to talk to the external data converter, to setup the peripherals of the DSP and all of the registers internal to the data converter. The minimum function set includes read/write functions, initialisation functions and data structures and some device-specific functions to control specific features of the device. The generated code is to a great extend hardware independent, so it can be used together with the analog EVMs from TI's modular EVM system, the DSP starter kits or with customer specific hardware.

Weblink: <http://www.ti.com/dcplug-in>



### ADS1178 Performance Demonstration Kit (PDK)

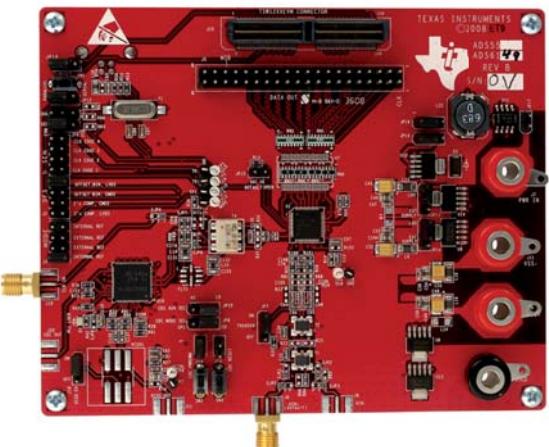
The ADS1178EVM-PDK is a complete evaluation/demonstration kit, which combines ADS1178EVM with the DSP-based MMB0 board as a motherboard. The mother board and the ADCPro evaluation software are supplied for use with a personal computer running Microsoft™ Windows XP operating system. This combination of boards allows the complete evaluation of the ADS1178 device. The MMB0 motherboard allows the ADS1178EVM/ADS1278EVM to be connected to the computer via an available USB port.



### ADS6149 Eval Board

The ADS6149EVM provides an environment to test the ADS6149 under a variety of clock, input and supply conditions. The EVM also includes TI's new 10 output low jitter clock synchroniser and jitter cleaner device, the CDCE72010, which can be used to drive the clocking input to the ADS6149. Open

sockets are provided for an external  $V_{CXO}$  and crystal band pass filter allowing for rapid evaluation of a combined high performance ADC and clocking circuit equivalent to a final system level solution. Alternatively an external clock source can be provided to the EVM and either routed through the CDCE72010 or passed directly to the ADS6149 clock input. The evaluation module also allows designers to use either a transformer coupled input into the ADC or an amplifier input based on the TI's THS4509. While the ADC EVM comes with the THS4509, users can easily evaluate any of the footprint compatible ADC driving amplifiers such as the THS4508, THS4511, THS4520.



#### ADS1232REF

Built around an ultra-low-power MSP430F449 MCU, this fully functional weigh scale board can be used by itself, powered from a 9 V battery. The LCD display and simple push buttons provide an easy-to-use interface that allows you to calibrate the scale, adjust for tare and make measurements in several different units of weight (grams, ounces, pounds, etc). A USB interface allows the board to connect to a PC and the data collected can be viewed and analysed with the included software. All source code for the firmware and software, as well as the PCB design files, are included.



#### TSW3070EVM

The development kit simplifies the complexity of interfacing between high-speed DACs and amplifiers and includes clocking and power management devices to further ease design and reduce cycle time. The TSW3070 development kit includes the following:

- DAC5682Z dual-channel, 1 GSPS DAC with current sink output
- OPA695 current feedback amplifier with 1.4 GHz bandwidth
- THS3091/5 high voltage swing amplifier with 30 V supply voltage
- CDCM7005 jitter cleaner with 800 MHz  $V_{CXO}$  and 10 MHz reference
- TPS7675x, TPS5430, UCC284-5 on board voltage supply

In addition, the kit also features a user-friendly GUI for easy DAC configuration. Designers can drive the DAC output to either the OPA695 or the THS3091/5, enabling customers to evaluate a high-frequency signal to support wide bandwidth or a large signal swing. As an additional option, designers can bypass the amplifiers and send the signal to a passive transformer output without gain.

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