

FIR Filter Coefficient Design Examples For the AFEDRI8201 in Digital Radio

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High-Speed Products

ABSTRACT

The AFEDRI8201 analog front end chip is an IF analog-to-digital converter for AM/FM/HD/DAB/digital radio systems. This article explains how the AFEDRI8201 can support applications such as HD radio $^{\text{TM}}$, Eureka DAB, and ISDB- T_{SB} . In addition, an actual AFEDRI8201 register configuration example is described.

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ScopeFIR is a trademark of lowegian International Corporation. HD radio is a trademark of iBiquity Digital Corporation.



1 Introduction

Three major systems have been recently emerging in the field of terrestrial-based digital sound broadcasting: high-definition (HD) radio, digital audio broadcasting (DAB), and Integrated Services Digital Broadcasting for Terrestrial Sound Broadcasting (ISDB-T_{SB}).

HD radio systems employ In-Band On-Channel (IBOC) technology to introduce digital sound broadcasting (DSB) services. HD radio upgrades the widely-used analog FM standard by delivering enhanced audio fidelity, improved signal robustness, and expanded auxiliary services. IBOC technology allows radio providers to add these new functions without the need for changing spectrum allocations. HD radio stations broadcast the same programming in analog and digital formats on the existing FM band.

The Eureka DAB system has been actively supported by the European Broadcasting Union (EBU) in light of the introduction of digital sound broadcasting services in Europe in 1995. Since 1998, the system has been successfully demonstrated and extensively tested in Europe, Canada, and the United States of America and in other countries worldwide.

The ISDB-T_{SB} system is designed to provide the Japanese consumer market with high-quality sound and data broadcasting, with high reliability even in mobile reception. The system is also designed to provide flexibility, expandability, and commonality for multimedia broadcasting using terrestrial networks.

Digital sound broadcasting systems that broadcast to vehicular, portable and fixed receivers will require many new digital radio receivers. A digital radio receiver consists of an antenna, tuner, low-noise amplifier (LNA), analog mixer, analog filter, IF analog digital converter, digital quadrature mixer, digital filters and a baseband processor.

The AFEDRI8201 is designed as a general-purpose analog front end chip to operate at the front end of newer digital radio receivers. The purpose of the AFEDRI8201 is to digitize the IF signal and generate I and Q signals by a quadrature mixer, as well as digitally down-convert an IF radio signal to baseband. The baseband processor (TI's DRI350 digital signal processor, or DSP) will further process the digitized signal into the desired information.

The AFEDRI8201 consists of a high-speed (80MSPS) analog-to-digital converter (ADC), digital down-converter and several digital filters (CIC, FIR). The cascaded integrator-comb (or CIC) is a fifth-order CIC filter. The first finite-impulse response (FIR) consists of a 16-bit wide filter coefficient memory bank so that up to 64 coefficients can be stored in memory. The second FIR can be configured up to 251 taps. The first and second FIR can also be interleaved.

The valid range for the CIC decimation ratio is from 8 to 1024. Both FIR1 and FIR2 contribute a fixed decimation 2, so the total decimation ratio of the AFEDRI8201 can be configured from 32 to 4096. The required input bandwidth of the AFEDRI8201 IF signal will determine the choice of the decimation ratio.

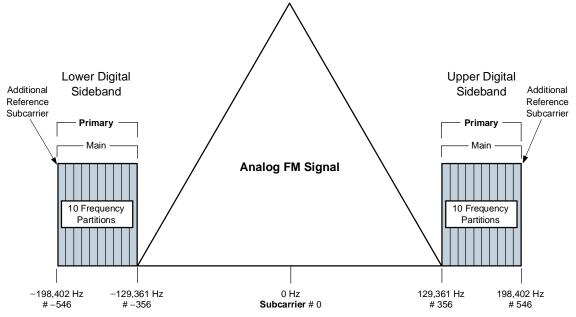
When the decimation ratio is set, the next step is to decide the length of the FIR1 and FIR2 filters as well as to design the coefficients of those filters. In the following sections, the coefficients are designed as examples for HD, DAB and ISDB-T_{SR} applications.



2 AFEDRI8201 FIR Coefficients Design Example for HD Radio Receiver

HD radio can simultaneously broadcast analog and digital signals across the existing FM band. This radio system offers enhanced audio quality and new data broadcasting services.

The hybrid waveform spectrum—service mode MP1 is shown in Figure 1.



A The level of the digital sub-carriers is such that the total power of these carriers is 20dB below the nominal power of the FM analog carrier.

Figure 1. Hybrid Waveform Spectrum—Service Mode MP1

To configure an AFEDRI8201 for an HD radio receiver, one can assume the baseband –3dB bandwidth is 284kHz, which is slightly wider than the bandwidth of IBOC DSB mode MP1 shown in Figure 1. If the sample clock sample rate is 80MSPS, and total decimation is chosen as 80, for example, then the CIC decimation ratio rate is DEC_CIC = 20, and the decimation ratio of the subsequent FIR1 and FIR2 filters is 4. The CIC scale = 42 and CIC shift = 22 can be calculated by Equation 1 and Equation 2. The CIC filter gain is then calculated as 1.001358 using Equation 3.

$$SHIFT = 5 \cdot log_{DEC_CIC} 2$$
 (1)

$$SCALE = 32 \cdot \frac{2^{SHIFT}}{DEC_CIC^5}$$
 (2)

$$GAIN = DEC_CIC^{5} \frac{SCALE/32}{2^{SHIFT}}$$
(3)

If one designs FIR1 = 62 taps and FIR2 = 151 taps, the FIR1 and FIR2 coefficients can be calculated by many different algorithms, such as ScopeFIR™ software by Iowegian (www.iowegian.com) which designs Finite Impulse Response (FIR) filters using the Parks-McClellan algorithm.

We have calculated an optimized cascaded FIR1 and FIR2 response with FIR1 = 62 taps and FIR2 = 151 taps. The calculated coefficients results are as shown in Table 1.

The resulting FIR1 filter gain is 0.999969 and the FIR2 filter gain is 0.999847. The total gain of the cascaded CIC, FIR1 and FIR2 filters is very close to 1.

The technique to configure the FIR coefficients registers in AFEDRI8201 can be found in the AFEDRI8201 register configuration section (see Section 5).



The cascaded filter performance of CIC, FIR1 and FIR2 using these coefficients is shown in Figure 2.

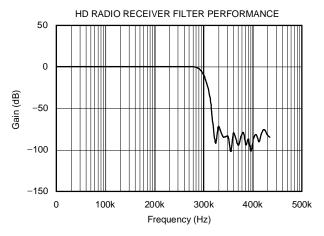


Figure 2. Cascaded Filter Gain vs Frequency for HD Radio Receiver

Table 1. Coefficient Examples for HD Radio Application

COEFFICIENT NO.	FIR2 (i = 1 TO 76)	FIR1 (i = 1 TO 31)
1	0	0
2	0	0
3	0	-1
4	0	0
5	0	6
6	1	6
7	0	-10
8	–1	-23
9	-2	0
10	-2	45
11	0	37
12	3	-49
13	4	-103
14	2	0
15	-3	167
16	-7	129
17	-5	-160
18	2	-319
19	10	0
20	11	475
21	3	356
22	-11	-432
23	-19	-847
24	-12	0
25	8	1267
26	26	976
27	25	-1247
28	2	-2687
29	-29	0
30	-41	6549



Table 1. Coefficient Examples for HD Radio Application (continued)

COEFFICIENT NO.	FIR2 (i = 1 TO 76)	FIR1 (i = 1 TO 31)
31	-20	12248
32	24	
33	56	
34	46	
35	-6	
36	-64	
37	-78	
38	– 27	
39	57	
40	108	
41	75	
42	-29	
43		
44	-133	
45	-133 -27	
46	121	
47	191	
48	109	
49	-80	
50	-233	
51	-213	
52	-7	
53	239	
54	323	
55	145	
56	-187	
57	-417	
58	-330	
59	56	
60	464	
61	549	
62	176	
63	-424	
64	-783	
65	-537	
66	241	
67	1006	
68	1083	
69	198	
70	-1190 -2022	
71	-2033	
72	-1298	
73	1312	
74	5020	
75	8275	
76	9568	



3 FIR Coefficients Design Example for DAB Radio Receiver

The standard spectrum of the DAB system for transmission Mode II is illustrated in Figure 3 . The out-of-band radiated signal spectrum in any 4kHz band should be constrained by one of the masks defined in Figure 4. The solid line mask should apply to VHF transmitters in critical areas for adjacent channel interference. The dotted line mask should apply to VHF transmitters in other circumstances and to UHF transmitters in critical cases for adjacent channel interference.

The level of the signal at frequencies outside the normal 1.536MHz bandwidth can be reduced by applying an appropriate filter, such as the digital FIR implemented in the AFEDRI8201.

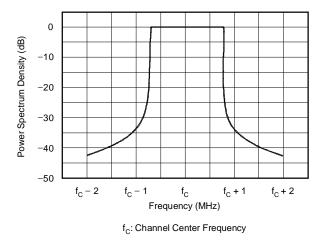


Figure 3. Theoretical Transmission Signal Spectrum for Transmission Mode II of System A



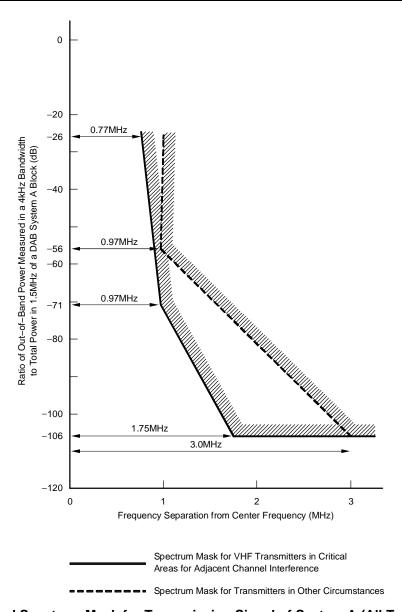


Figure 4. Out-of-Band Spectrum Mask for Transmission Signal of System A (All Transmission Modes)



To configure the AFEDRI8201 registers for a DAB receiver application, we presume that the passband is equal to 768KHz, and that the ripple is less than 1dB. In addition, the sample clock is set to 73.728MSPS, total decimation is chosen as 36, and the CIC decimation ratio rate (DEC_CIC) is 9. Thus, the CIC scale is 36 and the CIC shift is 16, as calculated from Equation 1 and Equation 2.

The cascaded performance of the CIC, FIR1 and FIR2 filters is shown in Figure 5. The attenuations are –0.1dB at 0.7MHz, –73dB at 0.97MHz and –110dB at 1.750MHz, respectively.

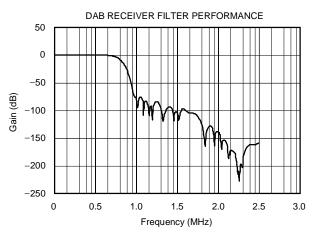


Figure 5. Cascaded Filters Gain vs Frequency for DAB Receiver

If setting the FIR1 filter equal to 28 taps, and the FIR2 filter equal to 64 taps, the FIR1 and FIR2 coefficients can then be calculated according to Table 2.



Table 2. Coefficient Examples for DAB Radio Receiver Application

COEFFICIENT NO.	FIR2 (i = 1 TO 32)	FIR1 (i = 1 TO 14)
1	0	0
2	0	-1
3	-1	-18
4	0	-41
5	5	6
6	6	177
7	-7	322
8	-21	76
9	-7	-712
10	35	-1406
11	45	-692
12	-20	2268
13	- 95	6586
14	-52	9822
15	107	
16	176	
17	-13	
18	-278	
19	-218	
20	225	
21	510	
22	104	
23	-652	
24	- 702	
25	357	
26	1348	
27	631	
28	-1569	
29	-2529	
30	446	
31	6679	
32	11875	



4 FIR Coefficients Design Example for ISDB-T_{SB} Receiver

The ISDB-T_{SB} system is designed to provide high-quality sound and data broadcasting, with high reliability even in mobile reception. The system is also designed to enable flexibility, expandability, and commonality for multimedia broadcasting using terrestrial networks. The system shares the physical layer characteristics with the ISDB-T system for digital terrestrial television broadcasting.

ISDB- T_{SB} is a narrowband system. Therefore, broadcasters can have their own RF channel which allows them to independently select transmission parameters. Single-segment bandwidth is defined to be 429kHz (6/14MHz), 500 kHz (7/14MHz) or 571kHz (8/14MHz). However, the segment bandwidth should be selected in compliance with the frequency situation in each country.

The ISDB- T_{SB} system adopts BST-OFDM, and consists of one or three OFDM segments (that is, single-segment and triple-segment transmission). If the bandwidth of single-segment transmission is presumed to be approximately 500kHz, the bandwidth of single-segment transmission and triple-segment transmission is approximately 500kHz and 1.5MHz, respectively.

The radiated signal spectrum of triple-segment transmission for a 6/14MHz segment system should be constrained by the mask defined in Figure 6 and Table 3. The level of the signal at frequencies beyond the 650kHz bandwidth can be reduced by applying an appropriate filter.

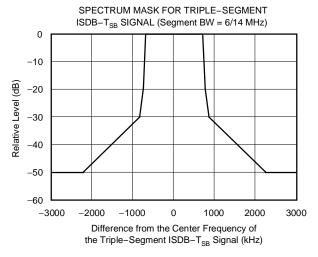


Figure 6. Spectrum Mask for Triple-Segment ISDB-T_{SB} Signal (Segment BW = 6/14MHz)

Table 3. Breakpoints of the Spectrum Mask for Triple-Segment Transmission (Segment BW = 6/14MHz)

DIFFERENCE FROM THE CENTER FREQUENCY OF THE TERRESTRIAL DIGITAL SOUND SIGNAL (kHz)	ITU-R BS.1114-2 RECOMMENDED RELATIVE LEVEL (dB)	ATTENUATION LEVEL BY CIC, FIR1, AND FIR2 IN THE AFEDRI8201 (dB)
±650	0	0
±720	-20	-40
±790	-30	-70
±2220	-50	-100

The FIR filters of the AFEDRI8201 can be configured for either ISDB-T_{SB} single- or triple-segment transmission bandwidth with a segment of 429kHz (6/14MHz), 500kHz (7/14MHz) or 571kHz (8/14MHz).

The FIR filters designed below are for a triple-segment transmission application with a segment of 429kHz (6/14 MHz). The triple-segment bandwidth is ($3 \times 429 \text{kHz}$) = 1.287MHz, which results in a 650 kHz base-bandwidth. The ripple can be designed to be less than 1dB within a 650 kHz baseband; some breakpoint attenuation levels are listed in Table 3.



Given that –3dB bandwidth is around 676kHz, the clock rate is 73.14MHz (or 512MHz/7), the total decimation is 36 and the CIC decimation ratio is 9. The CIC scale is then 36 and the CIC shift is 16, as calculated from Equation 1 and Equation 2.

Figure 7 shows the cascaded filter performance of the CIC, FIR1 and FIR2 filters.

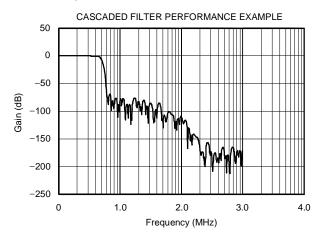


Figure 7. Cascaded Filters Gain vs Frequency for ISDB-T_{SB} Receiver

If setting the FIR1 filter equal to 28 taps, and the FIR2 filter equal to 127 taps with extended length mode, the FIR1 and FIR2 coefficients can then be calculated according to Table 4.

Table 4. Coefficient Examples for ISDB-T_{SB} Application

COEFFICIENT NO.	FIR2 (i = 1 TO 64)	FIR1 (i = 1 TO 14)
1	0	0
2	0	4
3	0	12
4	0	-24
5	0	-108
6	-1	-71
7	-2	256
8	-1	552
9	2	42
10	4	-1305
11	2	-1749
12	-4	952
13	-7	6534
14	-3	11286
15	7	
16	12	
17	4	
18	-13	
19	-20	
20	-4	
21	22	
22	29	
23	3	
24	-36	
25	-42	



Table 4. Coefficient Examples for ISDB-T_{SB} Application (continued)

COEFFICIENT NO.	FIR2 (i = 1 TO 64)	FIR1 (i = 1 TO 14)
26	1	
27	54	
28	57	
29	-7	
30	–7 9	
31	- 75	
32	19	
33	113	
34	96	
35	-37	
36	-156	
37	–119	
38	65	
39	212	
40	144	
41	-106	
42	-284	
43	-169	
44	165	
45	377	
46	195	
47	-251	
48	-498	
49	– 219	
50	376	
51	664	
52	241	
53	-569	
54	-912	
55	-259	
56	901	
57	1339	
58	273	
59	-1607	
60	-2348	
61	-281	
62	4350	
63	9162	
64	11206	



5 AFEDRI8201 Register Configuration

This section describes how to configure the data interface DIV, MODE, NCO, CIC, FIR1, and FIR2 registers of the AFEDRI8201 by using a simple function test setup.

5.1 FIR Coefficients Design Example for a Function Test

For this example, we assume that one digital radio application needs a system clock sample rate of 80MSPS, with a baseband width of 284kHz; the IF = 10.7MHz, the total decimation ratio is 80, and the CIC decimation ratio is 20. We can then set the data interface DIV = 0; data output mode = 1; FIR1 to EVEN mode = 1; NCOEFF = 9; FIR2A to NCOEFF = 31, and MODE = 1. We also set FIR1 and FIR2 into non-interleaved mode. All AFEDRI8201 registers can then be configured as shown in the subsequent example (see Section 5.2).

The cascaded filter performance of the CIC, FIR1 and FIR2 filters is shown in Figure 8. The FIR1 and FIR2 coefficients are calculated as shown in Table 5.

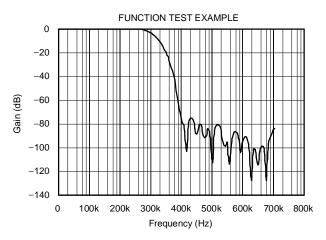


Figure 8. Cascaded Filters Gain vs Frequency for Function Test

COEFFICIENT NO.	FIR2 (i = 1 TO 31)	FIR1 (i = 1 TO 9)
1	–1	-12
2	-3	0
3	-2	175
4	5	-253
5	13	-521
6	9	-1606
7	-13	0
8	-37	5975
9	-29	12125
10	24	
11	83	
12	74	
13	-34	
14	-160	
15	-160	
16	32	
17	279	
18	315	

Table 5. Coefficient Examples for a Function Test



COEFFICIENT NO.	FIR2 (i = 1 TO 31)	FIR1 (i = 1 TO 9)
20	-454	
21	-583	
22	– 97	
23	714	
24	1063	
25	339	
26	-1155	
27	-2106	
28	-1047	
29	2394	
30	6880	
31	10040	

Table 5. Coefficient Examples for a Function Test (continued)

5.2 Example AFEDRI8201 Function Test Control Register and Memory Settings

The following example shows how to write control register and memory instructions into the AFEDRI8201 registers of DIV, MODE, NCO, CIC, FIR1, and FIR2.

```
/* Control Register settings */
Register write instruction [0]=0x8000; /* Write Control Register 0 */
 data[0]=0x0001; /* MCLK DIV=0, Data Out MODE=1 */
 /* NCO frequency of 10.80078125 MHz, code = 0x22900000 */
 Register write instruction [1]=0x8100; /* Write Control Register 1 */
 data[1]=0x0000; /* NCO FREQUENCY bits 15-0 */
 Register write instruction [2]=0x8200; /* Write Control Register 2 */
 data[2]=0x2290; /* NCO FREQUENCY bits 31-16 */
 Register write instruction [3]=0x8300; /* Write Control Register 3 */
 data[3]=0x0000; /* NCO PHASE bits 15-0 */
 Register write instruction [4]=0x8400; /* Write Control Register 4 */
 data[4]=0x0000; /* NCO PHASE bits 31-16 */
 Register write instruction [5]=0x8500; /* Write Control Register 5 */
 data[5]=0x0014; /* CIC DECIMATION_RATE=20 */
 Register write instruction [6]=0x8600; /* Write Control Register 6 */
 data[6]=0x0a56; /* SCALE=41, SHIFT=22 */
 Register write instruction [7]=0x8700; /* Write Control Register 7 */
 Register write instruction [8]=0x8800; /* Write Control Register 8 */
 data[8]=0x007d; /* BASE_ADDR=0, NCOEFF=31, FIR2A MODE=1 */
 Register write instruction [9]=0x8900; /* Write Control Register 9 */
 Register write instruction [11]=0x8b00; /* Write Control Register 11 */
 data[11]=0x0000; /* AUXILIARY DAC=0x000 */
 Register write instruction [12]=0x8c00; /* Write Control Register 12 */
 data[12]=0x0000; /* PGA GAIN=1, PWD=0 */
```



```
/* Coefficients for Filter 1 */
 Memory write instruction [0]=0xa000;
                                          data[0]=-12;
 Memory write instruction [1]=0xa001;
                                          data[1]=0;
                                          data[2]=175;
 Memory write instruction [2]=0xa002;
 Memory write instruction [3]=0xa003;
                                          data[3]=-253;
 Memory write instruction [4]=0xa004;
                                          data[4]=-521;
 Memory write instruction [5]=0xa005;
                                          data[5]=-1606;
 Memory write instruction [6]=0xa006;
                                          data[6]=0;
 Memory write instruction [7]=0xa007;
                                          data[7]=5975;
 Memory write instruction [8]=0xa008;
                                          data[8]=12125;
/* Coefficients for Filter 2A */
 Memory write instruction [0]=0xa100;
                                          data[0]=-1;
 Memory write instruction [1]=0xa101;
                                          data[1]=-3;
 Memory write instruction [2]=0xa102;
                                          data[2]=-2;
 Memory write instruction [3]=0xa103;
                                          data[3]=5;
 Memory write instruction [4]=0xa104;
                                          data[4]=13;
 Memory write instruction [5]=0xa105;
                                          data[5]=9;
 Memory write instruction [6]=0xa106;
                                          data[6]=-13;
 Memory write instruction [7]=0xa107;
                                          data[7]=-37;
                                          data[8]=-29;
 Memory write instruction [8]=0xa108;
 Memory write instruction [9]=0xa109;
                                          data[9]=24;
 Memory write instruction [10]=0xa10a;
                                          data[10]=83;
 Memory write instruction [11]=0xa10b;
                                          data[11]=74;
 Memory write instruction [12]=0xa10c;
                                          data[12]=-34;
 Memory write instruction [13]=0xa10d;
                                          data[13]=-160;
 Memory write instruction [14]=0xa10e;
                                          data[14]=-160;
 Memory write instruction [15]=0xa10f;
                                          data[15]=32;
 Memory write instruction [16]=0xal10;
                                          data[16]=279;
 Memory write instruction [17]=0xal11;
                                          data[17]=315;
 Memory write instruction [18]=0xa112;
                                          data[18]=0;
                                          data[19]=-454;
 Memory write instruction [19]=0xa113;
 Memory write instruction [20]=0xa114;
                                          data[20]=-583;
 Memory write instruction [21]=0xa115;
                                          data[21]=-97;
                                          data[22]=714;
 Memory write instruction [22]=0xal16;
 Memory write instruction [23]=0xa117;
                                          data[23]=1063;
 Memory write instruction [24]=0xa118;
                                          data[24]=339;
 Memory write instruction [25]=0xa119;
                                          data[25]=-1155;
 Memory write instruction [26]=0xalla;
                                          data[26]=-2106;
 Memory write instruction [27]=0xal1b;
                                          data[27]=-1047;
 Memory write instruction [28]=0xal1c;
                                          data[28]=2394;
 Memory write instruction [29]=0xalld;
                                          data[29]=6880;
 Memory write instruction [30]=0xalle;
                                          data[30]=10040;
  /* Coefficients for Filter 2B */
 Memory write instruction [0]=0xa200;
                                          data[0]=-1;
 Memory write instruction [1]=0xa201;
                                          data[1]=-3;
 Memory write instruction [2]=0xa202;
                                          data[2]=-2;
 Memory write instruction [3]=0xa203;
                                          data[3]=5;
 Memory write instruction [4]=0xa204;
                                          data[4]=13;
 Memory write instruction [5]=0xa205;
                                          data[5]=9;
 Memory write instruction [6]=0xa206;
                                          data[6]=-13;
 Memory write instruction [7]=0xa207;
                                          data[7]=-37;
 Memory write instruction [8]=0xa208;
                                          data[8]=-29;
 Memory write instruction [9]=0xa209;
                                          data[9]=24;
 Memory write instruction [10]=0xa20a;
                                          data[10]=83;
 Memory write instruction [11]=0xa20b;
                                          data[11]=74;
 Memory write instruction [12]=0xa20c;
                                          data[12]=-34;
 Memory write instruction [13]=0xa20d;
                                          data[13]=-160;
 Memory write instruction [14]=0xa20e;
                                          data[14]=-160;
 Memory write instruction [15]=0xa20f;
                                          data[15]=32;
 Memory write instruction [16]=0xa210;
                                          data[16]=279;
 Memory write instruction [17]=0xa211;
                                          data[17]=315;
 Memory write instruction [18]=0xa212;
                                          data[18]=0;
 Memory write instruction [19]=0xa213;
                                          data[19]=-454;
                                          data[20]=-583;
 Memory write instruction [20]=0xa214;
```



```
Memory write instruction [21]=0xa215; data[21]=-97; Memory write instruction [22]=0xa216; data[22]=714; Memory write instruction [23]=0xa217; data[23]=1063; Memory write instruction [24]=0xa218; data[24]=339; Memory write instruction [25]=0xa219; data[25]=-1155; Memory write instruction [26]=0xa21a; data[26]=-2106; Memory write instruction [27]=0xa21b; data[27]=-1047; Memory write instruction [28]=0xa21c; data[28]=2394; Memory write instruction [29]=0xa21d; data[29]=6880; Memory write instruction [30]=0xa21e; data[30]=10040;
```

6 Conclusion

This article provides three FIR filter coefficient design examples and an actual AFEDRI8201 register configuration example. Together, these examples illustrate that the AFEDRI8201 is ideal for HD radio, Eureka DAB, and ISDB-T_{SB} terrestrial digital sound broadcasting systems.

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