Parity-Generate and Parity-Check Features for High-Bandwidth-Computing FIFO Applications

Tom Jackson
Advanced System Logic – Semiconductor Group

SCAA015A
March 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Contents

Introduction

Parity-generate and parity-check features are available in both the internetworking family of first-in, first-out memories (FIFOs), SN74ABT3614 and SN74ABT3613, and the high-bandwidth-computing family, SN74ABT3612 and SN74ABT3611. Parity generate and parity check are needed in high-bandwidth and high-speed computing applications where demanding data integrity levels are required. All of TI's 36-bit FIFOs have bidirectional mailbox registers that allow quick access to data by bypassing the FIFO static random-access memory (SRAM) core. The same input/output (I/O) is shared between the mailbox registers and the FIFO data registers that allow parity generate and parity check on both the FIFO memory data and the mailbox-register data. The parity-generate and parity-check features are designed for fault-tolerant systems, such as those in computing and telecom that require error-detection techniques, in addition to many of today's microprocessors that have provisions for parity detection.

Parity-Generate Feature

The parity-generate feature enables the user to generate odd or even parity in the most significant bit (MSB) of each byte on either port A or port B of the FIFO. Odd and even parity are defined as follows:

Odd parity: The parity bit is set to one for an even number of ones, including the parity bit.

Even parity: The parity bit is set to zero for an odd number of ones, including the parity bit.

Parity is generated for data reads from either port A or port B of a bidirectional FIFO by asserting parity generate A (PGA) and parity generate B (PGB), respectively (CSA/B low, PGA/B high, ENA/B high). In Figure 1, a write to a FIFO or mailbox register stores the levels applied to all 36 inputs, regardless of the state of the parity-generate input PGB. When data is written to a port, the lower eight bits of each byte are copied to the parity-generate tree. These bits are then used to generate a parity bit according to the level of the ODD/$\overline{\text{EVEN}}$ select pin (see Table 1). When PGB is asserted, the results of the parity generator are written to the MSB of the output register. If PGB is low, the original contents of the MSB of the byte under consideration are transferred to the corresponding location in the output register.

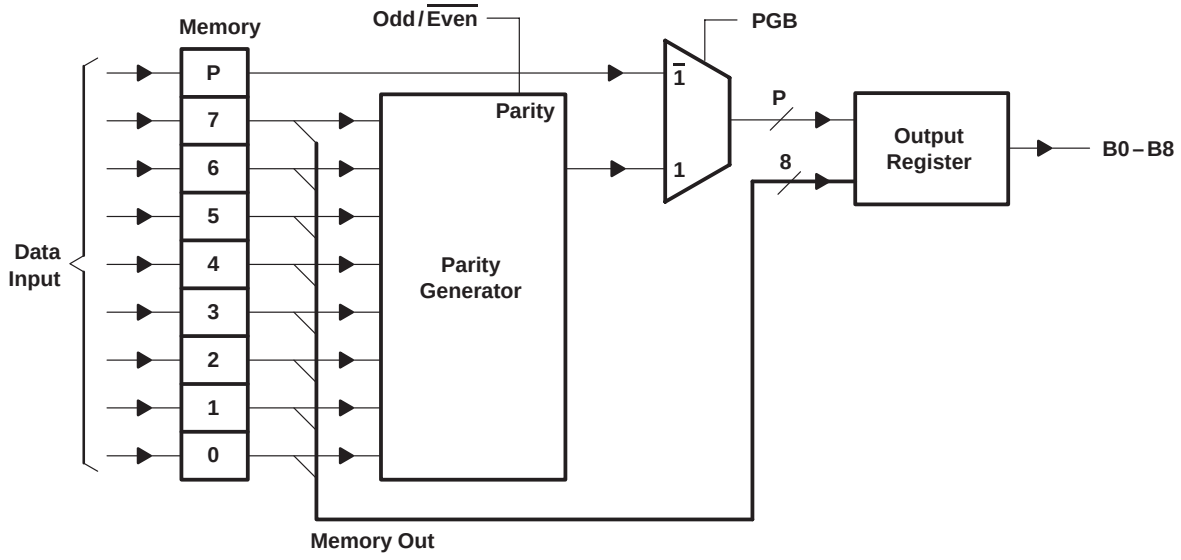

Figure 1. Parity-Generate Circuit

Table 1. Parity-Generate Input Pins

PACKAGE	PIN NUMBER		
	$\overline{\text{PEFA}}$	$\overline{\text{PEFB}}$	ODD/$\overline{\text{EVEN}}$
120-pin TQFP (PCB)	39	53	44
132-pin PQFP (PQ)	9	125	3

Each mailbox register has an associated parity-generate and check (gen/check) circuit (see Figure 2) that enables parity to be generated and checked on either port of the FIFO. The circuit that generates parity for the Mail1 mailbox register is shared by the port-B bus (B0–B35) and generates and checks parity for the FIFO data bus, as well as to check parity for the Mail2 mailbox register. The circuit that generates parity for the Mail2 mailbox register is shared by the port A bus (A0–A35) to check parity for FIFO data and mailbox register. The shared parity trees of a port generate parity bits for the data in a mailbox register when the port write/read select input is low, port-mail select input is high, and port-parity-generate select is high. Generating parity for mail register data does not change the contents of the register.

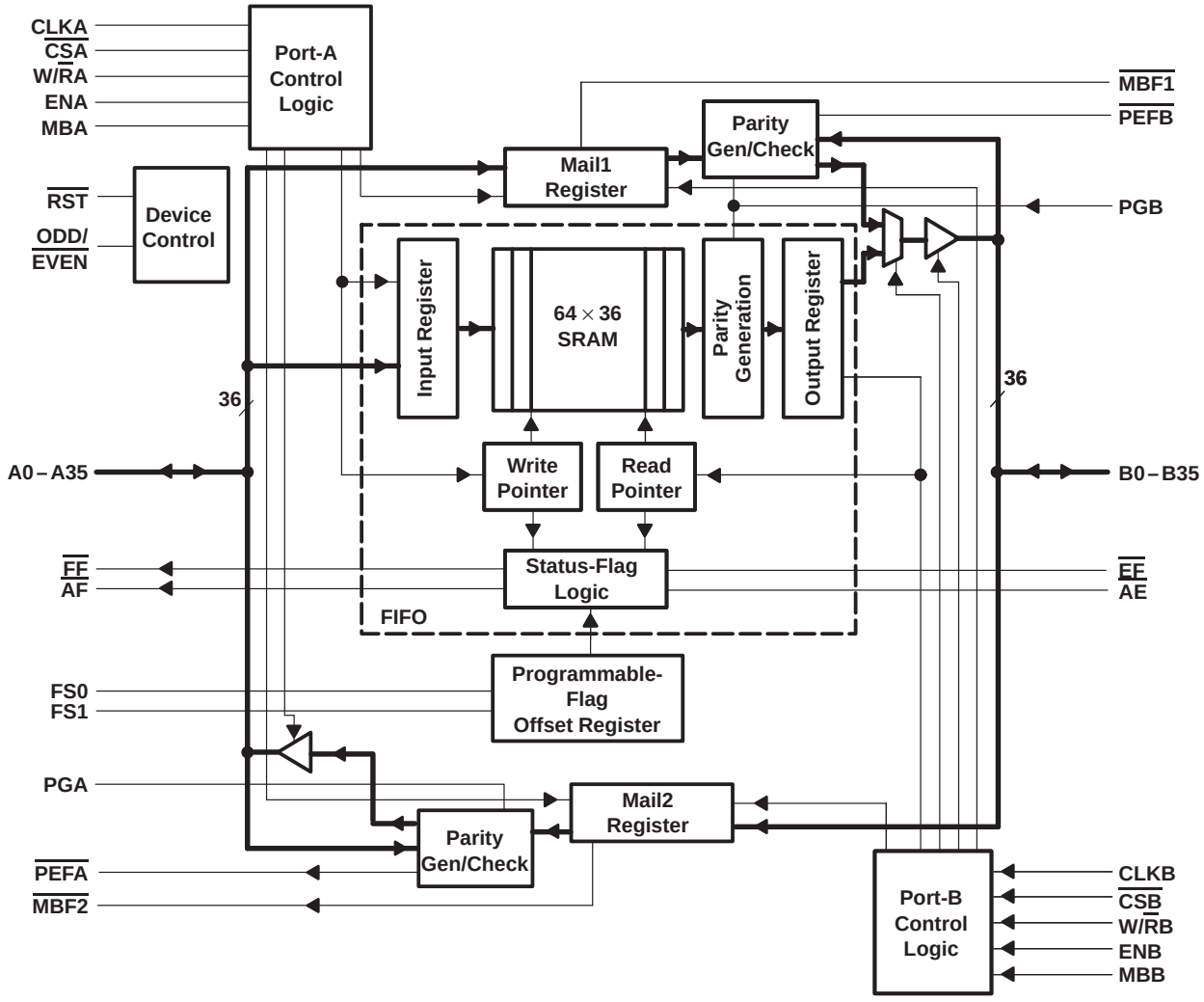

Figure 2. SN74ABT3611 Mailbox Registers and Associated Parity Gen/Check Circuits Functional Block Diagram

The parity-generate and parity-check features allow the user to select odd or even parity and to passively check the results of all incoming data to either port A or port B of the FIFO without disrupting normal operations. Both port A (A0–A35) inputs and

port B (B0–B35) inputs have four 9-bit parity trees to check the parity of incoming or outgoing data (see Figure 3). Parity is checked on the ninth MSB of each byte.

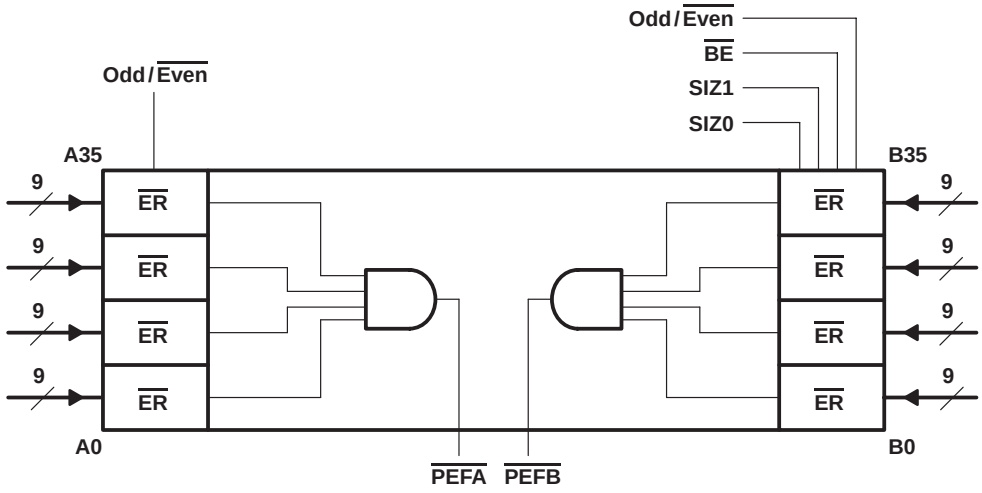

Figure 3. Parity Trees

A parity failure on one or more bytes of the input bus is indicated by a low level on the port parity-error flag ($\overline{\text{PEFA}}$, $\overline{\text{PEFB}}$) (see Table 2). The parity-error flags can be ignored if this feature is not desired.

Table 2. Parity-Error Input Pins

PACKAGE	PIN NUMBER		
	PGA	PGB	ODD/$\overline{\text{EVEN}}$
120-pin TQFP (PCB)	38	54	44
132-pin PQFP (PQ)	10	124	3

The user can choose odd or even parity by asserting the ODD/$\overline{\text{EVEN}}$ input or allow the FIFO to default to even parity. In this manner, the user can select the parity format that best fits the application requirements. Since four 9-bit parity trees are used, it is possible to implement the parity-check function on the bus-configuration port in conjunction with the bus-matching feature of the internetworking FIFOs. In this manner, any bus width that has been selected, 9-bit through 36-bit, can have parity checked. The parity-checking circuit is designed to ignore all error flags that may be generated on unused bytes.

As in parity generate, the four parity trees used to check the port-A inputs are shared by the Mail2 mailbox register. Port-B inputs on bidirectional FIFOs are shared by the Mail1 mailbox register (see Figure 2); therefore, parity errors are detected before the data is entered into the FIFO SRAM core.

Using Parity Error to Force an Exception

Although the parity-check feature is passive, it permits the designer to disregard data before it is written into the FIFO SRAM core. This type of functionality is easily implemented by the circuit shown in Figure 4. Since parity is checked on the inputs before being written to the FIFO, it is possible to capture the erred data and force an exception. Figure 4 shows a data error that has been detected by a low on $\overline{\text{PEFA}}$. The associated propagation delay, [$t_{pd(D–PE)}$] of a valid error flag is 10 ns for the –15 speed sort. This allows adequate time for a fast programmable logic device ($t_{pd\ PLD}$) to disallow a data write prior to the data becoming valid. If no parity error is detected, the data write is performed. If FIFOs with slower speed sorts (–20, –30) are used, the associated propagation delay is increased. This method eliminates the need for external counters to track the erroneous data through the FIFO to the output. By forcing an exception, the parity is captured and the clock cycle passes without writing the data to the FIFO memory core.

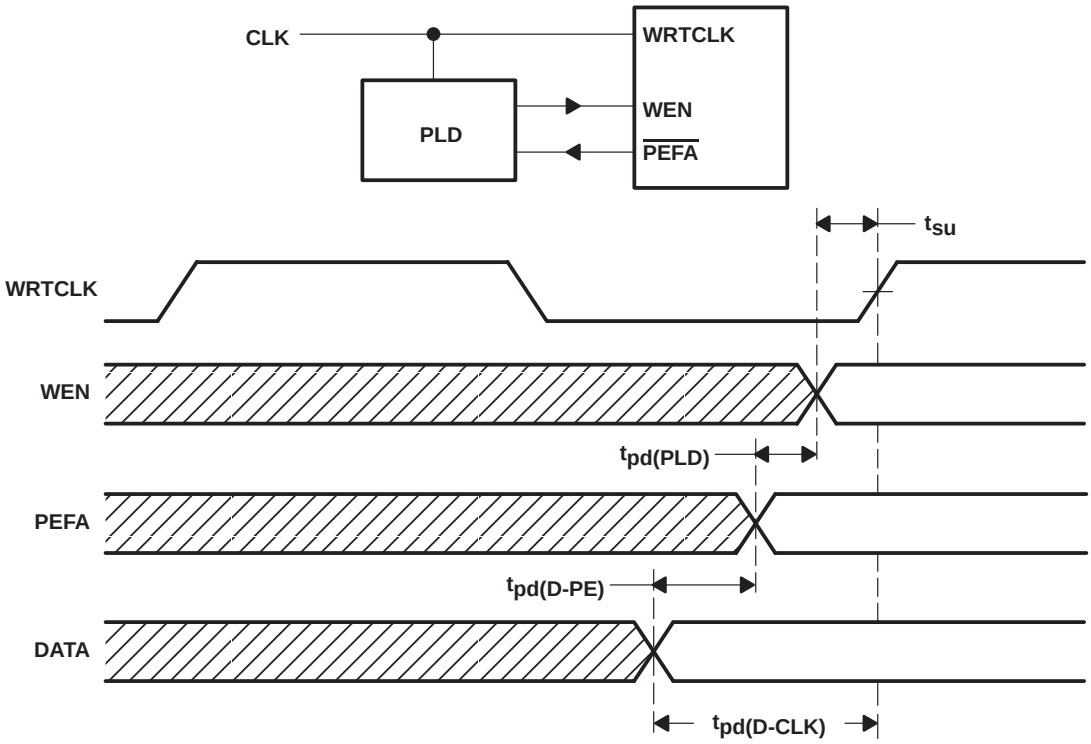

Figure 4. Parity-Error Exception Circuit

Conclusion

As systems become more integrated and bus speeds increase, there is a growing need to ensure data integrity. When parity generate or parity check is required by dynamic random-access memory (DRAM) refresh cycles, bus noise, or other card-to-card performance issues, TI's parity-generate and parity-check features provide a high-speed, space-saving alternative.