XIO2000A to XIO2001 Change Document

Connectivity

ABSTRACT

This document defines register and signal differences between the XIO2000A (literature number SCPS155) and XIO2001 (literature number SCPS212).

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1 Register Changes

Table 1 documents the changes in the PCI classic configuration space and the extended PCI configuration space.

Table 1. Register Changes

REGISTER NAME	COMMENTS
Power Management Capabilities Register (PCI offset 4Ah)	Bit Field Name: PM_VERSION=3 was 2 This bit field identifies the PCI Bus Power Management Interface Specification in which the device is compliant too. The default setting for this register has been changed to show revision 1.2 compliance.
Power Management Control/Status Register (PCI offset 4Ch)	Bit Field Name: NO_SOFT_RESET=1 was 0 The default setting for this bit was changed from 0 to 1 to indicate that no internal reset is generated and the device retains its configuration context when transitioning from the D3hot state to the D0 state.
PCI Express Capability Register (PCI offset 72h)	VERSION = 2 was 1 This bit field determines the PCI capability version. The value has been changed to reflect that the XIO2001 is compliant to the 2.0 PCI-Express base specification.
Device Capabilities Register (PCI offset 74h)	(bit 15) RBER = 1 was 0 The role-based error reporting bit was added to the Device Capabilities Register this bit is set to indicate that the XIO2001 implements the functionality originally defined in the Error Reporting ECN for *PCI Express Base Specifiation*, Revision 1.0a, and later incorporated into *PCI Express Base Specification*, Revision 1.1 and Revision 2.0.
Link Capabilities Register (PCI offset 7Ch)	CLK_PM=1 was 0 This bit indicates that the XIO2001 supports the $\overline{\text{CLKREQ}}$ protocol.
Link Control Register (PCI offset 80h)	CPM_EN bit 8 added (Clock Power Management Enable) Clock Power Management Enable bit. This bit is used to enable XIO2001 to use CLKREQ# for clock power management.
Expanded PCI Express Capability Structure (PCI offset 72h)	The PCI Express Capability structure was expanded to encompass nine new registers that were defined in the 2.0 PCI-Express Base Specification. The XIO2001 does not implement these registers since they are specific to 5.0Gb transfer rate which the XIO2001 does not support however register space must be allocated in the extended configuration address space to be compliant to software that is compliant to the 2.0 PCI-Express Base Specification. Six dwords of additional address space has been added starting at PCI offset A4h.
Pre-fetch Agent Request Limits Register (PCI offset E8h)	This new register contains three new bit fields that define the pre-fetch agent limits on retrieving data using upstream reads. The three new bit fields are: PFA_REQ_LENGTH_LIMIT: Determines the number of bytes in the thread that the pre-fetch agent will read for that thread. PFA_CPL_CACHE_MODE: Completion Cache Mode. Determines the rules for completing the caching process. PFA_REQ_CNT_LIMIT: Request Count Limit. Determines the number of pre-fetch reads that takes place in each burst.
Cache Timer Transfer Limit Register (PCI offset EAh)	The register is used to set the number of PCI cycle starts that have to occur without a read hit on the completion data buffer, before the cache data can be discarded.
Cache Timer Lower Limit Register (PCI offset ECh)	Minimum number of clock cycles that must have passed without a read hit on the completion data buffer before the “cache miss limit” check can be triggered.
Cache Timer Upper Limit Register (PCI offset EEh)	Discard cached data after this number of clock cycles have passed without a read hit on the completion data buffer.

2 Increased Upstream Memory Read Performance

The XIO2001 incorporates a new logic module which greatly improves the performance of upstream memory read transactions. This auto pre-fetch agent will generate speculative read requests on behalf of a PCI master or masters.

3 Added JTAG Interface to Support Boundary Scan

Boundary scan is a method for testing interconnects on printed circuit boards. The JTAG interface complies with IEEE standard 1149.1 and utilizes the standard 5 pin interface (TCLK, TDI, TDO, TMS).

4 Added $\overline{\text{CLKREQ}}$ Support

The $\overline{\text{CLKREQ}}$ signal is an open drain, active low signal that is driven low by the XIO2001 to request that the PCI Express reference clock be available in order to allow the PCI Express interface to send/receive data. $\overline{\text{CLKREQ}}$ is generally used when power consumption is a major concern.

5 New Support for Slower PCI Clock

The XIO2001 has additional native support for four PCI clock frequencies. When PCLK66SEL, and M66EN signals are pulled high the PCI clock frequency will operate at 66MHz, when M66EN is pulled low the PCI clock frequency will operate at 33MHz. When PCLK66SEL is pulled-low and M66EN is pulled-high the PCI clock frequency will operate at 50MHz, when M66EN is pulled low the PCI clock frequency will operate at 25MHz. Like the XIO2000A the XIO2001 still supports any PCI clock frequency up to 66MHz when the clock is provided externally.

6 Improved ASPM Support

There is a difference in the way the XIO2001 implements ASPM compared to the XIO2000A. On the XIO2000A the L1 state can only be entered if the receiver has detected entry into L0s. On the XIO2001 this dependency no longer exists, the XIO2001 will immediately send PM_Active_State_Request_L1 DLLP's after determining that there are pending TLP's or DLLP's.

7 Pin Out Changes

The XIO2001 is not pin compatible to the XIO2000A. There are some new signals in the XIO2001 while other signals have been removed.

Document Revision History

DATE	REVISION	COMMENTS
07/2009	–	Initial release

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