Reading the Configuration Registers of the 10-Bit THS10064, THS1007, THS10082, and THS1009

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ABSTRACT

The THS10064, THS1007, THS10082, and THS1009 are 10-bit variations of the THS1206. A useful feature of the THS1206 is the ability to read back the configuration register values for verification of the user configuration settings. While not specifically mentioned in the data sheets, these 10-bit parts provide similar debug functions.

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1 Introduction

THS1206, THS1207, THS12082, and THS1209 have a register read-back function that is very helpful during code debugging. This feature allows the user to verify that the configuration registers (CR0 and CR1) have been properly set to the desired operational configuration. With the introduction of the 10-bit THS1007, THS10064, THS10082, and THS1009, this feature has been removed from the data sheet—but not from the device.

2 Configuring the Registers

Note the THS1206 configuration register description includes the *RBACK* function, which is invoked by setting bit 9 of configuration register 1 (CR1 Bit 9 = 1). This special debug mode allows the user to read the values stored in CR0 and CR1 in two subsequent reads.

REG	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CR0	TEST1	TEST0	SCAN	DIFF1	DIFF0	CHSEL1	CHSEL0	PD	MODE	VREF
CR1	RBACK	OFFSET	BIN/2's	R/W	DATA_P	DATA_T	TRIG1	TRIG0	OVFL/FRST	RESET

Figure 1. THS1206 Configuration Registers

The THS1007, along with the other 10-bit devices listed above, declares this bit as *reserved*. By setting bit 9 of CR1 in the 10-bit devices, it is also possible to read the values stored in the configuration register. To properly interpret the results, the controlling software must reformat the values read back from the ADC.

REG	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CR0	TEST1	TEST0	SCAN	DIFF1	DIFF0	CHSEL1	CHSEL0	PD	MODE	VREF
CR1	RESERVED	OFFSET	BIN/2's	R/W	RES	RES	RES	RES	SRST	RESET

Figure 2. THS1007 Configuration Registers

3 Configuration Example

Using the 4-channel THS1007 as an example, the device is configured to scan 4 single-ended channels, using the internal reference with normal binary output and $\overline{RD}$ disabled. This is accomplished by writing the hex values 0x098 and 0x4C0 to CR0 and CR1 respectively.

To verify that the device is actually configured properly, simply revise the command word to the CR1 register from 0x4C0 to 0x6C0. This effectively sets the *reserved* BIT 9 of CR1, which is functionally equivalent to *RBACK* on the 12-bit devices, and the data converter responds by reporting the values 0x026 and 0x1B4.

At first glance, the data read appears to be totally unrelated to the command word. Careful review of the data, coupled with an understanding of the data output path from the ADC, reveals the correlation.

4 Interpreting the Data

Table 1 shows a straight binary representation of the command words as well as data values returned during the register read-back operation of the THS1007.

Table 1. Interpreting the Data

CR0 WRITE	CR0 READ	CR1 WRITE	CR1 READ	FORMAT
0x098	0x026	0x6C0	0x1B4	HEX
0000 1001 1000	0000 0010 0110	0110 1100 0000	0001 1011 0100	BINARY

Inspecting the value read from configuration register 0 reveals that the value returned is simply shifted two bits to the right. Realizing that the 10-bit THS1007 is based on the 12-bit architecture of the THS1206, it is relatively easy to understand that the output data is right shifted in order to maintain LSB to MSB alignment. This provides a clear and easy upgrade path between the 10- and 12-bit devices, since they can share a common footprint.

Notice that the value read from CR1 is also shifted two bits to the right, but it would appear as though there is an *extra* bit (Bit 2 is set in the read value). The explanation for this comes from the default values of CR1 and requires a minimal understanding of the THS1206 CR1 register.

Bits 5 and 4 of CR1 in the THS1206 control the DATA_AV signal behavior. These bits determine if the signal is active high or active low, and they set the signal to be a pulse or static output. The SYNC pulse of the THS1007 is equivalent to DATA_AV, except that it is always configured as a static level, active low signal. This means that the 3rd LSB during register read-back of the THS1007 always reads as the value 1.

Table 2. Reformatted Data

CR0 WRITE	CR0 READ	CR1 WRITE	CR1 READ	FORMAT
0x098	0x026	0x6C0	0x1B4	HEX
0000 1001 1000	0000 0010 0110	0110 1100 0000	0001 1011 0100	BINARY
	0000 1001 1000		0110 1101 0000	Shift CR0, CR1 left 2
			0100 110x 0000	Mask CR1 Bit 4
0000 1001 1000	0000 1001 1000	0110 1100 0000	0100 1100 0000	Compare Results

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