Interfacing the TLV320AIC1110 Codec With the TMS320C5402 DSP

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ABSTRACT

The TLV320AIC1110 is one of the high-performance codecs from Texas Instruments (TI) designed for easy use in various voice-band communication applications. It is an enhanced codec with more control capabilities. This application report provides the user with a simple coding example that facilitates the interface of this codec with the TMS320C5402™ DSP. The example code provides a good basis for more complex system developments. It also highlights some design issues to be noted. Project collateral discussed in this application report can be downloaded from the following URL: http://www.ti.com/lit/zip/SLAA158.

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1 Introduction

Texas Instruments (TI) offers a wide range of high performance codecs that can be used in various voice-band communication applications. The TLV320AIC1110 (AIC110) device is a low power pulse code modulation (PCM) codec, designed to perform analog-to-digital (A/D) conversion (coding) and digital-to-analog (D/A) conversion (decoding). It is programmable for either a 15-bit linear data conversion or an 8-bit companded μ-law or A-law data conversion format. It supports a PCM clock rate of 128 kHz or 2.048 MHz. The codec has an on-chip I^2C bus, which allows a simple 2-wire serial interface with a host processor. In addition, a dual-tone multifrequency (DTMF) generator with programmable resolutions and a single-tone generator capable of up to 8 kHz, are included in the device. This codec is pin compatible with the TLV320AIC1103 and the TLV320AIC1109 codecs.

The AIC1110 has a special function that makes it quite easy to work with. The power-up default mode feature gives the codec designer the option of having the device powerup on external reset, or power down on external reset. Upon power up, all registers are set with default values with which the codec can function effectively. In other words, in this mode, no further device programming is required. The choice of power-up default, and power-down default is selectable by placing the appropriate logic level on the PWRUPSEL terminal. Applying an active low external reset pulse, with a minimum pulse width of 500 ns to the $\overline{\text{RESET}}$ terminal, ensures that all registers are at their respective default values upon power up. See Table 1.

Table 1. Power On Device Status

PWRUPSEL LOGIC LEVEL	DEVICE STATUS
0	Power down on external reset
1	Power up on external reset

This report addresses the power up on reset option. This option requires no register programming—which would otherwise require access to the I^2C interface.

TI's inexpensive AIC1110 evaluation module (EVM), the TLV320AIC1110EVM, can be easily interfaced with a C54xx™ DSP development platform. See *Codec Evaluation System*[1]

Figure 1 shows the TLV320AIC1110EVM.

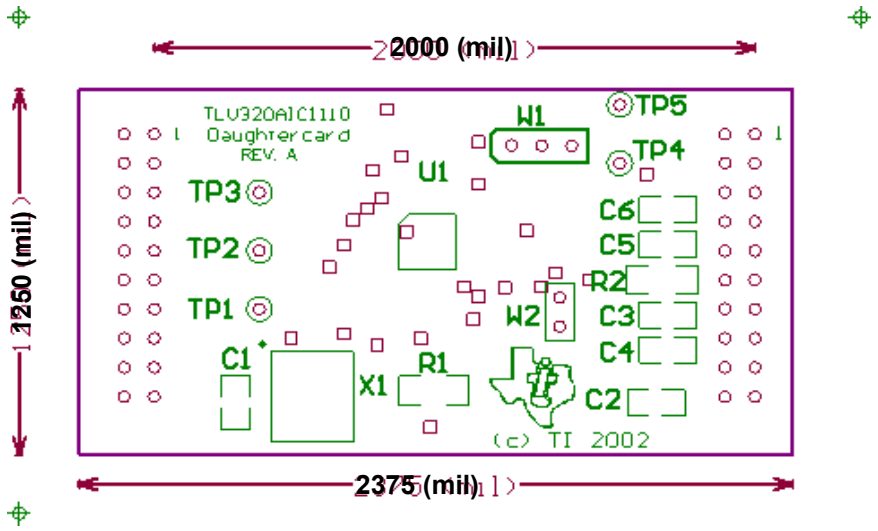

Figure 1. TLV320AIC1110 Codec EVM

The TMS320C5402 (C4302) DSP is an inexpensive fixed-point DSP with 16K word on-chip memory and has various on-chip peripherals. These peripherals include two multichannel buffered serial ports (McBSPs), an enhanced 8-bit parallel host port, two 16-bit timers, and a six-channel direct memory access (DMA) controller—see *TMS320C54x DSP Reference Set, Volume 1: CPU and Peripherals*(SPRU131)[2]. The C5402 performs up to 100 million instructions per second (MIPS), while the C5402A performs up to 160 MIPS. TI also has a series of DSP starter kits (DSK) for the various DSP families, in this case the TMS320C5402™ DSK. Using this starter kit, the DSP systems developer is able to design and test a complete AIC1110 codec system.

This application report describes the software needed to interface the AIC1110 codec with the TMS320C54xx DSP. It also provides a tested and proven software example code.

For more information on the TMS320C5402 DSP, refer to *TMS320VC5402 Fixed-Point Digital Signal Processor* (SPRS079)[3], and for more information on the AIC1110 codec, refer to *TLV320AIC1110 PCM Codec* data sheet (SLAS359) [4].

1.1 Design Concept

The AIC1110 codec is a voice-band communication device that interfaces easily with the TMS320C5402™ DSK through the DSK's McBSP port. See the sections on TLV320AIC1110 Control, and McBSP Initialization for detailed information on configuring both the AIC1110s and the McBSP.

The codec operates as a stand-alone slave, receiving all its timing and synchronization signals from the DSP—the *master*. The DSP is programmed to generate a 2.048 MHz clock signal, and an 8 kHz frame synchronization signal. These signals are made available at the CLKX and FSX terminals of McBSP1. Both signals drive the MCLK and the PCMSYNC inputs of the codec respectively. The analog-to-digital conversion output of the codec is available at the PCMO terminal of the codec, and the digital input to the digital-to-analog converter is fed into the codec through the PCMI terminal.

This device is a 15-bit codec with a configurable data I/O format. The data format can either be a 15-bit left-justified linear-data format, or an 8-bit left-justified companded μ-law or A-law data format.

The codec is configured for power up on reset by tying the PWRUPSEL high. In this mode, the codec *wakes up* from reset, into a viable operating state, by virtue of the internally generated register values. These values are automatically programmed into the internal registers of the codec device upon application of the appropriate reset signals to the RESET pin. This way, there is no need for programming any register. The default settings of this codec are discussed at length. Of course, the default settings for this device can be easily overwritten by programming the desired registers through the I^2C interface.

The basic concept of this example is as follows:

- Configure the AIC1110 for a stand-alone, power up on RESET.
- Sample a given analog input signal at 8 kHz through the receive terminal of the DSP.
- Read each 15-bit data sample through the McBSP0's DRR register of the DSK, and send it back (unchanged) through the DXR of the same McBSP channel. This simulates a digital loop back.

2 Software Interface

For the interaction between the DSP and the codec, a set of software routines is available. These include the DSP initialization routine for both the McBSP and the complex programmable logic device (CPLD) registers, and the interrupt service routines for the DSP/codec handshake. This software package is available for download at www.ti.com. The user can adapt this software package for whatever application he chooses to implement. In addition, shell programs or templates for customizing application software programs are also available at [5].

2.1 DSP Initialization

The DSP initialization routine sets up the DSP by programming its memory-mapped registers (MMRs) to the top of the data-memory page. For a more comprehensive discussion of the MMRs, see [2]. The MMR initialization program is located in the zipped file associated with this application report and available for download at www.ti.com.

2.2 DSP System Clock Frequency

An onboard 20-MHz crystal oscillator provides the basic system clock for the C5402™ DSK. The on-chip phase locked loop (PLL) circuitry provides a series of derivative clock frequencies that can be selected either by hardware or software:

- Hardware: Set the toggle posts of DIP switches DIP SW #5, DIP SW #4, and DIP SW #3 to the corresponding terminals CLKMD1, CLKMD2, and CLKMD3 respectively. See the CLKMD DIP switch control chart, Table 2. Whatever setting is programmed through this DIP switch is the reset default frequency of the DSP.

  OR

- Software: Set the corresponding bits of MMR CLKM to change the DSP clock frequency from the reset default value, to a new operating value. Refer to *Interfacing the TLV320AIC10/11 to the TMS320C5402 DSP*, SLAA109[6], for more information.

Table 2. DIP Switch Settings for CLKMD Configuration

DIP SW #5 (CLKMD1)	DIP SW #4 (CLKMD2)	DIP SW #3 (CLKMD3)	CLKMD RESET DEFAULT	DSP CPU CLOCK FREQUENCY (DSK ONBOARD 20-MHz CRYSTAL)
0	0	0	0xE007	x15 (not valid)
0	0	1	0x9007	1 x10 (not valid)
0	1	0	0x4007	x5 (100 MHz)
1	0	0	0x1007	x2 (40 MHz)
1	1	0	0xF007	x1 (20 MHz)
1	1	1	0x0000	x0.5 (10 MHz)
1	0	1	0xF000	x0.25 (5 MHz)
0	1	1	—	Reserved

2.3 Software Loop Control

The main program for this software release has an infinite loop from within which a LoopControl routine is called continuously. It allows the loop to be repeated at a fixed frequency of 16 kHz. Its operation and cycling frequency computation are described in the subsequent paragraphs. If the user wishes to include some routines that should be repeated periodically, they could be placed within this infinite loop. These routines should be short enough to ensure completion within the 0.0625 msec period—otherwise the 16 kHz period requirement must be relaxed.

Timer0 is used to set and control an idle loop which determines the rate at which the instructions in the main loop (of the main program) are repeated. For this example, a cycling rate of 16 kHz is used. Assuming that the DSP is configured for a 100 MHz clock rate, the required loop rate can be obtained by any one of three ways:

- Setting the Timer0 divide-down counter, MMR:TDDR to 0 and MMP:PDR to 6249, on the basis of the LoopFrequency = 100 MHz/(MMR:TDDR+1)/(MMR:PDR+1) formula
- Setting the Timer0 divide-down counter, MMR:TDDR to 4 and MMP:PDR to 1249, on the basis of the LoopFrequency = 100 MHz/(MMR:TDDR+1)/(MMR:PDR+1) formula
- Setting any combination of MMR:TDDR and MMR:PDR that makes the product of (MMR:TDDR+1) and MMR:PDR+1) equal to 6250

Upon executing the InitC5402 () routine, Timer0 is stopped, and the MMR registers of the timer are programmed for the 16 kHz requirement. The timer's countdown is subsequently started, and the infinite loop of the main program is entered. After executing the body of the main program, the LoopControl () routine continuously monitors the status of TImer0's interrupt flag. Note that the timer's interrupt does not have to be enabled, since its status is being polled. Upon timeout, the interrupt flag is cleared, and control is passed back to the main loop, where the body of the main loop is repeated. This cycle continues indefinitely. Refer to the flow chart in Figure 2.

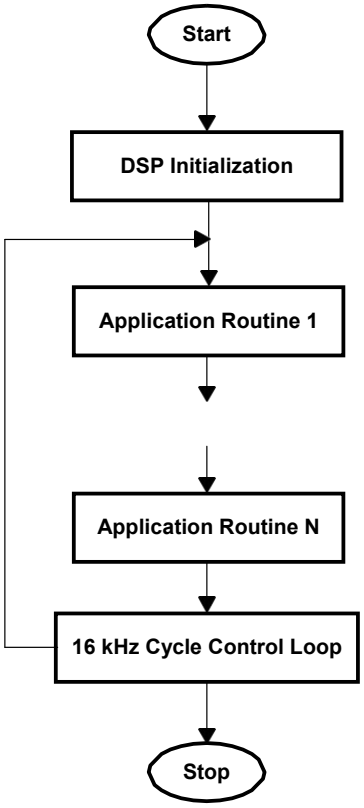

Figure 2. Main Loop Control Flow Chart

2.4 McBSP Initialization

The McBSP is a high-speed, full-duplex serial port communication channel. McBSP0 and McBSP1 are two independent McBSP channels available on this DSP. The McBSP's triple buffered input port (Receiver) and double buffered output port (Transmit) on each channel enable a continuous stream of input and output data to be transferred across either channel. In addition, an independent setting for each channel's frame synchronization and clocking signals for data transmit and data receive can be programmed. When properly configured, a McBSP channel interfaces gluelessly with another McBSP channel, any individual member of the AIC family, or any other device that adheres to the smart time division multiplexed serial port (SMARTDM) communication protocol. The ability to configure these clock signal terminals, frame synchronization and clocking terminals, as inputs or outputs, gives the McBSP the flexibility to operate as a master device or a slave device.

For this application report, the DSP is the master, with McBSP1 being used for communicating between the DSP and the slave TLV320AIC1110 codec device.

See Table 3 for the pin definition and pin description for each McBSP channel.

Table 3. McBSP Hardware Pin Description

PIN ID	I/O DIRECTION	DESCRIPTION
DR	Input	Received serial data
DX	Input/output/high impedance	Transmitted serial data
FSR	Input/output/high impedance	Receive frame synchronization
FSX	Input/output/high impedance	Transmit frame synchronization
CLKR	Input/output/high impedance	Receive clock
CLKX	Input/output/high impedance	Transmit clock
CLCKS	Input	External McBSP system clock

Each McBSP channel has seven pins with which the DSP communicates with external circuits. The direction and characteristics of each terminal are programmed through the McBSP's MMR registers described in Table 4. Refer to *TMS320C54x DSP Enhanced Peripherals, Reference Set Volume 5*, (SPRU302)[7], for more information on accessing the McBSP control registers.

Table 4. McBSP Registers Memory Map

ADDRESS DATA MEMORY		SUBADDRESS	ACRONYM	DESCRIPTION
MCBSP0	MCBSP1			
0x0020	0x0040		DDR2	Data receive register 2
0x0021	0x0041		DDR1	Data receive register 1
0x0022	0x0042		DXR2	Data transmit register 2
0x0023	0x0043		DXR1	Data transmit register 1
0x0038	0x0048		SOSA	Serial port sub-bank address register
0x0039	0x0049		SPSD	Serial port sub-bank data register
		0x0000	SPSCR1	Serial port control register 1
		0x0001	SPSCR2	Serial port control register 2
		0x0002	OCR1	Receive control register 1
		0x0003	RCR2	Receive control register 2
		0x0004	XCR1	Transmit control register 1
		0x0005	XCR2	Transmit control register 2
		0x0006	SRGR1	Sample rate generator register 1
		0x0007	SRGR2	Sample rate generator register 2
		0x0008	MCR1	Multichannel register 1
		0x0009	MCR2	Multichannel register 2
		0x000A	RCERA	Receive-channel enable register partition A
		0x000B	RCERB	Receive-channel enable register partition B
		0x000C	XCERA	Transmit-channel enable register partition A
		0x000D	XCERB	Transmit-channel enable register partition B
		0x000E	PCR	McBSP pin-control register

For this application report, the McBSP1 is programmed such that

- The word size is 16-bit.
- Data is left-justified.
- Frame length is 1 word per frame.
- Transmit interrupts are issued on new-frame synchs.
- The frame synch rate, i.e., sampling frequency, is 8 kHz.
- CLKX or MCLK is set for 2.048 MHz.

2.5 Interrupts

There are two types of interrupt systems on this DSP, the hardware driven interrupts which are truly synchronous, and the software driven interrupts which are asynchronous. The TMS320C5402 DSP has 30 different interrupt vectors:

- Two nonmaskable interrupts, the hardware RESET, and the nonmaskable interrupt (NMI). These interrupt sources can not be disabled by software. The global interrupt enable (GIE) status has no bearing on the individual nonmaskable interrupt's ability to interrupt any execution process.
- Fourteen software interrupts that can be issued at any point during the program execution. If called within a subroutine, as long as the DSP's interrupt system is globally enabled, the processor vectors to the associated interrupt service routine (ISR).
- Fourteen hardware peripheral interrupts that could be enabled or disabled corporately by enabling or disabling the DSP's interrupt system globally or individually, by the designer's setting or choosing the associated bit. At the end of the current instruction, the CPU suspends the current routine being processed, and vectors to the associated interrupt service routine (ISR)—if all the following conditions are satisfied:
  - The DSP's interrupt system is globally enabled.
  - That particular interrupt has been individually enabled.
  - There is no other interrupt with a higher priority being serviced.

Upon receiving a valid interrupt request that satisfies the requirements stated above, the DSP accesses an interrupt vector table, from which it picks up the address of the corresponding ISR routine. The application report *Interfacing the TLV320AIC10/11 to the TMS320C5402 DSP*, SLAA109[6], provides a more concise description of the TMS320C5402 interrupt protocol and ISR vectoring.

For this application report, the McBSP1 is configured to generate a transmit interrupt (XINT) each time a frame synchronization pulse is issued. When this occurs (and no interrupts of higher priority are pending, and the McBSP1's XINT interrupt is enabled) the DSP completes the current instruction, suspends its current tasks, and vectors to the appropriate ISR routine—McBSP1TXISR(). The ISR is configured so that upon issuing a frame-sync pulse, a string of 16-bit digital data (resulting from a previous conversion) is available for transmission to the DSP—and the codec is ready to receive a 16-bit string of digital data from the DSP. Within this routine, the DSP reads the result of the codec's left-justified analog-to-digital conversion through the McBSP1's DRR1 register. It sends the new data out to the codec's digital-to-analog converter through the McBSP1's DXR1 register. This process simulates a digital loopback system.

The ISR used for this application example is available for download in a zipped file.

2.6 CPLD Register Initialization

The C5402 DSK has a complex programmable logic device (CPLD) through which it implements the various logic required for interfacing the DSP to the outside world, and at the same time, providing control and status interfaces for the DSP through software. Refer to *Interfacing the TLV320AIC10/11 to the TMS320C5402 DSP*, SLAA109[6], for more details.

The C5402 DSK is equipped with an onboard codec unit. The onboard codec is configured such that it is interfaced with the DSP through the McBSP port 0, and the onboard data access arrangement (DAA) chip is also interfaced through the McBSP port 1. However, there are only two McBSP ports on this DSP. In order to accommodate a plug-in codec board, there must be a way of rerouting the McBSP ports so they can be alternatively connected to an external unit, through software. This is one of the functions of the CPLD. By programming various bit patterns into the control register CNTL2 of the CPLD, the user can choose between routing the McBSP signals to the various onboard peripherals, or to the plugged-in peripherals. See Figure 3. Refer to Table 5 for the definition of the bits of the CLPD control register CNTL2. The zipped AIC initialization assembly routine includes the set of commands required to accomplish this signal rerouting.

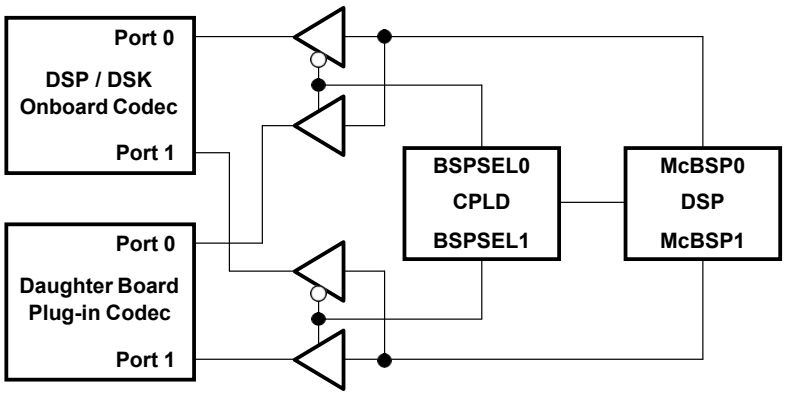

Figure 3. Main Loop Control Flow Chart

Table 5. CLDP Control Register, CNTL2

BIT POSITION	ACRONYM	R/W	DESCRIPTION
7	DAAOH	RW	DAA off-hook control
6	DAACID	RW	DAA caller ID enable
5	FLASHENB	RW	External memory source selection (0 = flash; 1 = SRAM)
4	INT1SEL	RW	INT1 interrupt source selection (0 = UART; 1 = daughter board)
3	FC1CON	RW	Microphone/speaker AD50 FC control
2	FC0CON	RW	DAA AD50 FC control
1	BSPSEL1	RW	McBSP1 data source selection (0 = Microphone/speaker; 1 = daughter board)
0	BSPSEL0	RW	McBSP0 data source selection (0 = DAA; 1 = daughter board)

2.7 TLV320AIC1110 Control

The TLV320AIC1110 configured for power up on reset requires no programming. Applying a high logic on the PWQRUPSEL pin prior to issuing a codec reset command, places the device in the power up on reset mode. Codec operations can commence on the strength of the default register setting without having to reprogram any registers. The following paragraphs describe the operating condition of the codec in the power up on reset mode. Any of these registers can be subsequently read or modified by communicating with the respective register through the I^2C port. Refer to the *TLV320AIC1110 PCM Codec* data sheet, (SLAS359)[4] for more information on the codec operation.

Table 6. AIC1110 Register Power-Up Default Values

REGISTER ID	REGISTER FUNCTION	DEFAULT VALUE	OPERATING CONDITION
00	Power control	0xF6	PWRUPSEL = 0 (not applicable)
00	Power control	0x9B	PWRUPSEL = 1 (selected option)
01	Mode control	0x02	N/A
02	TXPGA	0x40	N/A
03	RXPGA	0xA0	N/A
04	High DTMF	0x00	N/A
05	Low DTMF	0x00	N/A
06	Auxiliary	0x00	N/A

Based on the default value of the individual register, the following tables show the features activated.

Table 7. AIC Register 00 Default Features

CODEC FEATURE	SELECTION
Reference system	REF powered up
EAR amp. selected	AMP1, AMP2 powered down
Receive channel status	Enabled
Microphone bias	Enabled
Microphone selection	MIC1
Transmit channel status	Enabled
Sidetone status	Muted

Table 8. AIC Register 01 Default Features

CODEC FEATURE	SELECTION
Transmit channel filtering	High-pass filter disabled and slope filter enabled
Receive channel filtering	High-pass filter disabled, only low filtering available
Buzzcon status	Buzzer control logic disabled
Data format mode	Liner, 15-bit data mode, no μ-law nor A-law companding
Transmit/receive mode	Normal, no PCM loopback
Tone mode status	Tone mode disabled

Table 9. AIC Register 02 Default Features

CODEC FEATURE	SELECTION
Transmit PGA gain setting	MIC AMP1 Gain = 23.5 dB, MIC AMP2 Gain = 6, TX PGA = 0 dB, Gain Mode = Normal, Total TX Gain (typical) = 29.5 dB
Sidetone gain setting	(Typical) –12 dB

Table 10. AIC Register 03 Default Features

CODEC FEATURE	SELECTION
Receive PGA gain setting	RX PGA = –4 (typical/voice mode), PX PGA = –6 dB (tone mode)
Receiver volume setting	(Typical) 0 dB

Table 11. AIC Register 04 Default Features

CODEC FEATURE	SELECTION
DTMF (high tone) and single tone setting	N/A

Table 12. AIC Register 05 Default Features

CODEC FEATURE	SELECTION
DTMF (low tone) setting	N/A

Table 13. AIC Register 06 Default Features

CODEC FEATURE (AUXILIARY)	SELECTION
MCLK setting	2.048 MHz
Analog switch output setting	OUT2
Low tone frequency resolution	N/A (7.8125 Hz)
High tone frequency resolution	N/A (7.8125 Hz)
Receiver channel gain	0 dB (voice mode only)
MCLK detector setting	Powered ON

Table 14. Functions and Default Settings of Jumpers W1 and W2 for the TLV320AIC1110 EVM

JUMPER	DESCRIPTION	POSITION		
		1–2	2–3	DEFAULT
W1	Power-up reset select	Power up	Power down	Power up
W2	Pseudo-differential input configuration	Pseudo differential	N/A	Single ended

2.8 Codec ADC/DAC Sampling Frequency

A 2.048 MHz master clock (MCLK) signal is delivered from the CLKX terminal of McBSP1 to the codec's MCLK terminal. In addition, the frame synchronization signal, which is also the sampling frequency signal, can take values up to 8 kHz. It is transmitted from the FSX terminal of McBSP1 to the PCMSYNC terminal of the codec. From both input signals, all the derivative clocks required by the codec are generated internally.

2.9 Design Issues

The operation of the AIC1110 codec in the power up on reset mode is quite easy and straightforward. All that is required is to provide the appropriate set of SMARTDM communication protocol signals for receiving data from the codec's analog-to-digital converter circuits and for transmitting data its digital-to-analog converter circuits. After codec reset, the user can modify any of the codec's programmable registers through the I^2C communication interface. This mode of operation will be covered in a future application report.

The user must keep in mind that the linear data format is 15 bits, left justified, for both transmit and receive. In either companding mode, μ-law or A-law, the data format is 8 bits, left justified.

3 References

1. *Codec Evaluation System* (SLAA141)
2. *TMS320C54x DSP Reference Set, Volume 1: CPU and Peripherals* (SPRU131)
3. *TMS320VC5402 Fixed-Point Digital Signal Processor*, data sheet (SPRS079)
4. *TLV320AIC1110 PCM Codec* data sheet (SLAS359)
5. *TMS320C54x DSP Reference Set, Volume 4: Applications Guide* (SPRU173)
6. *Interfacing the TLV320AIC10/11 to the TMS320C5402 DSP*, (SLAA109)
7. *TMS320C54x DSP Enhanced Peripherals, Reference Set, Volume 5* (SPRU302)
8. *TLV320AIC12/13/14/15 Codec Operating Under Stand-Alone Slave Mode* application report (SLAA142)

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