APPLICATION NOTE

POWER FACTOR CORRECTION USING THE UC3852 CONTROLLED ON-TIME ZERO CURRENT SWITCHING TECHNIQUE

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INTRODUCTION

The controlled on-time, zero current switching technique provides a simple and efficient solution to obtaining high power factor correction. This discontinuous inductor current approach essentially programs a constant switch on-time during one line half-cycle. It does not require any "complex" analog square, multiply and divide functions to control the instantaneous switch current as with other PFC techniques. Additionally, zero current switching limits the peak current to exactly twice that of the average inductor current over all line and load combinations. High efficiency operation is also achieved with no boost rectifier recovery concerns and power loss. In a typical 80 Watt application the UC3852 PFC technique delivers a power factor of 0.998 with 5.8% Total Harmonic Distortion at nearly 94% efficiency.

CIRCUIT SCHEMATIC

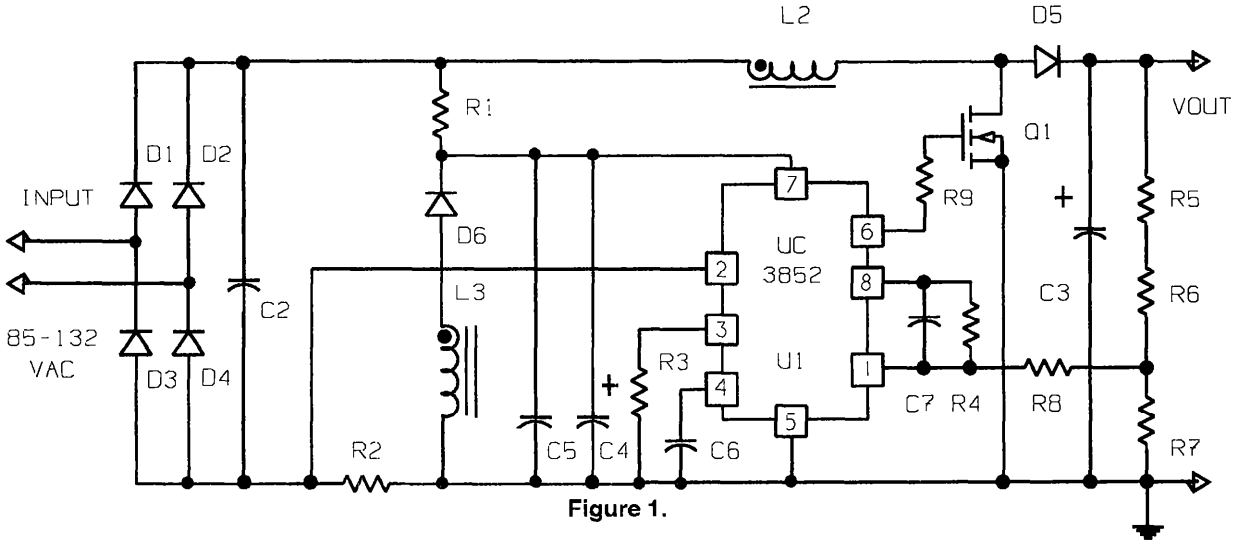


Figure 1.

UC3852 FEATURES

The UC3852 PFC controller contains several features which minimize external parts count while providing excellent performance and protection. Optimized for this off-line PFC application, the UC3852 delivers high power factor (0.997 typical) and a low cost overall solution.

OFF-LINE PROTECTION

- undervoltage lockout with hysteresis 16V turn-on, 11 V turn-off [1]
- clamped 12V gate drive output [2]
- active low, self biasing output [3]
- overcurrent protection [4]

CONTROL CIRCUIT ATTRIBUTES

- programmable maximum frequency [3, 5]
- programmable maximum on-time [3, 5]
- overcurrent indication output [7]

OPERATIONAL CHARACTERISTICS

- low operating current [8]
- low start-up current (0.4 mA) [1]
- few external required components
- 30 V maximum supply input [7]

CONTROL TECHNIQUE

- Zero Current Switching [9]
- controlled on-time [6]
- high noise immunity [6]

UC3852 POWER FACTOR CORRECTION CONTROL IC BLOCK DIAGRAM

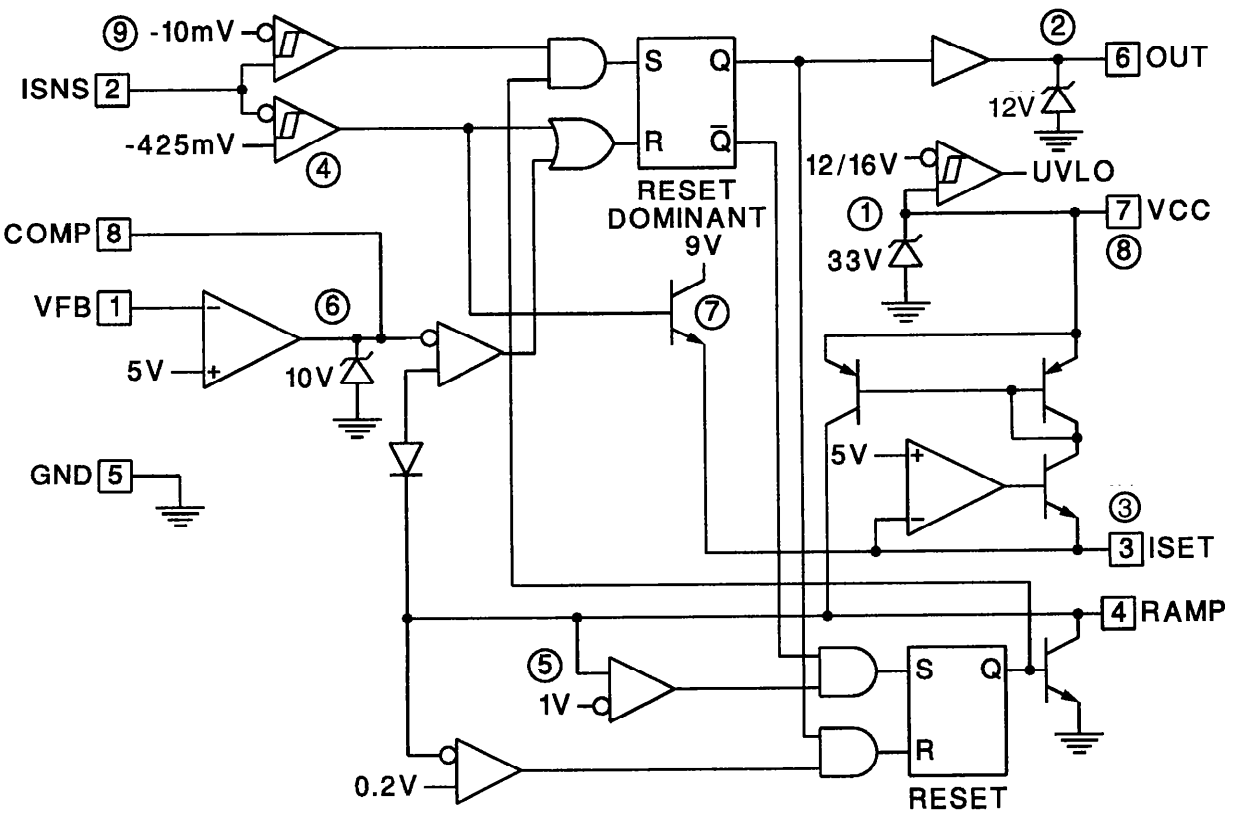


Figure 2.

UC3852 POWER FACTOR CORRECTION CONTROL IC BLOCK DIAGRAM

PFC TECHNIQUE OVERVIEW

Most power factor correction techniques incorporate the boost topology which can be operated in either the continuous or discontinuous inductor current modes and switched at a fixed or variable frequency. Generally, the fixed frequency, continuous inductor current variety is preferred for higher power applications to minimize the peak current. Below about 500 Watts, the discontinuous inductor current version operated in a variable frequency mode offers several advantages. Benefits include reduced inductor size, minimal parts count and low cost of implementation. This paper will highlight the controlled on-time, zero current switched variety of discontinuous inductor current PFC operation.

FUNDAMENTALS

CONTROLLED ON-TIME

On-time of the PFC switch is controlled by the voltage error amplifier of the UC3852 which is compared to a sawtooth waveform generated at the ICs RAMP function at pin 4. The PFC switch on-time varies with line and load conditions but should be considered constant for one line half-cycle. A low frequency bandwidth is necessary in the voltage error amplifier loop compensation which is typically rolled off to cross zero dB below the line frequency.

ZERO CURRENT SWITCHING

Zero current switching facilitates three important advantages in this application. First, the inductor current must be zero before the next switching cycle is initiated inferring high efficiency and elimination of the boost rectifier recovery loss. Secondly, the change in inductor current (delta IL) is equal to the peak inductor current (IL(pk)) since current starts and returns to zero each cycle. The discontinuous boost converter current waveform has a triangular shape with an area (charge) equal to one-half of the product of its height (peak current) multiplied by its base (time). Since the timebase can be considered as a series of consecutive triangles, the peak current is therefore limited to exactly twice that of the average current. This is valid for both the steady state and instantaneous switching cycle relationships. The converter operates right on the border between continuous and discontinuous current modes which results in variable frequency operation.

The "fixed" on-time in conjunction with zero current switching provide automatic power factor correction of the input current. This can be demonstrated by analyzing the basic inductor waveform using specific attributes of this PFC technique for either charging and discharging of the inductor current. Since the inductor charging condition is being controlled by the UC3852 circuitry it will be used for the analysis.

INDUCTOR WAVEFORM

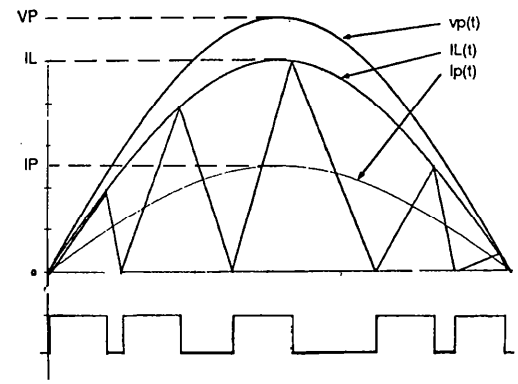


Figure 3.

1. $\frac{V}{L} = \frac{dI}{dt}$

For the PFC boost converter operation, V can be replaced by Vin(t), the instantaneous voltage across the inductor. Also, it is assumed that the inductance and the switch on-time is constant for the duration of one line-half cycle. The change in inductor current, delta I is actually the peak value of current (Ipk(t)) since the inductor always begins charging at zero current, as forced by zero current switching. Substituting these relationships into the inductor wave from equation will demonstrate the simplicity of this specific technique when used for power factor correction.

V = Vin(t)

L = constant

dI = Ipk(t)

dt = constant

2. Ipk(t) ∝ Vin(t)

This relationship demonstrates that the instantaneous line current will exactly track that of the instantaneous line voltage. Since the input voltage waveform is sinusoidal (Vin sin(wt)), then so is the input current (Ipk sin (wt)). This controlled on-time, zero current switched technique provides automatic power factor correction with very simple control circuitry.

PFC POWER STAGE DESIGN

It is advantageous to begin the power relationships from the AC line input of the preregulator and work towards the DC output section. The instantaneous primary voltage (VP(t)) is related to the steady state peak input (VP) by the following relationship:

3. $VP(t) = VP \sin(wt)$

where $VP = \sqrt{2} \times Vp$ (rms)

The amplitude of Vp(t) varies between zero and VP as sin(wt) goes from zero to one for one line half-cycle. Note that Vp(t) and VP are always positive with respect to the PFC circuit common due to the bridge rectification of the AC input waveform. The input current can similarly be expressed as:

4. IP (t) = IP sin (wt)

where $IP = \sqrt{2} \times Ip$ (rms)}

Input power to the PFC converter is the Root Means Squared (RMS) component of the line voltage (Vp(RMS)) multiplied by the line current (Ip(RMS)). This can also be expressed using the peak terms of each waveform which is simpler for this application.

$$5.\ Pin = \frac{VP}{\sqrt{2}} \times \frac{IP}{\sqrt{2}}$$

$$Pin = \frac{(VP \times IP)}{2}$$

The average DC output current (Io) is determined by dividing the output power (P_O) by the output voltage (V_O).

$$6.\ Io = \frac{P_O}{V_O}$$

Converter efficiency (n) can also be factored into the design equations although it may typically be in the neighborhood of 94% at full load.

$$7.\ Pin = \frac{Po}{n}$$

or P_O = Pin x n

where $Pin = \frac{(VP \times IP)}{2}$

$$7A.\ Po = \frac{(VP \times IP \times n)}{2}$$

Equation 7A. can expressed with regard to primary current.

$$7B.\ IP = \frac{(2 \times Po)}{(VP \times n)}$$

It has been already established that the peak inductor current is exactly twice that of the average inductor current due to zero current switching.

8. IL(pk)=2xIL(avg)

The average input current must be equal to the average inductor current since they are in series.

$$9.\ Ipri\ (avg) = IL\ (avg)$$

Combining equations yields the peak inductor current to the input current.

$$10.\ Ipri\ (pk) = \frac{(4 \times Po)}{(VP \times n)}$$

The inductor current can now be analyzed in its time variant form and over all line and load conditions.

$$11.\ IL\ (t) = \frac{(4 \times Po \times \sin\ (wt))}{(VP \times n)}$$

TIMING RELATIONSHIPS

Steady state conditions will be used to analyze the timing relationships of this controlled on-time PFC technique. The peak primary voltage (VP) will be used as the starting point for the calculations, so the input line must be specified.

The inductor relationship of equation 1. will be solved for the specific on-time required to charge the inductor to the correct peak current. This equation can be restated for a given set of operating conditions as:

$$12.\ t\ (on) = IL\ (pk) \times \frac{L}{VP}$$

Substituting equation 10. for IL(pk) into equation **12** results in:

$$12A.\ t\ (on) = \frac{(4 \times Po \times L)}{(VP^2 \times n)}$$

The instantaneous switch off-time varies not only with the line and load conditions, but also with the instantaneous line voltage. Off-time is analyzed by solving equation 1. for the inductor discharging where the voltage across the inductor is Vout minus Vin. This should be solved for the time required to discharge the current from its instantaneous peak to zero, which can be expressed as:

$$13.\ t\ (off) = \frac{(IL\ (pk) \times L)}{(Vo - VP\ (\sin\ (wt)))}$$

Substituting equation 11. for IL(pk) above will expand the off-time equation to:

$$13A.\ t\ (off) = \frac{(4 \times Po \times L \times \sin\ (wt))}{VP \times (Vo - (VP \times \sin\ (wt)))}$$

Due to the high efficiency during the boost inductor discharge and lack of rectifier recovery losses, the efficiency term (n) is essentially one. Loss can be ignored during the off-time since the boost diode forward voltage drop is very small in comparison to

the high voltage DC output, and resistive losses at these lower powers and currents are minimal.

CONVERSION PERIOD

The total time for one switching cycle is obtained by adding the on-time with the instantaneous off-time. Switching frequency is the reciprocal of the cyclical switching period which varies with line, load and instantaneous line voltage.

14. t(per) = t(on) + t(off)

$$t(per) = 4 \times Po \times L \times \left(\frac{1}{VP^2} + \frac{\sin(wt)}{VP \times [Vo - VP\sin(wt)]} \right)$$

SWITCHING FREQUENCY

15. f(conv) = 1 / t(per)

Switching frequency varies with the steady state line and load operating conditions along with the instantaneous input line voltage. Generally, the PFC converter is designed to operate above the audible range after accommodating all circuit and component tolerances. Many applications can use thirty kiloHertz (30 kHz) as a good first approximation. Higher frequency operation should also be evaluated as this can significantly reduce the inductor size without negatively impacting efficiency or cost. In most applications, the minimum switching frequency will coincide with full load operation during the peak of the input voltage waveform at low line. In contrast, the highest frequency conversion occurs at light load and high line conditions, just as the input voltage waveform nears the zero crossing point. A plot of t(on), t(off), t(per) and switching frequency versus instantaneous line voltage is shown in figure 4 and for the specific application circuit of figure 1. Figure 5 demonstrates the typical changes incurred in conversion frequency from low to high line inputs.

SELECTING THE OUTPUT VOLTAGE

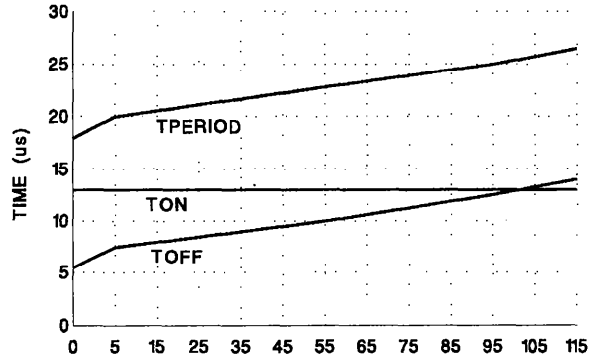
The boost converter output voltage should be designed to be at least thirty volts higher than the peak of the input voltage at high line. This will prevent long conversion cycles due to the small voltage across the discharging boost inductor. When this thirty volt margin is ignored, the minimum switching frequency will occur at the peak of high line operation and not at low line, but also at full load. This will require recalculation of the timing intervals.

INDUCTOR CONSIDERATIONS

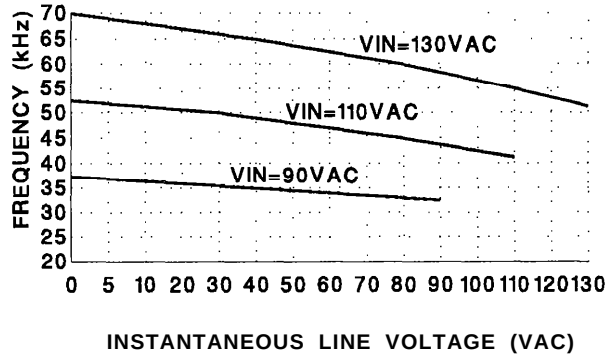
The exact inductor value can determined by solving equation 14 for the required inductance at the selected minimum operating frequency. Maximum on-time needs to be programmed into the UC3852 timing circuit. Both t(on)max and t(off)max will be individually calculated and added together to obtain the maximum conversion period, t(per)max. This is required to obtain the inductor value. Equations 12A and 13A will be solved for their respective maximums.

12B. $t\ (on)\ max = \dfrac{4 \times L \times Po\ (max)}{VP\ (min)^2}$

13B. $t\ (off)\ max = \dfrac{4 \times L \times Po\ (max)}{[VP\ (min) \times (Vo - VP\ (min)]}$



Conversion Times vs Instantaneous Line Nominal Line Voltage
Fig. 4



Conversion Frequency vs Instantaneous Line
Fig. 5.

14A. t(per)max = t(on)max + t(off)max

The minimum conversion frequency (F(conv)min) corresponds to the reciprocal of the maximum conversion period, t(per)max.

15A. F(conv)min = 1 / t(per)max

INDUCTOR VALUE

The inductance value necessary for an application can be obtained by substituting equations 12B and 13B into 15A. using the relationship of 14A.

$$16A.\ L = \frac{VP\ (min)^2 \times [Vo - VP\ (min)]}{4 \times Po\ (max) \times Vo \times F\ (conv)\ min}$$

This equation provides insight as to the possible ways to reduce the inductor value (size and cost) for a given set of design specifications. The most obvious approach is to increase the minimum conversion frequency above thirty kiloHertz if none of the other parameters (Vo, Po) can be varied.

INDUCTOR DESIGN SUMMARY

Generally, the size and cost of an inductor vary with its energy storage capacity, W(L). Although most of the energy is stored in the air gap (with a gapped ferrite design), the core set must support the necessary flux density (B) without saturating or exhibiting high core loss. The required energy storage of the boost inductor is:

17. W(L) = 0.5*L*IL(pk)^2

The number of turns required for a selected core size and material is:

18. N = L*IL(pk)*10^4 / (Bmax*Ae)

where Bmax is in Teslas and Ae is in square centimeters (cm^2)

The center leg gap to achieve the correct

inductance and storage is expressed by:

19. l(gap)={Uo*Ur*N^2*Ae*10^-2}/L (cm)

where Uo=4*Pi*10^-7(permitivity of free space), and Ur=1 (relative permeability of air)

OUTPUT CAPACITOR

The value of output capacitance is a generally determined by the required hold-up time or the acceptable output ripple voltage for a given application. It may also be governed by the specified ripple current rating or capacitor temperature rise. Typically, an approximation of one microFarad per Watt (1uF/W) is a good starting point. The exact value can later be changed depending on conversion frequency and other factors previously mentioned.

Electrolytic capacitors are typically used near 80% of their working voltage. This will necessitate a 500 VDC rating for use in a 264 VAC PFC application which may not be practical from a cost perspective. One option is to connect two lower voltage capacitors in series, each having the same value and a 250VDC rating.

SEMICONDUCTOR SELECTION

Peak currents and voltages must first be known over all operating conditions to select the proper MOSFET switch and boost rectifier. Standard design practice is to derate all semiconductors to about 75% of their maximum ratings, indicating the use of 500+ volt devices.

Low cost bipolar transistors are an acceptable alternative to MOSFETs if the conversion frequency is maintained fairly low. Inexpensive high voltage diodes with recovery times of 200 nanoseconds, or less should be used for the boost rectifier. Two popular devices are the 1N4937 and MUR160. Speed is not an issue with the input bridge rectifiers where 1N4004 to 1 N4006 types are acceptable. High frequency switching noise in the PFC converter should be well filtered before reaching the input bridge diodes due to their low speed characteristics. This is best accomplished by adding an UC filter between the bridge rectifier DC output and the boost converter.

CONTROL CIRCUIT DESIGN :

PROGRAMMING THE UC3852

STARTUP CIRCUITRY

The UC3852 design incorporates a low startup current feature and draws less than one milliamp (mA) from the Vcc bias supply. This minimizes the power loss due to with the startup resistor after the converter begins operation when a bootstrap winding supplies the full DC supply current. The UC3852 IC turns on when Vcc reaches approximately 16 volts, and IC supply current will increase to its operational level. Undervoltage lockout protection will turn the UC3852 device off when the supply voltage falls below the lower UVLO threshold of approximately 10 volts.

The startup circuitry for this off-line consists of a startup resistor from Vcc to the input supply voltage and a storage capacitor from Vcc to ground. Typically, select Rstart to supply around 1.5 milliamps (rms) of charging current (I(charge) at low line. The exact value can be obtained from the following approximations.

$$R(start) = \frac{VP(min)\ -\ V(turn\text{-}on)}{1.41 \times I(charge)}$$

The Vcc bias supply filter capacitor value is determined by several factors, but primarily by the UC3852 undervoltage lockout hysteresis. Implementation and phasing of this boost inductor winding in addition to soft start circuitry will also effect the capacitance.

$$C(V_{CC}) = \frac{(ICC - I(charge) \times t(boot)}{UVLO\ hysteresis}$$

For many applications, the following approximations can be used:

ICC = 10mA

I(charge) = 1.5 mA

t(boot) = 10 ms (one-half cycle at 50 Hz)

UVLO hysteresis = 5 volts

V(turn-on) = 15V

A standard 15 uF electrolytic with an adequate voltage rating (35V once derated) is used.

PROGRAMMING THE ON-TIME

The maximum switch on-time must be calculated to program the UC3852 oscillator. This maximum occurs when the line voltage, VP is at its minimum and the output power is at its maximum. This is more commonly known as the low line, full load condition.

t(on)max = 4*Pout(max)*L / Vp(min)^2

The UC3852 on-time is programmed by R/C components and uses two of the IC pins. A resistor from the ISET pin to ground programs the charging current into the RAMP pin. The Iset pin has an output voltage of approximately 5 volts, so the ISET is 5 volts divided by Rset. Typical charging current should range between 100 and 600 microamps.

The RAMP pin is used as one input to the Pulse Width Modulator of the UC3852. Internally, the RAMP voltage is compared to the error amplifier output (COMP) voltage to determine the exact on-time. The RAMP pin has a maximum amplitude of approximately 9 volts, and begins charging from approximately 0.2 volts, or an 8.8 volt swing.

The RAMP capacitor value is selected to program the maximum switch on-time as it charges from 0.2 to 9 volts by Iset. It can be calculated from the capacitor charge equation, shown below.

C = (I * dt) / dV

C(RAMP) = [Iset * t(on)max] / 8.8 V

The RAMP capacitor should be selected first from a list of standard values within the 100pF to 1nF range. The resulting ISET programming resistor selection is much easier as standard values with an initial tolerance of one percent (1%) are readily available.

$$RSET = \frac{5 \times t(on)max}{8.8 \times C(RAMP)}$$

or

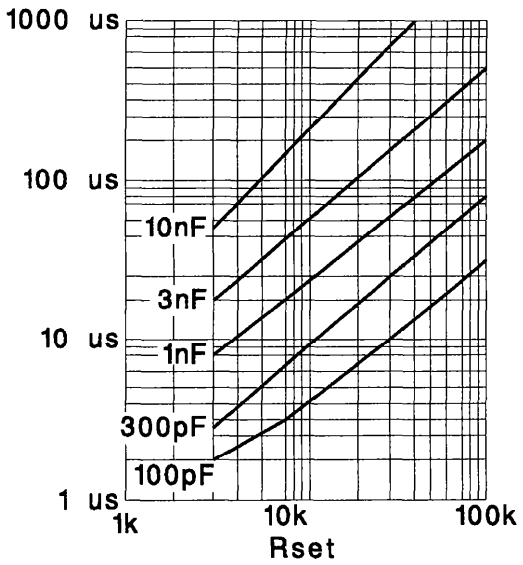
RSET = 0.568 * t(on)max / C(RAMP)

t(on)max = [RSET*C(RAMP)] / 0.568

UC3852 ON-TIME vs. RSET & C(RAMP)

ERROR AMPLIFIER COMPENSATION

Power Factor Correction using the ZCS controlled on-time technique requires a very low bandwidth voltage loop to deliver high power factor (). This is necessary to keep the switch on-time constant during any one line cycle. Other advantages to this approach are high noise immunity, and simplicity,



Max On-Time vs. Rset and Ct
Fig. 6

since no squarer, multiply or divide circuitry is needed.

Configuration of the compensation circuitry is shown in the UC3852 PFC application schematic. First, the PFC preregulator output voltage (Vout) is accurately divided down to 5.0 volts to interface with the error amplifier. Three standard one-half watt resistors are used to avoid needing more expensive, high voltage rated resistors for this application. This signal goes through a 20K ohm input resistor to the error amplifier inverting input. Feedback components are a 1 meg ohm resistor and a 0.1 uF capacitor in parallel from the E/A output to the inverting input.

This recommended amplifier compensation delivers one low frequency pole in the loop response at 1.6 Hz, as programmed by 1 meg ohm and 0.1 uF components. Low frequency gain is determined by the 20 K ohm input resistor, the output voltage divider resistance and the 5.0 reference voltage seen at the amplifiers (internal) noninverting input.

Many other compensation arrangements are possible.

Using this compensation network, a low frequency gain of approximately 34 dB is achieved. This rolls off with a single pole (-20 dB/decade) response centering at 1.6 Hz. The gain curve will intersect zero dB at about 120 Hz and result in excellent power factor correction. Better dynamic response and less overshoot of the output voltage can be obtained by adjusting the 20 K ohm input resistor to increase low frequency gain and move the zero dB crossing out to a higher frequency. Some slight degradation of the power factor is to be expected by increasing the loop response.

SOFT START

Soft starting of the output is optional, but recommended to minimize the output voltage overshoot upon power-up. This does not occur in applications which will always have some load on the output. However, most electronic ballast have either no load, or a very light load on the output at power-up and will see the overshoot. Soft start implementation requires only a diode and capacitor from the compensation pin to ground. Another diode from the capacitor to VCC discharges the soft start capacitor to the falling Vcc voltage when the AC line power is removed. This will guarantee that the circuit will always start up in soft start if the line is AC plug is removed for a few seconds. Again, this is an optional feature which depends on the application.

One “trick” to significantly reduce the size of the soft start capacitor is to replace the diode with a cheap PNP transistor. A capacitance multiplier can be obtained by connecting the PNP emitter to the error amplifier output and soft start capacitor from the base to ground. The collector of the transistor is connected to ground. This adaptation will scale the capacitance value up by beta of the transistor at the amplifier output. A 2N2907 or equivalent is a popular choice and will reduce the capacitance value by a factor of approximately 50.

A 1N914 or 1N4148 signal diode should be used from the base to emitter to prevent negative base-emitter voltages from damaging the transistor. Additionally, this transistor can easily be interfaced with any optional fault protection schemes to soft start the controller following a fault.

SOFT START IMPLEMENTATION

CURRENT SENSE

Current in the PFC design is sensed in the return line of the preregulator circuitry at the AC input bridge rectifiers. One side of the current sense resistor is referenced to the UC3852 “ground” connection. The other end of the resistor develops the current sense voltage which is equivalent to minus IL(t) * Rsense. The UC3852 zero current detection circuitry incorporates two comparators, one for zero current detection and another for over current protection.

ZERO CURRENT DETECTION

The zero current detection circuitry uses a negative 10 millivolt (-10mV) threshold as its reference. This negative threshold guarantees that there are no

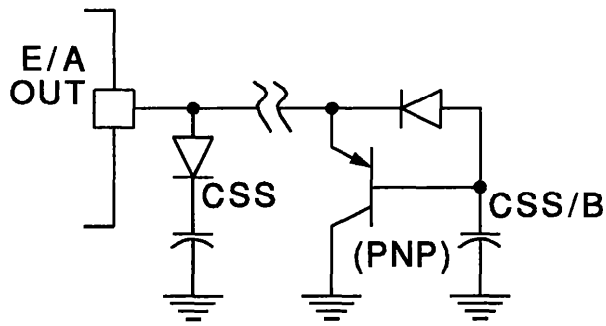


Figure 7.

startup problems since this input must be pulled below ground for normal operation. Whenever the zero detect input is raised above the minus ten millivolt threshold, the comparator is triggered and the next switching cycle begins.

Inductor current can be sensed by a current sense resistor which develops minus 400mV maximum during an overcurrent condition. This should only occur at a twenty percent overload, or 1.2 * IL(pk).

R(shunt) = 0.4 V / (1.2 * IL(pk))

Power dissipated in the shunt can be calculated by using the RMS component of the line current. The peak input current (IP) is one half of the peak inductor current (IL(max). The RMS component of the line current (IP(rms)) is obtained by dividing the peak line current (IP) by the square root of two (1.41).

IP(rms) = [IL(pk) / (2 * 1.414)

P (R(sense)) = IP(rms)^2 * R(sense)

Standard value, low resistance (1 ohm or less) one-eighth to one-quarter watt resistors can used alone or paralleled to obtain the exact value. Carbon composition or film resistors exhibit low series inductance and will work best.

A small R/C filter can be added in the current sense circuitry to filter out switching noise caused by circuit parasitics. This delay will minimally effect the precise two-to-one ratio of the peak to average

duce the amount of EMI/RFI filtering required by minimizing the rectifier recovery noise. For best results, the filter delay time should match the rectifiers recovery time. A ten ohm resistor and a one nanoFarad (1 nF) capacitor are good starting values.

OVERCURRENT FAULT PROTECTION

The UC3852 contains and overcurrent comparator (-400mV) which quickly terminates the PWM output. This comparator also drives circuitry connected to the ISET pin which raises its normal 5 volt amplitude to 9 volts during the overcurrent condition. In addition to programming the ramp capacitor charging current, the ISET pin can be used to drive external fault protection circuits. A resistor in series with a 5.6 volt zener diode to the ISET pin will develop approximately 3.4 volts across the resistor when an overcurrent fault is detected. This signal can be used to trigger external shutdown or hiccup circuitry.

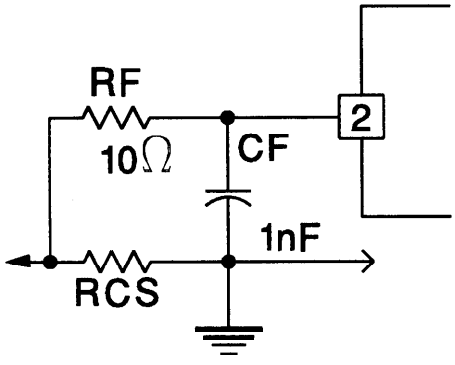


Figure 8.

GATE DRIVE

The UC3852 PWM output section is MOSFET compatible and rated for a one amp peak current. This totem pole design also features a twelve volt (12V) clamped output voltage to prevent excessive gate voltage when used with unregulated (Vcc) supply voltages. A twelve ohm resistor between the UC3852 and the MOSFET switch gate will limit the peak output current to its one amp maximum during normal operation.

Additionally, the UC3852 self biasing active low totem-pole design holds the MOSFET gate low during undervoltage lockout, preventing catastrophic problems at power-up and removal of the AC input.

inductor current and have an insignificant impact on power factor. However, this modification can re

ADVANCED PROTECTION CIRCUITRY

Certain applications of the UC3852 control IC may require sophisticated protection features. Some examples of these options are overvoltage protection and restart delay, soft start or latch-off following a fault. Each of these features can be added to the control circuit with a minimal amount of external parts, and often combined using shared components.

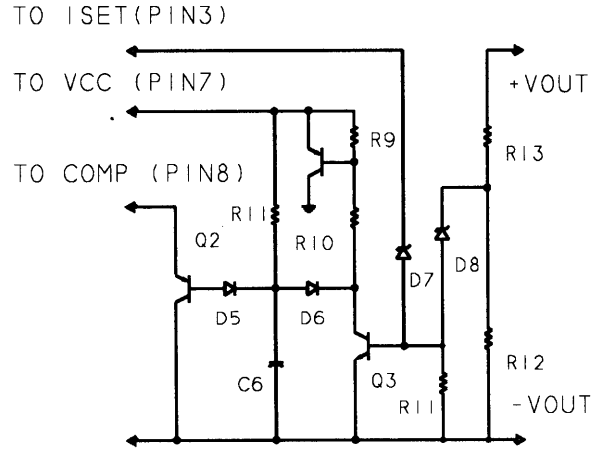


Figure 9.

LIST OF COMPONENTS

C6 = 1 uF, 35V

D5,6 = IN4148

D7= 6.2V ZENER

D8 = 40 V ZENER

Q2,4 = 2N2907

Q3 = 2N2222

R9,10=10K

R11 = 1 MEG

R12 = 24 K

R13 = Calculate for OVP

R14 = 1 K

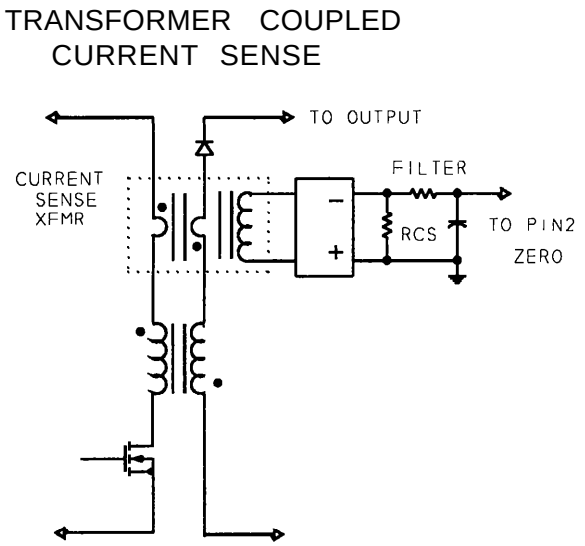


Figure 10.

Soft start is programmed by R11, C6 and the beta of Q2. Overcurrent protection starts at the UC3852 ISET pin which outputs a 9 V signal during a fault. This drives Q3 on through D7 and discharges C6 causing a soft start. Q4 also turns on with this arrangement which discharges Vcc causing a "hiccup". This is optional, and replacing Q3 with an SCR would latch the circuit off until power is reset. Overvoltage protection is attained via R11, R12, R13 and zener diode D8. When enough current flows through the zener (D8), R11 biases transistor Q3. Protection is similar to the overcurrent condition.

Regulated Auxiliary Bias Circuit

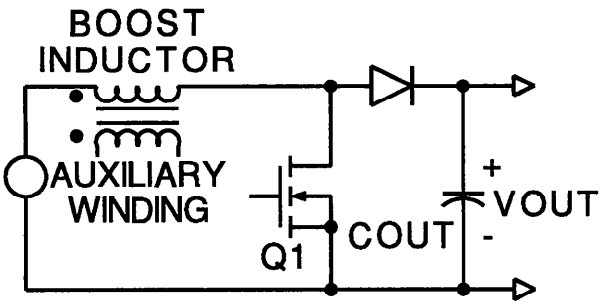


Figure 11.

CURRENT SENSE TRANSFORMERS

A transformer can be used to sense current in most of the UC3852 applications for higher efficiency. Two primary windings are needed to sense each component of the switched current. These may also be unequal in number of turns, depending on the input and output currents (or voltages). A single secondary winding and bridge rectification recreates the total inductor current. A small R/C filter network may be required to smoothen out spikes caused by the leakage inductance.

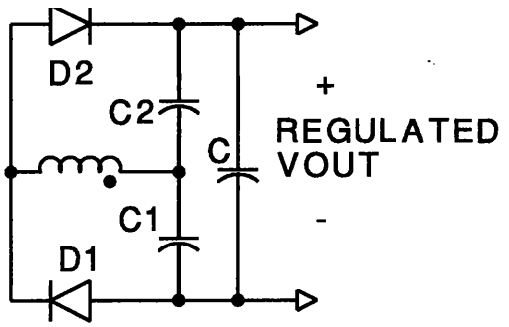


Fig. 12

Universal AC Input Feedforward Circuit

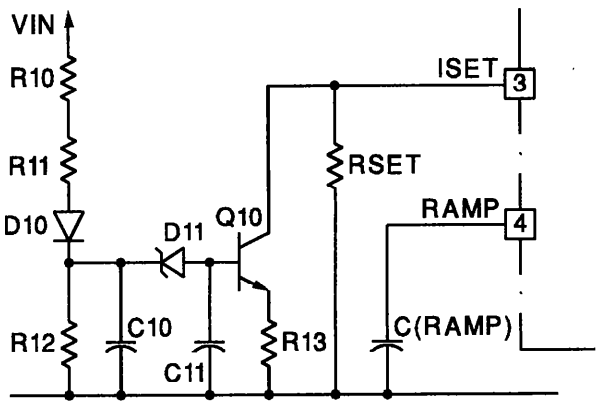


Figure 13.

REGULATED BOOTSTRAP SUPPLY

A regulated auxiliary supply is obtainable with a slight modification to the bootstrap interface and two inexpensive components. This circuit is advantageous in applications which incorporate other control ICs for the main converter or ballast drive sections. A regulated auxiliary voltage is NOT needed for the UC3852 which features a clamped twelve volt (typical) gate drive output voltage. This insures proper drive amplitude for power MOSFETs with an unregulated IC supply voltage to 30 volts.

Dual AC Input Range (110/220 VAC) Feedforward Circuit

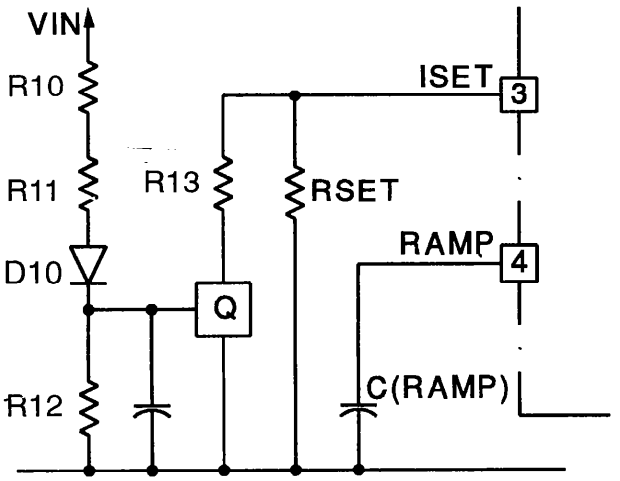


Figure 14.

OTHER PFC APPLICATIONS

The basic PFC schematic of Figure 1 can be used as a template for other PFC applications with different input voltage ranges and output power levels. A majority of the changes will be to accommodate higher (or lower) voltages and currents. Once familiar with the complete design procedure as outlined in this application note, designers are encouraged to recalculate the values for their applications using the same guidelines.

UNIVERSAL AC INPUT RANGE

The UC3852 controlled-on time, zero current switched PFC technique can be used to accommodate wide AC input voltages with the addition of a simple feedforward circuit. This external circuitry is required to cancel out the line dependent changes in the switch on-time over the three-to-one input range from 85 to 264 volts. Otherwise, the approximate nine-to-one control range of the UC3852 on-time would be fully used for line regulation allowing no accommodation for load changes.

CIRCUIT OPERATION

The rectified input voltage is applied across the network consisting of R10 through R12, D10 and C10. Capacitor C10 charges to the peak of the divided input voltage and is large enough to maintain this level over one line cycle. Diode D11 serves as an offset to bypass the range extender circuitry until a sufficient minimum line voltage has been established, typically 80 VAC. Capacitor C11, a small filter capacitor and the base of transistor Q10 reach a voltage of V(C10) minus the Zener forward voltage drop of diode D11. As this voltage rises, the emitter of Q10 and voltage across resistor R13 follows, offset by the base-emitter diode drop of Q10. This increasing bias pulls more current from the UC3852 ISET pin which sits at a fixed voltage. The current in both resistor R13 and resistor RSET is pulled from the UC3852 ISET output. Within the UC3852, the ISET current is mirrored to the RAMP capacitor (Cramp) which is compared to the error amplifier output to determine the ON-time. As the input voltage increases bias to Q10, more current is pulled from ISET thus increasing the RAMP charging current. For a fixed output load, this circuit performs the function of voltage feedforward and can keep the error amplifier output voltage fixed regardless of AC input voltage. This allows the full use of the ICs ON-time control range to accommodate load variations.

FEEDFORWARD CIRCUIT DESIGN

LOW LINE:

ISET = 5V/RSET

t(on)max=8.8*Cramp / ISET

HIGH LINE:

ISET = 5V/(RSET II RI3)

GENERAL:

V(C10) = 1.41*VIN*R12/(R10+R11+R12)

NOTE:V(C10)MAX=5V+Vzener

ISET(MIN)=5V/RSET

ISET(MAX)=ISET(MIN)+5V/R13

FEEDFORWARD BEGINS WHEN:

V(C10)-Vzener-Vbe(Q10) 0V

COMPONENTS:

C10=22uF/16V Q10=2N2222

C11=1nF/16V R10,11=100K

D10=1N4148 R12,13=5.1K

D11=1N5221(2.4V) RSET=51K

CONTINUOUS CURRENT PFC BOOST CONVERTER

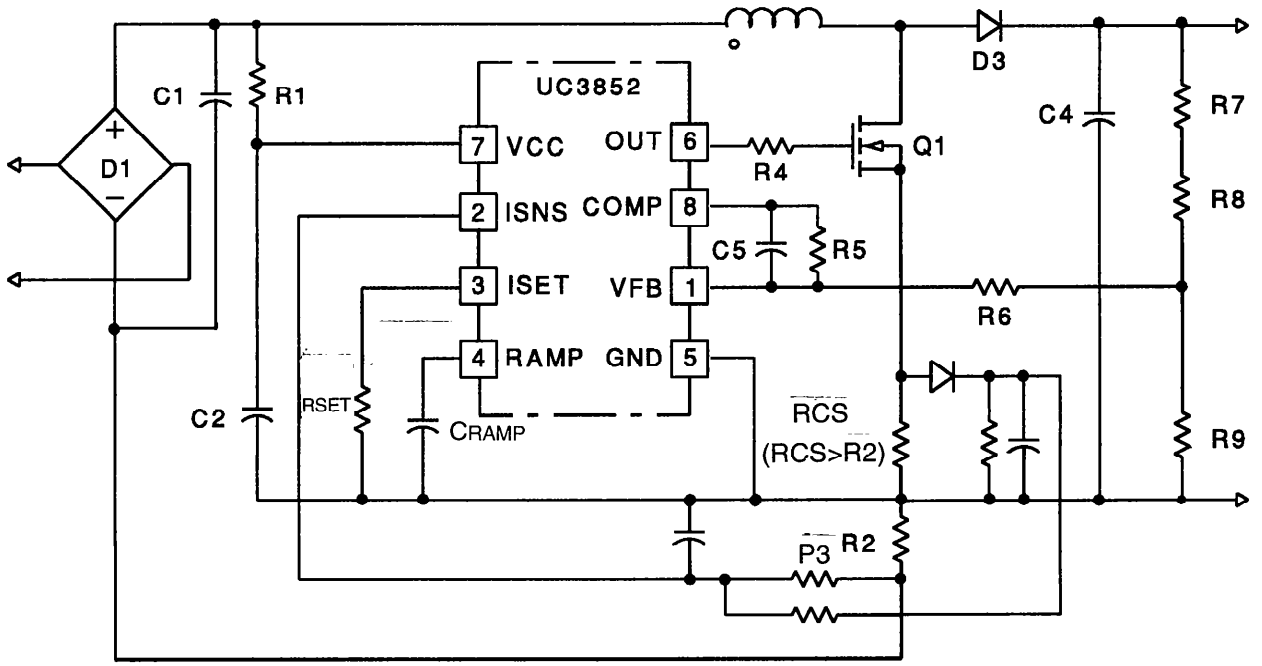


Figure 15.

CONTINUOUS PFC CURRENT IMPLEMENTATION

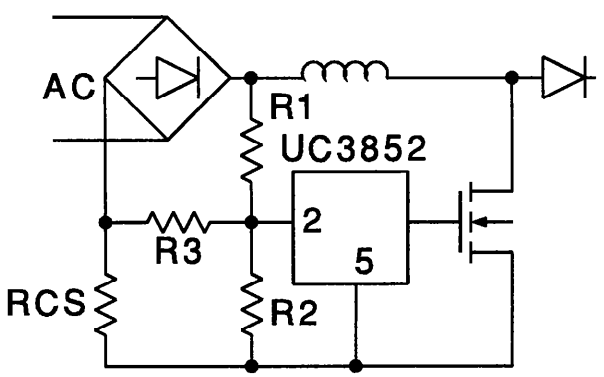


Figure 16.

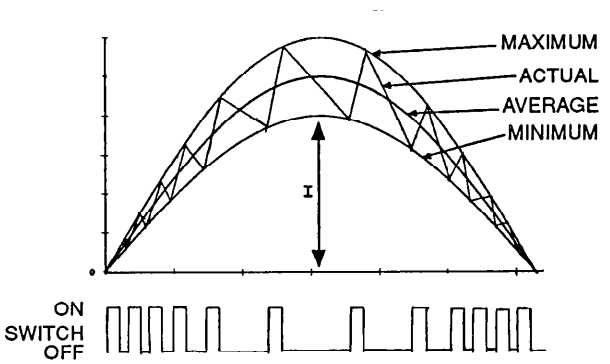


Figure 17.

UC3852 CONTROLLED PFC FLYBACK CONVERTER

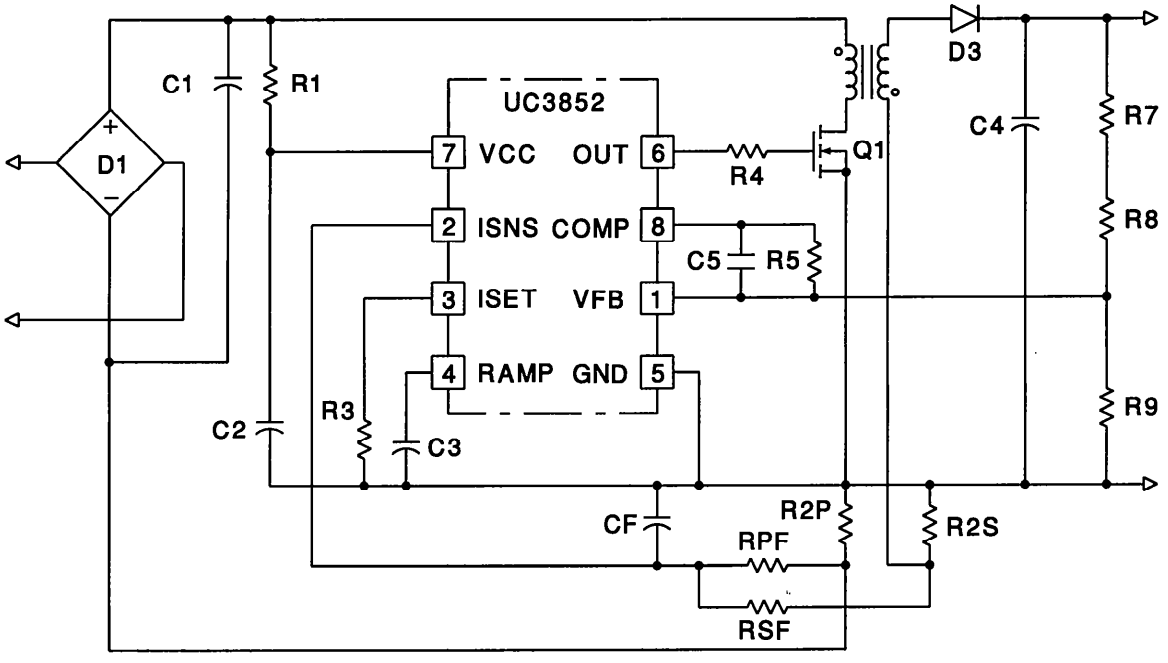


Figure 18.

UC3852 AS A CAPACITIVE DISCHARGE DRIVER

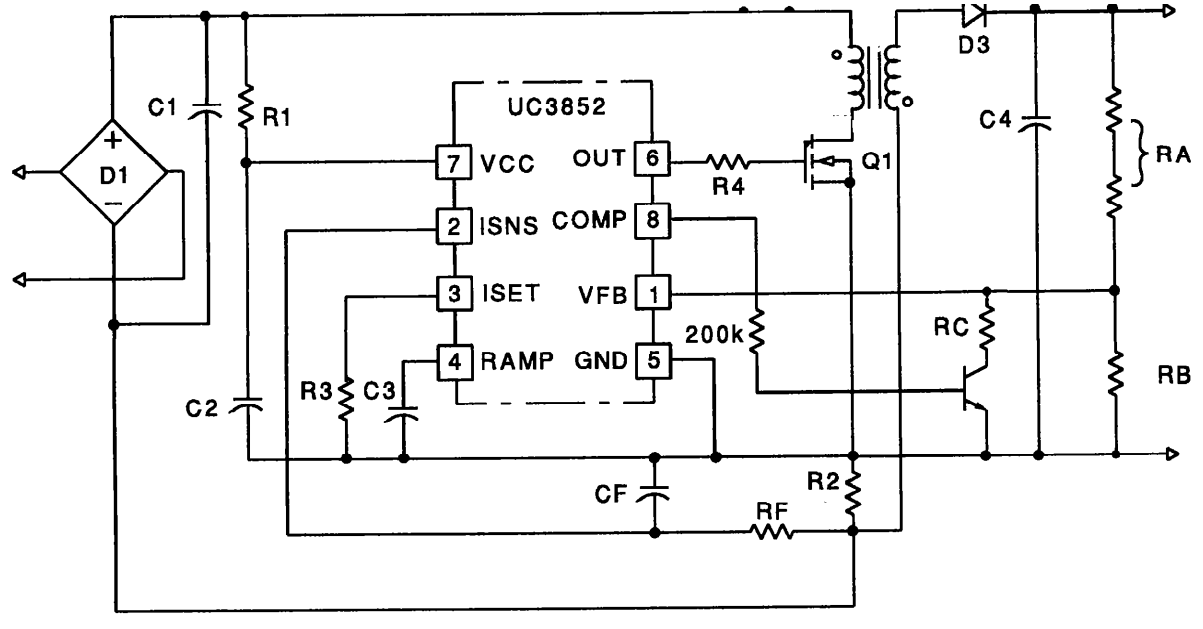


Figure 19.

AUTORANGE (110/220) VOLTAGE FEEDFORWARD CIRCUIT

Input line voltage feedforward can also be obtained with a simple circuit for dual AC input ranges with less demanding load variations. Shown below is a single step autorange circuit for use with the UC3852 timing circuitry. Basically, the TL431 is used as a comparator to switch in a second timing resistor (RSET') when the input voltage exceeds a preset threshold.

The AC input voltage is rectified by diode D20 and 'divided down by resistors R20 and R21. Capacitor C20 peak charges and filters this waveform to develop a DC voltage proportional to the input line. RSET is programming the initial charging current to the timing capacitor CRAMP. When the voltage across C20 exceeds the 2.5 V threshold of the TL431 comparator, its output goes low. This places

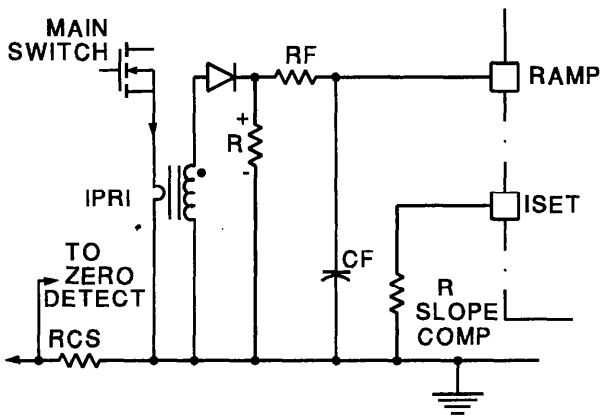


Figure 20.

a second timing resistor, RSET', in parallel with the original one thus increasing the current to CRAMP and performing line feedforward. Resistor values should be selected to switch in the feedforward compensation at approximately 155 VAC which is mid-range between high line of a 110 VAC input (130 VAC) and low line for a 220 VAC input (180 VAC). The value of RSET' must be selected to account for the TL431 output saturation voltage.

CONTINUOUS CURRENT PFC BOOST CONVERTER

The zero current switched PFC technique can also be modified to operate in the continuous inductor current mode. A positive amplitude, small offset signal is derived from the input voltage waveform. It gets added to the normal current sense signal which is negative with respect to ground. Summing these two signals to the ZERO input biases the actual inductor current sense more positive. Therefore, the zero current detection threshold is crossed before the inductor current is actually zero, and the PFC prereguIator operates with continuous current. The exact amplitude of both parts of the inductor current can be determined by adjusting the inductance, on-time, and current sense resistor.

OTHER PFC TOPOLOGIES

The UC3852 can also perform power factor correction using the Flyback topology with a slight degradation to Power Factor. A Flyback topology is commonly used to generate a lower (or much higher) voltage output than the Boost converter. A nonisolated version of this is shown in Figure 18. for simplicity.

A resistor in series with the power return lead senses the inductor charging current while the switch is on, similar to that of the boost converter. However, the discharging current information is lost when the switch is off while the stored inductive energy is delivered to the output. A second current sense resistor is added in series with the secondary winding as shown to recover this information. A small amount of filtering may be necessary to smoothen out switching noise spikes while summing the current sense signals.

Good regulation of the output voltage will be obtained with this technique although some 120 Hz (2 x line frequency) ripple is to be expected. The flyback circuitry cannot fully transfer power when the input line voltage goes down near zero each cycle. This approach has numerous applications where a small amount of power supply ripple is acceptable. Post regulator circuits can be added to improve regulation if necessary.

CAPACITIVE DISCHARGE CIRCUITS

The UC3852 can also be used in capacitive discharge circuits, typical of photoflash and strobe applications. In fact, the circuit shown below will provide the minimum recharge time for a given peak input current. Zero current switching insures that the next switching cycle is initiated as soon as the inductor current discharges to zero. There is no deadtime between conversion cycles and the output is charged as quickly as possible for the programmed maximum inductor current.

Regulation is achieved by using a burst mode of operation where the UC3852 stops delivering output pulses when the output voltage setpoint is reached. Operation will begin again when the output voltage drops below the lower programmed threshold. Both of these thresholds are pro-

grammed by Ra, Rb and Rc according to the following formulas.

Vout(max) = (5*(Ra+Rx))/Rx

Vout(min) = (5*(Ra+Rb))/Rb

where Rx=(Rb*Rc)/(Rb+Rc)

NON PFC APPLICATIONS USING VARIABLE FREQUENCY OPERATION

Conventional PWM (non PFC) applications using a variable frequency control techniques can also be implemented with the UC3852. This applies to both current mode and variable ON-Time control methods. Typical examples of these are discontinuous current boost and flyback converters. Variable frequency operation is popular in numerous applications as it can minimize the peak current in comparison to fixed frequency designs. The zero current detection and switching technique of the UC3852 should be used in its standard configuration with current sensed below ground, although a current transformer can be introduced.

IMPLEMENTING CURRENT MODE

The ICs RAMP input will be used as the current sense input to be compared to the error amplifier output for current mode control. A current transformer is recommended to fully utilize the 9 volt compliance of this pin. This implementation allows for a wide load swing with maximum noise immunity. The RAMP pin gets discharged by internal IC logic to 0.2 V at the end of each ON-time. Therefore, some series impedance to the current sense resistor is recommended to keep load current outside of the IC. Any filter capacitor to suppress the switch leading edge noise spike will also get discharged. The ramp pin does not need a programming resistor, but one could be used to introduce optional slope compensation via the filter capacitor.

VARIABLE ON-TIME CONTROL

The switch ON-Time can also be controlled by comparing a sawtooth ramp to the error amplifier output. Configuration of this is basically identical to the standard PFC application using a RAMP capacitor and resistor to program the maximum ON-Time. Error amplifier compensation is likely to be much different and utilize a much higher loop crossover frequency than its PFC counterpart. The ICs error amplifier is similar to a '741 type general purpose OP-AMP and is programmed accordingly.

REFERENCES and ADDITIONAL INFORMATION:

1. ANDREYCAK, W. : "Controlled ON-Time, Zero Current Switched Power Factor Correction Technique"; UNITRODE Power Supply Design Manual SEM-800.

2. AHMED, SAEED, : "Controlled On-time Power Factor Correction Circuit with Input Filter"; Thesis, Virginia Polytechnic Institute.

3. MAMMANO, BOB and DIXON, LLOYD: "Designing High Power Factor Systems - Choosing the Optimum Circuit Topology", PCIM Magazine, March 1991.

PERFORMANCE EVALUATION

The UC3852 controlled PFC circuit shown in Figure 1 was constructed using the list of materials provided for this application. Power Factor and Total Harmonic Distortion to the 50th harmonic were measured using a VOLTEC PM- 3000 AC power analyzer. Test results indicated a power factor of 0.998 and T.H.D. below 6% at nominal line and full load. Very similar readings were obtained over the complete input voltage range and a moderate load change. Zero Current Switching (ZCS) facilitates high overall efficiency with this PFC technique.

UC3852 PFC TEST CIRCUIT

SPECIFICATIONS:

VIN = 85 TO 135 VAC

VOUT = 350 VDC

POUT = 86 W

MEASURED PERFORMANCE:

P.F. = 0.998

T.H.D. = 5.81%

TEST CONDITIONS;
(nominal line)
VIN = 115.7 VAC
IIN = 0.799 AAC
PIN = 92.13 W
VA IN = 91.84
INRUSH Ipk = 17.7 A
VOUT = 355.6 VDC
IOUT = 0.242 ADC
POUT = 86.1 W
EFFICIENCY = 93.45 %

C U R R E N T :
HARMONIC CONTENT
1st : 0.775 Amp
3rd : 3.91%
5th : 0.82%
7th : 0.38%
9th : 0.35%
11th: 1.30%
13th : 0.21%

LIST OF MATERIALS

CAPACITORS
C2 = **0.47** uF / 200 V
C3 = 82uF / 400 V
C4 = 22uF / 35 V
C5 = 0.1uF / 35V
C6 = 1nF / 16V
c7 = 0.1uF / 16V

DIODES
D1-4 = 1N4004, 1A / 400 V
D5 = 1N4937, 1A / 600 V
trr = 200ns
D6 = 1N4148, 0.2 A / 50 V

INDUCTORS
L2 = 1 mH Boost inductor
L3 = Several turns on L2 to
provide 20 VDC supply voltage

RESISTORS
R1 = 100 k ohms 1 Watt
R2 = 0.1 ohm 1 W non-inductive
R3 = 18.2 k ohms 1% 1/2 W
R4 = 1 meg ohm 1/4 W
R5 = 330 k ohms 1% 1/2 W
R6 = 390 k ohms 1% 1/2 W
R7 = 10 k ohms 1% 1/4 W
R8 = 20 k ohms 1/4 W
R9 = 10 ohms 1/2 W non-inductive

TRANSISTOR
Q1 = IRF830 500 V / 4 A

INTEGRATED CIRCUIT
U1 = UC 3852

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7 CONTINENTAL BLVD. ¡MERRIMACK. NH 03054
TEL. (603) 424-2410 ¡FAX (603) 424-3460

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