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## ***Optimizing the UCC28019A to Avoid Audible Noise***

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### ABSTRACT

The UCC28019A and its predecessor, the UCC28019, are eight-pin active power factor correction (PFC) controllers that use the boost topology and both operate in continuous current conduction mode. Despite having few pins, the UCC28019A and the UCC28019 offer many protection features, such as output over-voltage and under-voltage protection, peak current limit, open-loop detection, and input brown-out. These features require few external components while providing tight output voltage regulation with low harmonics and minimal input current distortion.

PFC circuits are traditionally optimized at maximum load, providing the power system with a low-distortion input current waveshape when it is most needed. It is easy to assume that during light-load, or no-load, the input current from the mains would be so low that less than ideal PFC would not have much of a system impact. The UCC28019A performs well at full load, and with careful attention to circuit design, light-load and no-load performance can be optimized as well.

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### ***UCC28019A compared to UCC28019***

Of the two available devices, which would be the preferred controller for a given application? The UCC28019A PFC controller is a pin-for-pin compatible drop-in replacement for the original UCC28019 controller. The exact same design procedure applies to both devices and the steady-state behaviors of both remain unchanged. A socket that was originally intended for the UCC28019 can be successfully filled by the UCC28019A with no changes to the overall circuit. So what features differentiate the two from each other?

The UCC28019A improvements become evident during start-up and transient conditions. During UCC28019A start-up a pre-charge current from VCOMP will charge the external capacitor-resistor network to 1.9 V as soon as VCC exceeds the turn-on threshold, VINS exceeds the input brown-out detection threshold, and VSENSE crosses its enable threshold. When VCOMP reaches 1.9 V, the precharge current reduces to a constant 30  $\mu$ A until the voltage signal at VSENSE is equal to 85% of its targeted regulation value, then the VCOMP source current decreases linearly, reaching zero when VSENSE indicates that the output is within 99% of the regulation voltage level. At this point, the circuit is out of soft-start mode and begins normal operation and the enhanced dynamic loop response is enabled. The UCC28019 version also had an effective turn on by initially adjusting VCOMP with a 2-V step and ending soft-start at 75% of the regulated output voltage, thereby activating the non-linear enhanced dynamic loop response sooner than

the “A” version. This sudden increase in the current loop gain of the UCC28019 by the instantaneous 2-V step and more demand for dynamic response is a faster start-up but may cause audible noise. Both start-up methods are effective but the UCC28019A version results in less input current distortion and is usually preferred.

The response to a transient condition is also softened in the UCC28019A because this device uses a continuous gain change in the voltage error amplifier as opposed to the UCC28019’s sudden step change. Although the input current was only briefly distorted during transients with applications using the UCC28019, this distortion, and the resultant audible noise, is avoided with the UCC28019A.

Open-circuit protection was added to the ISENSE pin of the UCC28019A. ISENSE has an internal 1.5- $\mu$ A pull-up current which will trigger a fault condition and shut down the controller if the ISENSE pin is open-circuited. If the ISENSE pin of the UCC28019 is opened, the response would be the same as if it were shorted to ground. The controller would demand maximum duty cycle and an output over-voltage condition would result, with erratic current spikes on the input.

### ***Avoid Audible Noise at Light Load and No-Load Operation:***

Power factor correction, PFC, is crucial to reduce power losses and minimize harmonics for high power converters powered off the AC mains. Because the primary concern is at full load, PFC circuits are customized for this operating point. Operation at light-load and no-load operation will not lead to increased self-heating in the neutral line conductor or increase the dielectric stresses in the capacitors and cables that the PFC circuit is designed to address. Because the main purpose of the PFC circuit is not critical at light-load conditions, it has not been the traditional focus for optimal performance. Although not required for no-load operation, the performance of the UCC28019A PFC stage can be enhanced with the addition of a small bias current to the current compensation node.

The strategy of the UCC28019A compensation is a non-linear dynamic response to changes in the line and load conditions, governed by the voltage on the ICOMP pin and compared to an internal ramp signal that is set by VCOMP. At no-load and very light load, the voltage loop compensation pin, VCOMP, will settle to approximately 1.5V which maximizes the current amplifier gain and sets the internal slope of the ramp signal to near zero. The internal voltage ramp will be very shallow. If the voltage on the current loop compensation pin, ICOMP, is higher than the peak voltage of the internal ramp there will be zero duty cycle. This is because GATE pulses are initiated when  $V_{RAMP}$  intersects ICOMP; at no-load conditions the ramp signal is very shallow and does not intersect the ICOMP signal, resulting in the desired PWM duty cycle that is zero, refer to Figure 1.

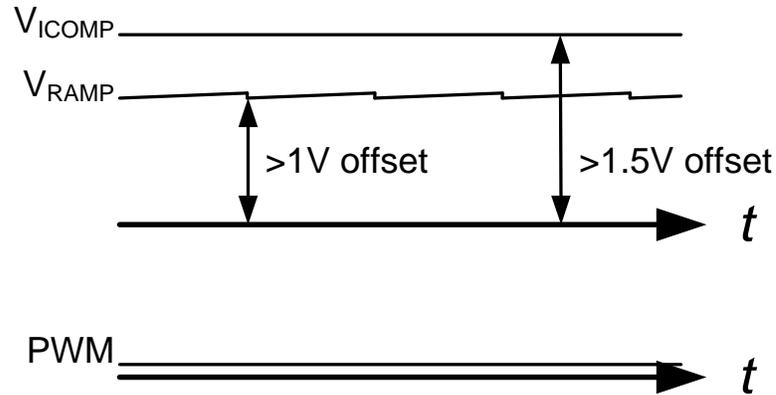


Figure 1. During no-load operation, the  $V_{RAMP}$  signal is very shallow and does not intersect  $V_{ICOMP}$  resulting in no PWM pulses.

As expected, with no PWM pulses to the gate driver, the output voltage will eventually fall and cause  $V_{COMP}$  to rise which then increases the slope on  $V_{RAMP}$  and also reduce the internal current amplifier gain. As the  $V_{RAMP}$  slope increases and the current amplifier gain decreases, intersection of the  $V_{RAMP}$  and  $V_{ICOMP}$  occurs at the ramp signal peaks and very narrow PWM pulses are generated, refer to Figure 2. Enough current is supplied to the output by these narrow pulses to keep the output voltage well regulated. Narrow pulses are sufficient to maintain the desired output voltage but do not carry enough energy to create audible noise.

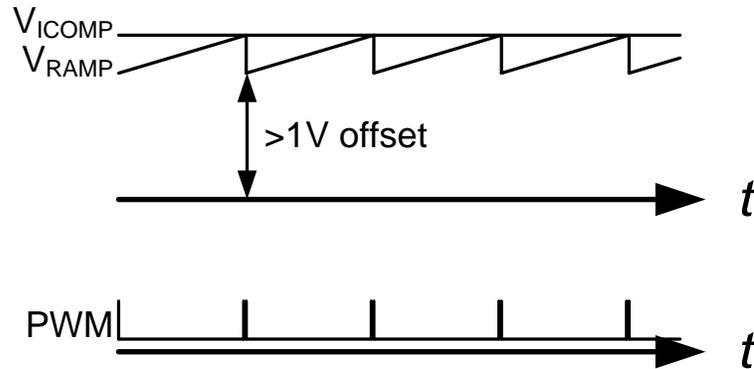


Figure 2. Eventually, during no-load, the falling output voltage will require narrow PWM pulses to maintain regulation, the rising  $V_{RAMP}$  signal intersects  $V_{ICOMP}$  and very narrow PWM pulses result.

But process variations and semiconductor parametric shifts internal to the device can result in a condition in which the ICOMP voltage signal may not rise high enough to be above the  $V_{RAMP}$  voltage. This would only be evident in the precise operating conditions that are seen during no-load operation and would have negligible influence during other load conditions. If it happens that, at no-load, the internal voltage of the current loop compensation, ICOMP, is lower than the peak voltage of  $V_{RAMP}$ , the ramp signal will intersect with the ICOMP signal and, instead of the ideal zero duty cycle at no-load, PWM pulses will be generated, refer to Figure 3.

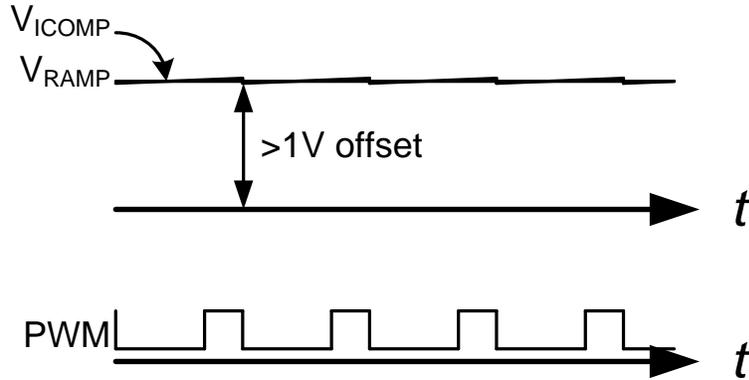


Figure 3. Process variations may result in PWM pulses at no-load.

The PWM pulses will cause large currents that will make the voltage on ICOMP rise and eventually increase the output voltage. This will force the PWM pulses to stop until  $V_{ICOMP}$  falls and intersects the shallow slope of  $V_{RAMP}$ . This leads to wide PWM pulses that carry enough energy to create audible noise. Also consider that the excess charge from these wide pulses will drive the output inot over-voltage and result in increased output voltage ripple, see Figure 4.

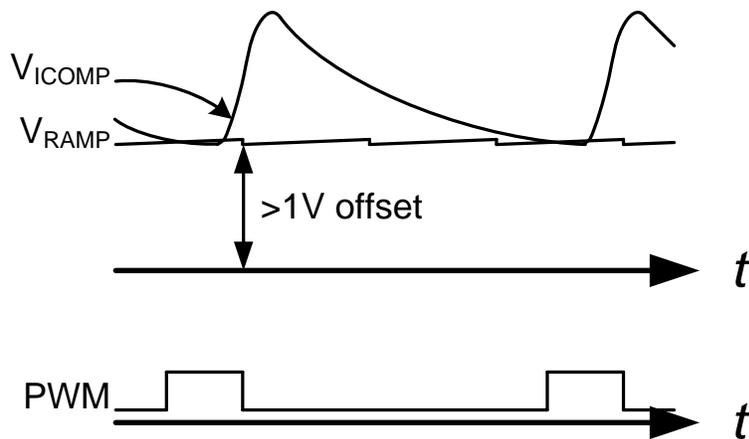


Figure 4. The wide PWM pulses carry enough energy to create audible noise.

In order to achieve the desired narrow PWM pulses and eliminate audible noise at no-load conditions, a small bias current can be superimposed into the ICOMP pin. This superimposed bias current will raise the ICOMP voltage just enough to be above the  $V_{RAMP}$  signal at no-load and achieve the desired zero duty cycle, refer to Figure 5.

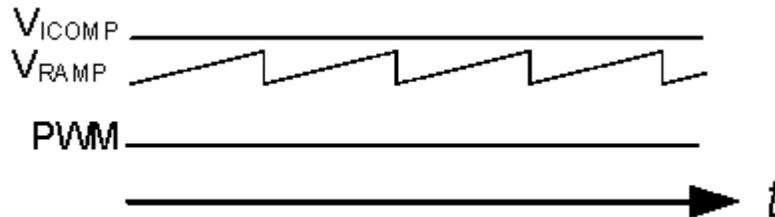


Figure 5.  $V_{ICOMP}$  is raised by an external bias current into the ICOMP pin to eliminate the wide PWM pulses at no-load.

It only requires an offset current on the order of 6 to 7  $\mu\text{A}$  into ICOMP to restore the narrow PWM pulses and smooth quiet operation of the PFC circuit under no-load conditions. The most effective way to do this is to add an external resistor between VCC and ICOMP. With a regulated 12 V bias on VCC, a 1.5 M $\Omega$  resistor from VCC to ICOMP is usually enough bias current to optimize no-load performance for most devices, as shown in Figure 6. Using a smaller external resistor to provide more bias to ICOMP should be avoided as too much offset current into ICOMP will increase the total harmonic distortion, THD, of the converter.

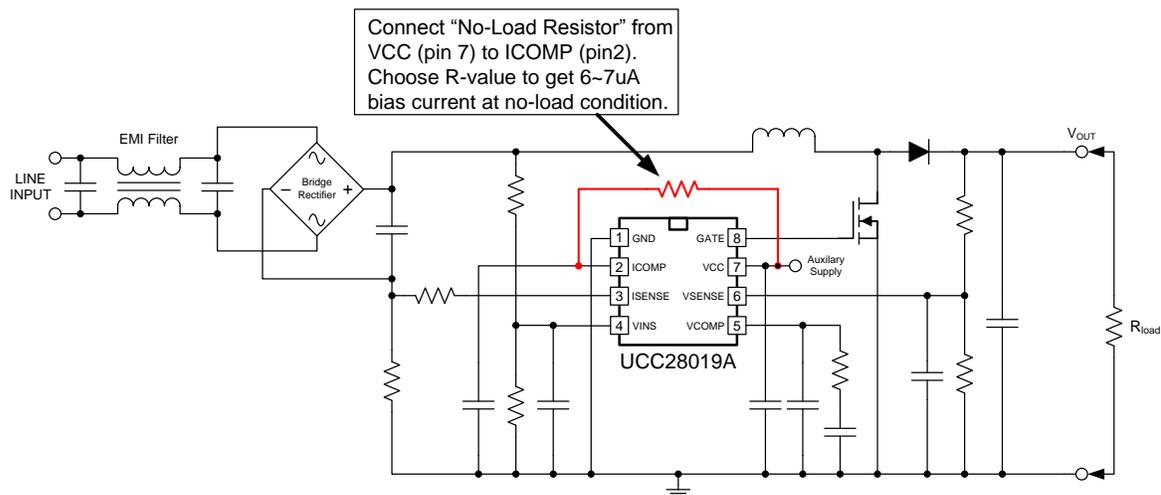


Figure 6. Recommended placement of the external resistor from VCC to ICOMP to add the desired offset current for robust no-load operation.

**Avoid Bursts of Audible Noise Due to OVP During Normal Operation**

Some UCC28019A designs may experience short bursts of audible noise during start-up and load transients. The most prevalent cause of this audible noise is because the over-voltage protection, OVP, is activated. The UCC28019A and the UCC28019 both have OVP thresholds internally set to 105% of the output regulation voltage. If VSENSE detects that this threshold has been reached, the standard control loop is bypassed and the GATE is immediately disabled until VSENSE falls below the 105% detection threshold. This hard-stop can occur during start-up or when the load is reduced quickly, an “un-load step”, and produce short bursts of audible noise.

Low PFC output capacitance will allow high output ripple voltage and make it easy for VSENSE to hit the OVP threshold during start-up and during an un-load step. Because the OVP response is a hard-stop limit, it shuts off pulse width modulation when VSENSE exceeds the OVP threshold and resumes when VSENSE falls below the threshold. With almost no hysteresis, the system can hit OVP multiple times until VCOMP falls low enough to reduce the output power being delivered so that VSENSE no longer crosses the OVP threshold. Increasing the output capacitance will prevent hitting OVP at start-up or at least minimize its duration. This simple fix of adding more output capacitance may be all that is needed.

During an “un-load step” VCOMP programs the PFC to deliver more power than the load can absorb. VCOMP adjusts slowly with respect to the reduction in load, leading to an over-charge of the output capacitor. OVP immediately stops delivery of power but lack of hysteresis will result in chatter if OVP is triggered multiple times. Additional circuitry is shown in Figure 7 that will prevent the output from overcharging and avoid OVP during an un-load step if it is absolutely required to avoid OVP completely.

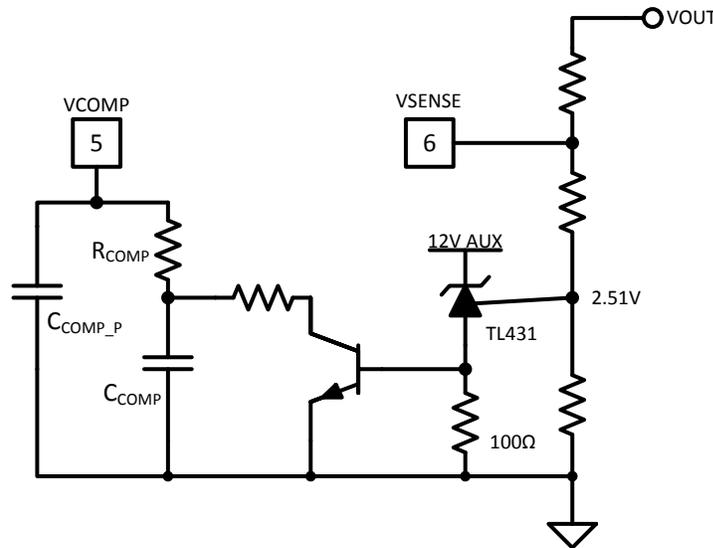


Figure 7. Suggested external circuit to avoid audible noise due to OVP.

Referring to Figure 7, when the output voltage rises to just over its regulation value, but before OVP is triggered, the current will begin flowing in the TL431, turning on the NPN transistor, which will discharge  $C_{COMP}$  slightly. This will flatten out the internal  $V_{RAMP}$  slope and help keep VOUT from rising more, avoiding the OVP threshold. The circuit must be

designed such that the TL431 turns on before the output rises to 105% of its regulation value for this to be successful.

If audible chatter is consistently present, this is a clear indication that the amount of output capacitance is insufficient and is not maintaining the output voltage ripple below 5%, and the OVP threshold is being reached at every half-line cycle. The simplest solution to avoid this situation is to use an adequate amount of output capacitance, taking into account capacitance tolerance over temperature, so that the output voltage remains within the regulation value under all normal operating conditions.

### CONCLUSION

By adding a small offset current into ICOMP, audible noise can be avoided in the UCC28019A and UCC28019 during no-load operation. This small offset, provided by a resistor from VCC to ICOMP, will achieve the desired narrow PWM pulses and eliminate audible noise at no-load conditions. Audible noise at start-up or un-load steps can be avoided by increasing the output capacitance of the PFC, avoiding the non-hysteretic over-voltage protection response. Maintaining the output voltage ripple below 5% of the regulation voltage is required under all operating conditions in order to avoid OVP.

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