TPS330x Supervising DSP and Processor Applications

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ABSTRACT

This application report describes the TPS330x–xx supply-voltage supervisor (SVS) families of devices. The report gives a general introduction on generator resetting, followed by an overview of the technical parameters and the special features of the TPS330x. Each feature is discussed separately. Measurements make it easy to understand SVS principles of operation. Typical applications that increase system reliability, such as supervising a dual-voltage DSP, are included. Layout and design issues are also discussed.

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1 Introduction

A digital system must be forced into a definite initial state after power-on. Digital-signal processors (DSPs) and microprocessor applications provide a reset input for this purpose.

In the simple application shown in Figure 1, an RC network is connected to the $\overline{\text{RESET}}$ input to deliver the necessary reset pulse. After switching on the power supply, this circuit keeps the logic level at the $\overline{\text{RESET}}$ input low for a time determined by the capacitor and resistor values. This delay time, required by the system to complete the initialization, allows the power supply to become stable.

This RC network, however, has some disadvantages. In cases of brief reductions of the supply voltage, it does not work correctly. It does not recognize spikes, because the voltage at the $\overline{\text{RESET}}$ input does not decrease as fast as the supply voltage due to the capacitor. Malfunction is thus possible. The capacitor can be discharged quickly through the diode only if V_{DD} decreases by more than 0.7 V. A small decrease in V_{DD} can destroy the contents of memory and internal registers without activating the reset circuit.

A small decrease in V_{DD} can destroy the contents of memory and internal registers, as well as cause software malfunction, which may fall into an infinite software loop state without activating the reset circuit.

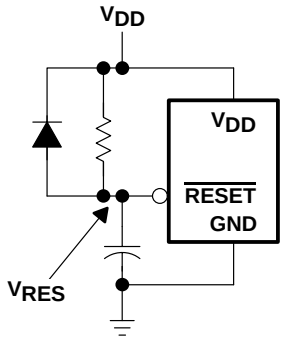


Figure 1. A Simple Reset Solution

If the reliability of a processor-based system is very important, several features are available to prevent errors: power-fail interrupts can signal dangerous conditions in time, a battery backup can protect the content of the memory, and so on. In smaller systems this may be too expensive, and, in most applications, it is not required. It is usually sufficient to force the system into a defined initial state after a considerable voltage drop.

To implement this function while preventing problems, the following circuit capabilities are required:

- Accurate detection of a voltage drop below the critical voltage
- Generation of a reset signal when the supply voltage is not in the allowed range

- Capability to hold the reset signal active for a definite time after the supply voltage has returned to its nominal value to ensure proper system initialization

The Texas Instruments TPS330x family of integrated circuits fulfills the requirements described above without the need for external components†. Some versions provide the system with additional features.

2 Circuit Description

This section describes the TPS330x circuits and features.

2.1 Overview of Features

Figure 2 gives an overview of the TPS330x features.

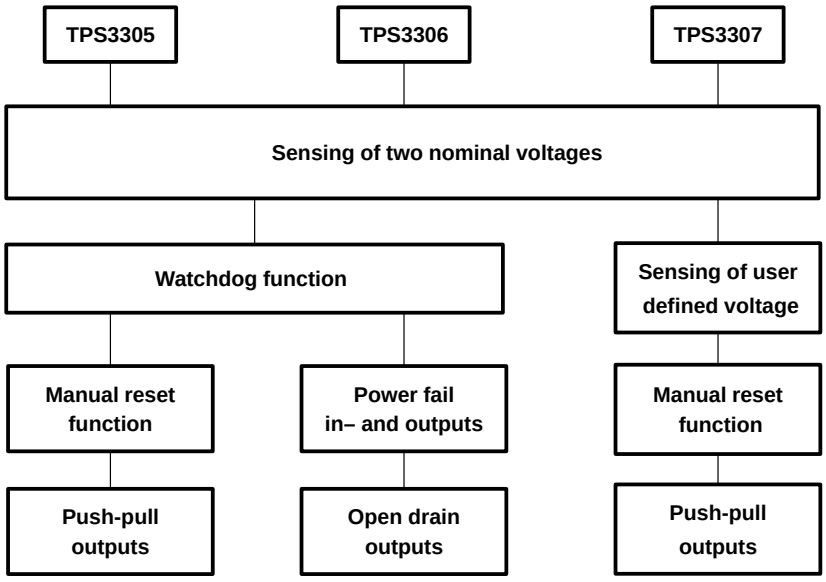


Figure 2. Features Overview

2.2 Supply Voltages Supported

All three TPS330x families are designed to supervise two defined voltages. The TPS3307 can also control a third voltage, which is individually adjustable and internally connected to the reset-logic circuit. A separate power-fail in– and output is provided by the TPS3306; this provides a separate comparator-output connector. The TPS3307 provides an $\overline{MR}$ pin. Table 1 lists the fixed voltages and their typical threshold voltages.

†An external resistor is required on the TPS3306-xx if the microprocessor does not provide a pullup resistor at its input stage.

Table 1. Supported Voltages

DEVICE	SENSE1 VOLTAGE	THRESHOLD VOLTAGE	SENSE2 VOLTAGE	THRESHOLD VOLTAGE
TPS330x-33	5 V	4.55 V	3.3 V	2.93 V
TPS330x-25	3.3 V	2.93 V	2.5 V	2.25 V
TPS3306-20	3.3 V	2.93 V	2.0 V	1.85 V
TPS330x-18	3.3 V	2.93 V	1.8 V	1.68 V
TPS3306-15	3.3 V	2.93 V	1.5 V	1.40 V

2.3 Package Information

The TPS330x is available in two different packages: the SO (small outline) and the MSOP package (microsmall outline). Terminal numbering is the same for both packages. The pin assignment is shown in Figure 3.

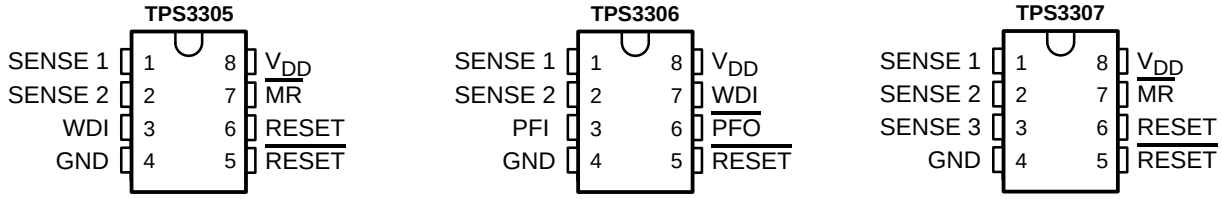


Figure 3. Pin Assignments of the TPS330x

2.4 Pin Functions

Table 2 lists and describes the functions of the TPS330x pins.

Table 2. Functional Overview and Description

PIN NAME	PIN NO.	STATUS	DESCRIPTION
GND (all devices)	4	Negative power supply	Connects the circuit to ground. This is the zero-volt reference for all signals.
$\overline{\text{MR}}$ (TPS3305, TPS 3307)	7	Logic output, active-low	Manual reset. To trigger a reset pulse by an external component (e.g. a pushbutton can be connected to this terminal.)
$\overline{\text{PFO}}$ (TPS3306)	6	Logic output, active-low	Power-fail output. Logic level output of comparator weighting
$\overline{\text{RESET}}$ (all devices)	5	Logic output, active-low	The output with a active-low reset signal
RESET (TPS3305, TPS 3307)	6	Logic output, active-high	Output with an active-high reset signal
SENSE1 (all devices)	1	Analog Input	Supervises the first voltage
SENSE2 (all devices)	2	Analog Input	Supervises the second voltage
SENSE3 (TPS3307)	3	Analog Input	Supervises the third voltage adjusted by an external resistive divider
PFI (TPS3306)	3	Analog Input	Power fail input. A comparator is weighting an external voltage with the internal 1.25-V reference voltage. The logic output is shown at $\overline{\text{PFO}}$.
WDI (TPS3305, TPS3306)	3, 7	Edge-sensitive input	Watchdog input. The watchdog input is used to reset the internal timer by a positive or negative transition.
V_{DD} (all devices)	8	Positive power supply	Supplies power to the circuit

2.5 Block Diagram

Figures 4 to 6 show a block diagram of the TPS330x derivatives. The main part of the voltage supervisory circuit is a very stable, temperature-compensated band gap reference voltage source. The voltages at SENSE1 and SENSE2 are divided by internal resistor dividers and compared with the reference voltage by a comparator. The SENSE3 input is directly compared with $V_{\overline{REF}}$ = 1.25 V. This is also true for the PFI pin. The only difference is its output is connected to a $\overline{PFO}$ pin instead of being connected to the reset logic. The sum of the two resistor values between SENSE input, the comparator input, and ground is 1.2 MΩ for SENSE1 and 1 MΩ for SENSE2 for all devices. Table 3 lists the nominal values.

Table 3. Values of the Internal Resistive Dividers

CIRCUIT	SENSE1	R1 TYP	R2 TYP	SENSE2	R3 TYP	R4 TYP
TPS330x-33	5 V	870 kΩ	330 kΩ	3.3 V	573 kΩ	427 kΩ
TPS330x-25	3.3 V	688 kΩ	512 kΩ	2.5 V	444 kΩ	556 kΩ
TPS3306-20	3.3 V	688 kΩ	512 kΩ	2.0 V	324 kΩ	676 kΩ
TPS330x-18	3.3 V	688 kΩ	512 kΩ	1.8 V	256 kΩ	744 kΩ
TPS3306-15	3.3 V	688 kΩ	512 kΩ	1.5 V	107 kΩ	893 kΩ

If there is a low signal at the manual reset ($\overline{MR}$) terminal, the $\overline{RESET}$ output is also triggered. If the $\overline{MR}$ input is unconnected, an internal 14-kΩ pullup resistor pulls it up to V_{DD}.

The watchdog input (WDI) is supervised by a transition detector to reset the watchdog timer at each positive or negative transition. If this input is not electrically connected, an internal driver with a 40-kΩ resistor delivers the necessary transitions in time, so that $\overline{RESET}$ is not asserted.

The reset timer and the watchdog timer are both clocked with a common internal oscillator.

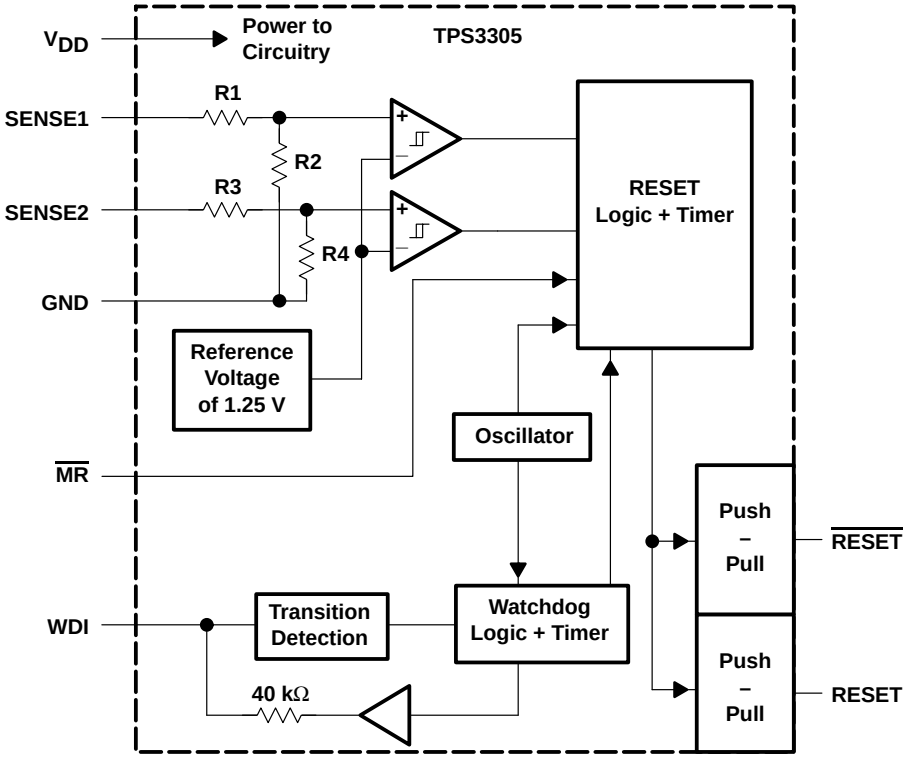


Figure 4. Block Diagram of the TPS3305

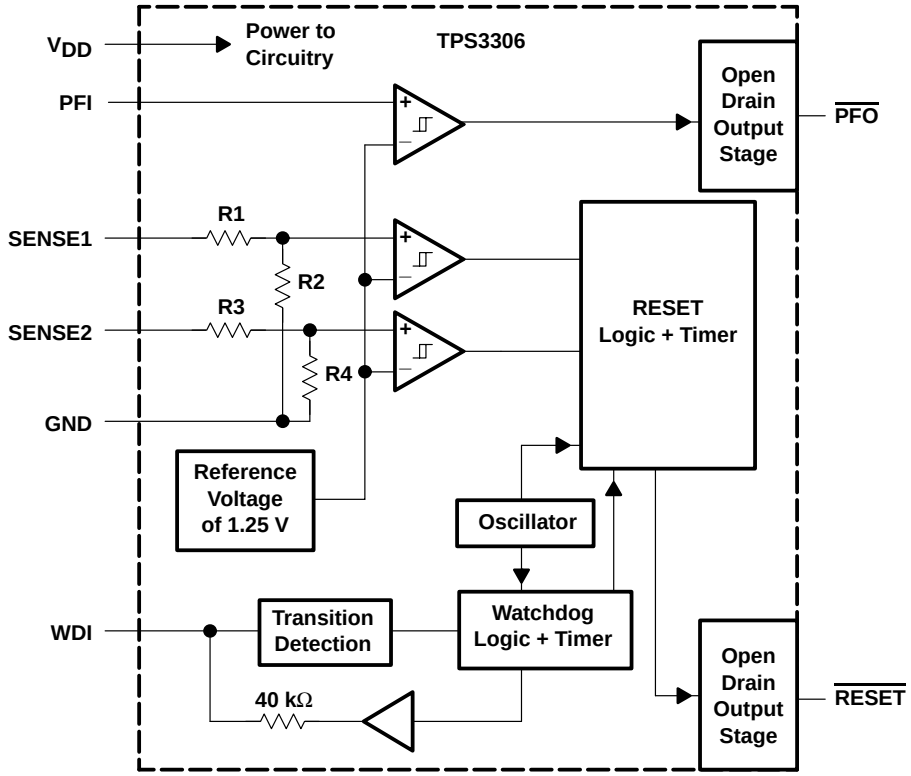


Figure 5. Block Diagram of the TPS3306

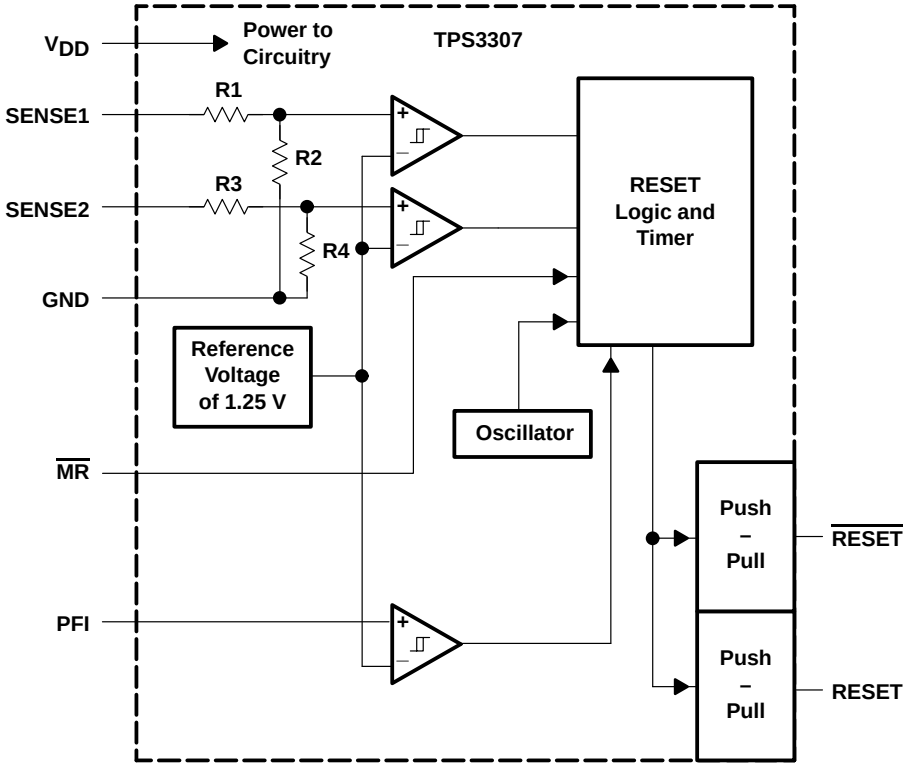


Figure 6. Block Diagram of the TPS3307

2.6 Basic Timing

Figure 7 summarizes the different reasons for a reset and shows the most important timing parameters. A general SENSEn input represents the various SENSE inputs. The diagram is valid at a constant supply voltage V_{DD} of 5 V.

The time-out has a typical value of 1.6 s; the delay time t_d is typically 200 ms, while the TPS3306 has a time-out period of 0.8 s and a typical delay time of 100 ms. The negative-going threshold voltage V_{IT-} approximates the nominal voltage V_{nom} minus 10%. Table 1 lists all possible values.

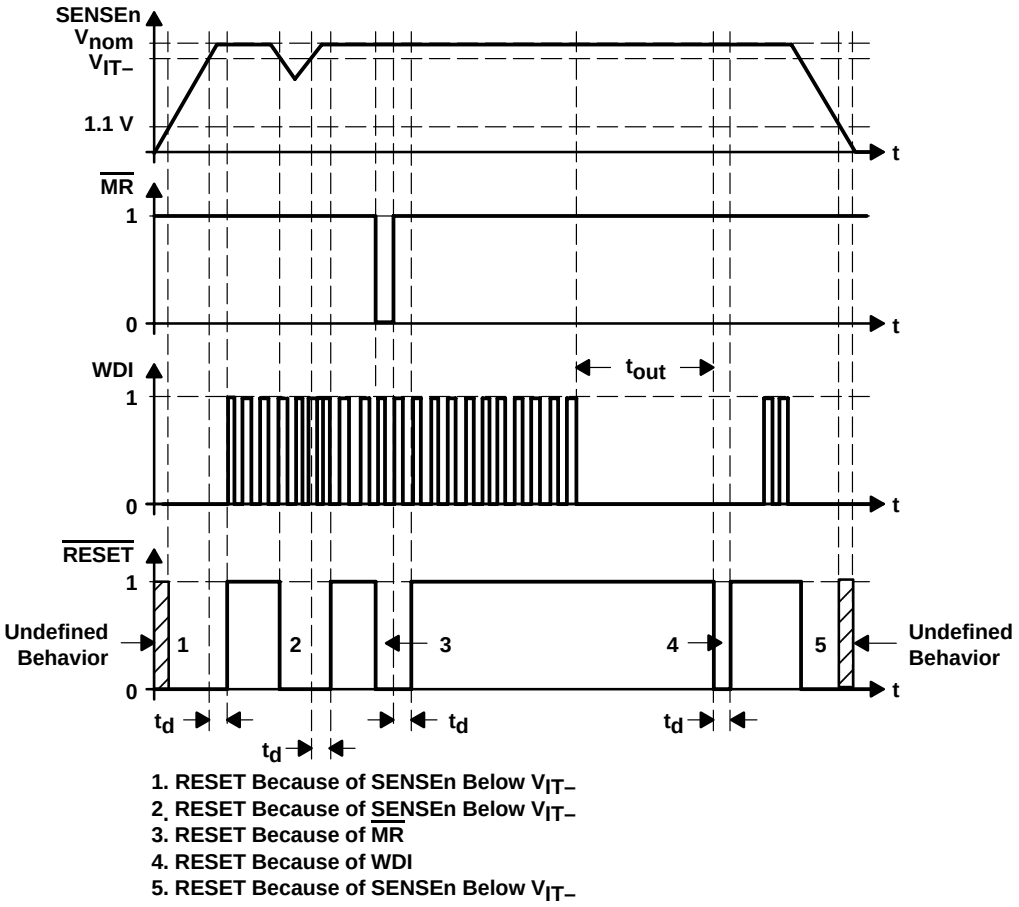


Figure 7. Basic Timing of the TPS330x

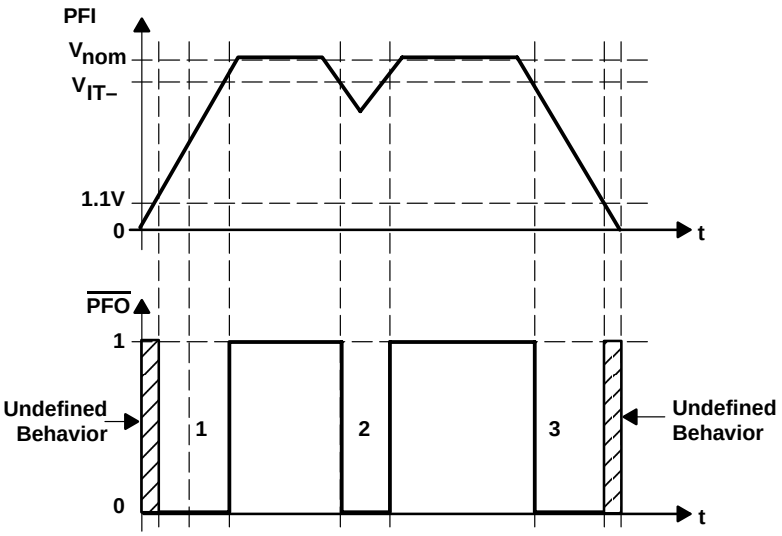


Figure 8. PFI and $\overline{\text{PFO}}$ Basic Timing

3 SENSE Inputs and RESET or Power-Fail Output

Pin 1 : SENSE1 ⇔ supervising input 1
Pin 2 : SENSE2 ⇔ supervising input 2
Pin 3 : SENSE3 ⇔ supervising input 3 ⇒ (TPS3307 only)
Pin 3 : PFI ⇔ supervising PFI input ⇒ (TPS3306 only)
Pin 5 : $\overline{\text{RESET}}$ ⇔ reset output – active low
Pin 6 : RESET ⇔ reset output – active high (TPS3305 and TPS3307 only)
Pin 6 : $\overline{\text{PFO}}$ ⇔ power-fail output – active low (TPS3306 only)

3.1 Functional Description

The main function of a supply voltage supervisor (SVS) is to control a supply voltage. If this voltage decreases below the negative-going voltage V_{IT-}, the device has to assert a reset. The reset returns to the inactive state about 200 ms (100 ms for the TPS3306) after the voltage increases again to the positive-going voltage V_{IT+}. This time delay, t_d, is necessary to ensure that the processor-based system is able to complete the initialization phase during the reset cycle.

The power fail input (PFI) can be used for different purposes. Its hysteresis function is as previously described. The difference is that the power-fail output ($\overline{\text{PFO}}$) returns from its inactive state immediately after the voltage increases again to the positive-going value V_{IT+}.

The difference between the negative and the positive-going threshold voltage is called hysteresis, V_{hys}.

$$V_{IT+} = V_{IT-} + V_{hys} \quad (1)$$

The hysteresis avoids toggling the RESET outputs if the voltage is noisy.

Figure 9 shows the relationships between V_{IT+}, V_{IT-}, and V_{hys}.

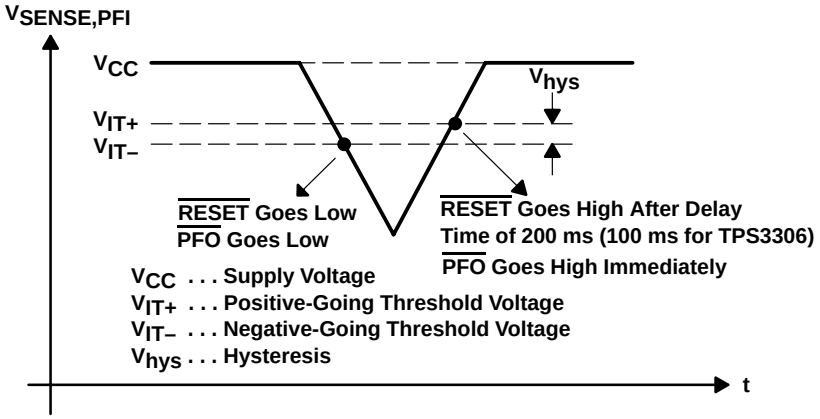


Figure 9. V_{IT+}, V_{IT-}, and V_{hys} Timing Relationships

Table 4 lists the minimum, typical, and maximum values for V_{IT-} and the typical values for V_{hys} with different supply voltages over the whole temperature range from –40°C to 85°C and over the recommended supply voltage range.

Table 4. Specified Values of V_{IT-} and Hysteresis V_{hys}

SUPPLY VOLTAGE	V_{IT-} – MIN	V_{IT-} – TYP	V_{IT-} – MAX	V_{hys} – TYP
5 V	4.46 V	4.55 V	4.64 V	40 mV
3.3 V	2.86 V	2.93 V	3 V	30 mV
2.5 V	2.20 V	2.25 V	2.3 V	20 mV
2 V	1.81 V	1.85 V	1.89 V	20 mV
1.8 V	1.65 V	1.68 V	1.71 V	15 mV
1.5 V	1.37 V	1.4 V	1.43 V	15 mV
Adjustable (PFI)	1.22 V	1.25 V	1.28 V	10 mV

3.2 Measurement of a Voltage Drop at SENSE2

The circuit shown in Figure 10 was used to demonstrate the typical working of an SVS during a drop in voltage.

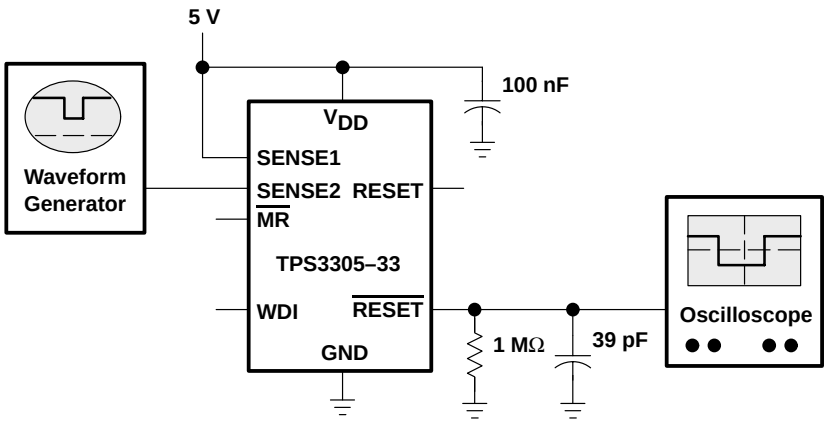


Figure 10. Circuit for Measuring the SVS Reaction to a Voltage Drop

The V_{DD} and SENSE1 terminals are connected to a stable 5-V power supply. $\overline{MR}$ and WDI are unconnected because they do not influence the working of the SVS. The SENSE2 input is connected to the waveform generator, which generates the voltage drop from 3.3 V to 2 V. The negative-going voltage of SENSE2 is typically 2.93 V. An oscilloscope measures the $\overline{RESET}$ output.

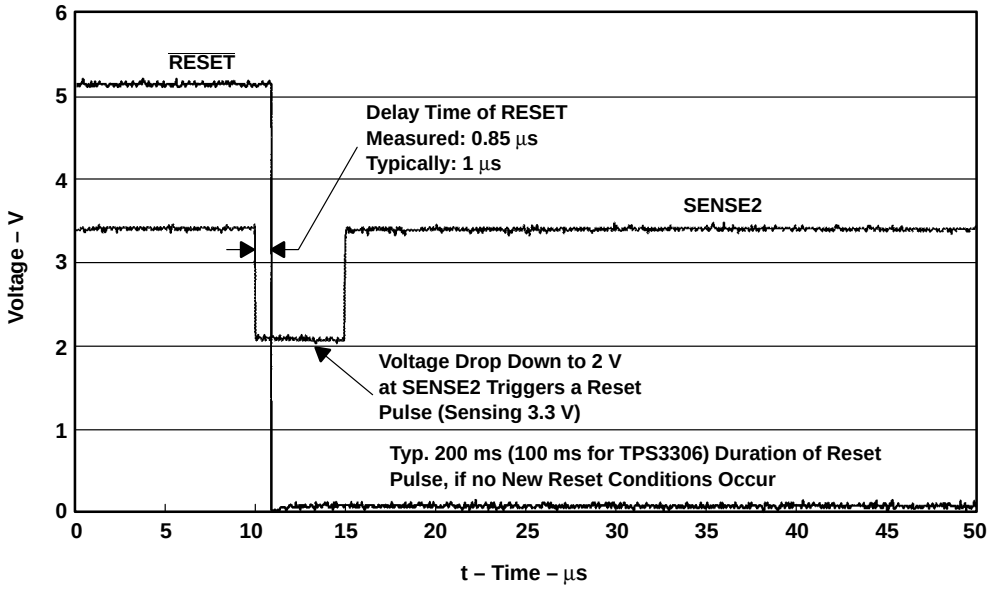


Figure 11. Measurement of the Voltage Drop at SENSE2 Input

This measurement is transferable to all SENSE inputs with all possible voltage values and their specified values in the data sheet.

3.3 The SENSE3 Input (TPS3307-xx Only), or PFI Input (TPS3306-xx Only)

The SENSE3 and PFI inputs have a threshold voltage of 1.25 V. If the supervised voltage falls below 1.25 V:

- A reset will be asserted in the case of the TPS3307–xx device.
- The $\overline{PFO}$ output changes its logic level from open-drain state to active low in the case of the TPS3306–xx device.

If the voltage increases above 1.265 V (15 mV hysteresis included):

- The reset goes to the inactive state after a typical delay time in the case of the TPS3307–xx device.
- The $\overline{PFO}$ output changes its logic level from active low to open-drain state in the case of the TPS3306–xx device.

The most important difference between SENSE3 input (or PFI input in the case of the TPS3306–xx) and the other SENSE inputs is that it can be customized easily. Every voltage above 1.25 V can be supervised or monitored with two external resistors. Equation 2 can be used to calculate the trip-point voltage.

$$V_{trip} = \frac{R1 + R2}{R2} \times 1.25\ V \qquad (2)$$

Figure 12 shows that the trip point is the voltage at which the SENSE3 (or PFI input in the case of the TPS3306–xx) has a value of 1.25 V.

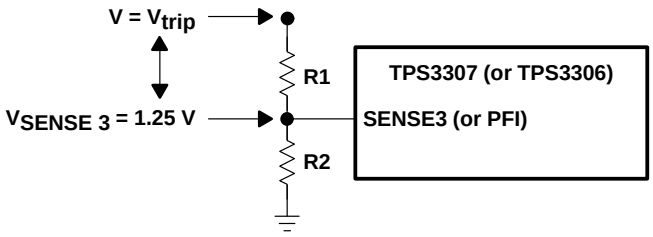


Figure 12. Trip-Point Voltage

For resistor selection, two points are important to consider:

- Resistors with a small tolerance should be used (e.g., <1%).
- The sum of both resistors should be about 1 MΩ. This ensures low current consumption.

Table 5 lists resistor pairs and the corresponding trip-point voltages.

Table 5. Look-Up Table for Trip Points Using E24 Resistors

R1/kΩ	R2/kΩ	V_{trip}/V	R1/kΩ	R2/kΩ	V_{trip}/V	R1/kΩ	R2/kΩ	V_{trip}/V
100	910	1.4	620	360	3.4	820	150	8.1
180	820	1.5	680	360	3.6	750	130	8.5
330	750	1.8	620	300	3.8	910	150	8.8
360	750	1.9	680	300	4.1	820	130	9.1
390	680	2.0	680	270	4.4	820	120	9.8
470	680	2.1	750	270	4.7	910	130	10.0
470	620	2.2	820	270	5.0	820	110	10.6
470	560	2.3	750	240	5.2	910	120	10.7
510	560	2.4	750	220	5.5	820	100	11.5
560	560	2.5	750	200	5.9	910	110	11.6
560	510	2.6	750	180	6.5	1000	120	11.7
560	470	2.7	820	180	6.9	820	91	12.5
620	470	2.9	750	150	7.5	910	100	12.6
680	470	3.1	910	180	7.6	1000	100	13.8
560	360	3.2	820	160	7.7	1100	100	15.0

3.4 Breakdown Voltage Over Pulse Width

The data sheet specifies that a 6-µs voltage drop of at least 200 mV below V_{IT-} must trigger a reset pulse. But what happens with a deeper drop of shorter duration? The circuit shown in Figure 13 was used to answer this question.

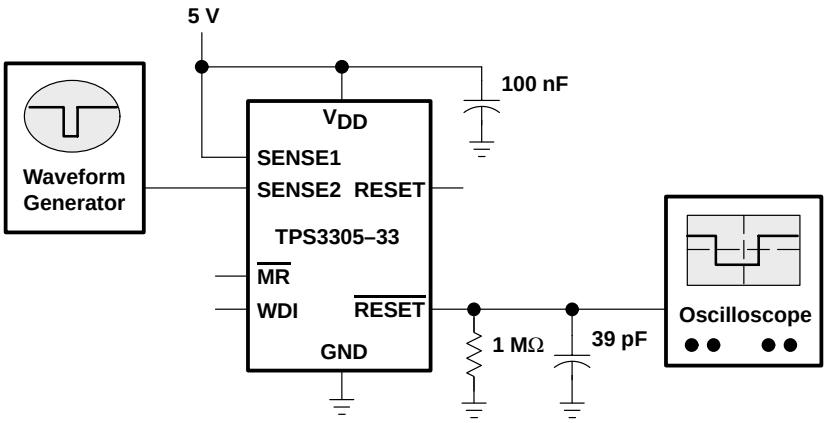


Figure 13. Circuit for Measuring Breakdown Voltage Over Pulse Width

A TPS3305-33 and a TPS3307–33 were used for the first set of measurements, with the SENSE1 input sensing 5 V with a typical V_{IT-} of 4.55 V and the SENSE2 input sensing 3.3 V with a V_{IT-} of 2.93 V. One result is the average of five measured values. If the voltage breaks down to 0 V, a pulse width of 200 ns is enough to trigger a reset pulse in both cases. Figure 14 shows the results of the measurements.

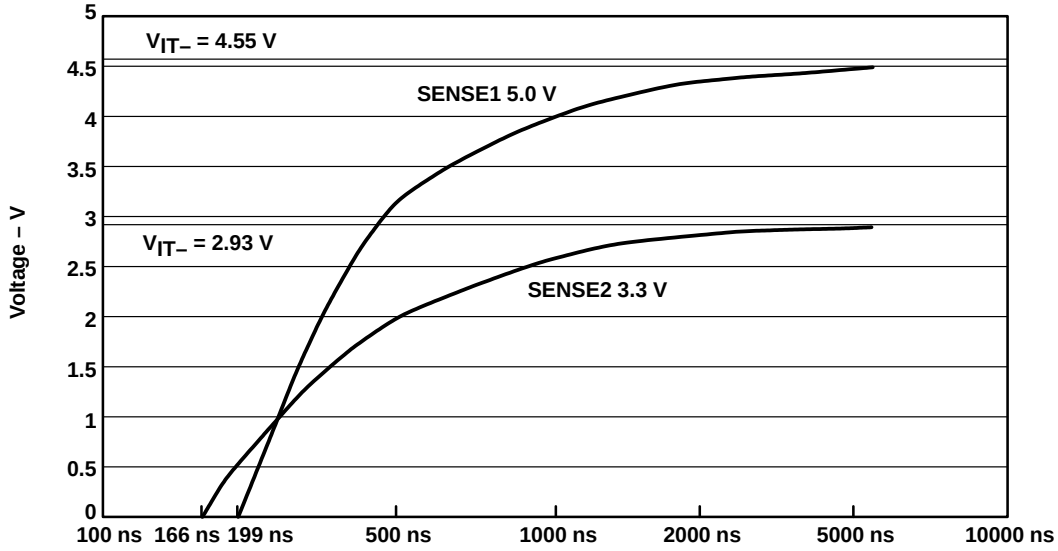


Figure 14. Breakdown Voltage Over Pulse Width (TPS3305-33, TPS3307–33)

A TPS330x-25 and a TPS3307–25 were used for the second set of measurements, with the SENSE1 input sensing 3.3 V with a typical V_{IT-} of 2.93 V, and the SENSE2 input sensing 2.5 V with a V_{IT-} of 2.25 V. Figure 15 shows the results of the measurements.

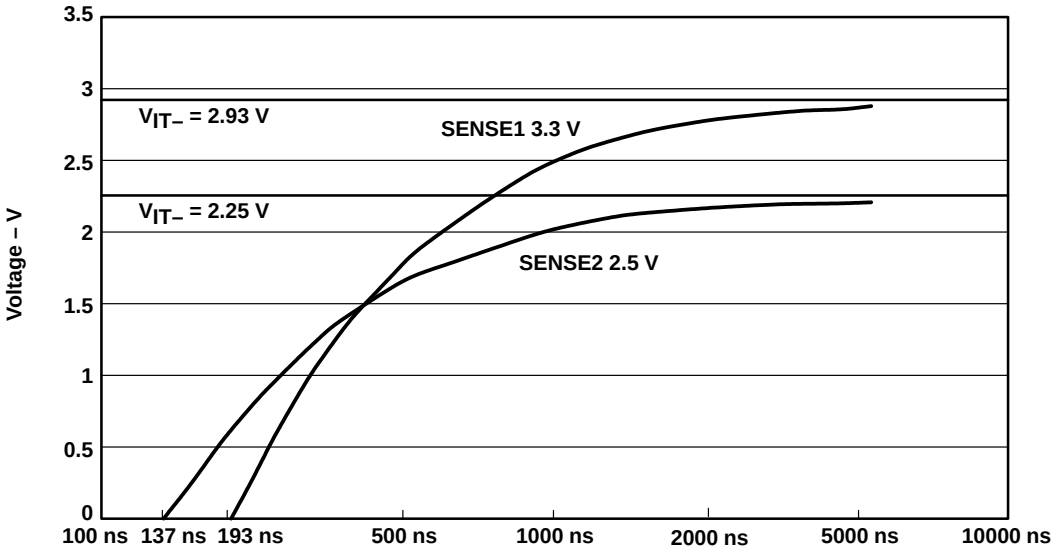


Figure 15. Breakdown Voltage Over Pulse Width (TPS3305-25, TPS3307–25)

3.5 Making the SENSE Input Less Sensitive

The SENSE input detects short-duration voltage drops. If the voltage falls 200 mV below $V_{IT–}$, a pulse duration of 6 μs is enough to assert the reset. Usually, an SVS is used in DSP or microcontroller-based systems to minimize the danger of losing data in registers or volatile memories. But there are also systems that are not influenced by such short-duration drops in V_{DD} voltage. For these systems, the sensitivity of the SENSE inputs should be reduced. Figure 16 shows one solution to this problem: add a low-pass filter in front of the SENSE input.

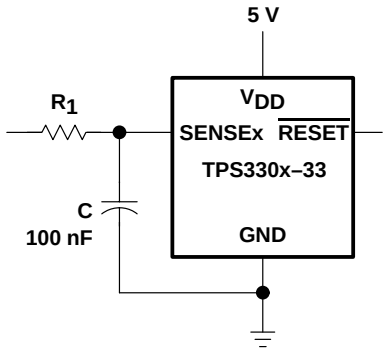


Figure 16. TPS330x With a Low-Pass Filter at SENSE Input

Care must be taken to ensure that the additional resistor does not change the threshold voltage. The threshold voltage is determined by the internal resistor divider shown in the block diagram, Figures 4 to 6. A 10-kΩ resistor, for example, decreases the threshold voltage by 40 mV, a 1-kΩ resistor by 4 mV, and a 100-Ω resistor by 0.4 mV. Measurements were made using these three values for R1. In Figures 17 and 18, the y-axis shows breakdown voltage; the x-axis shows the duration of the voltage drop.

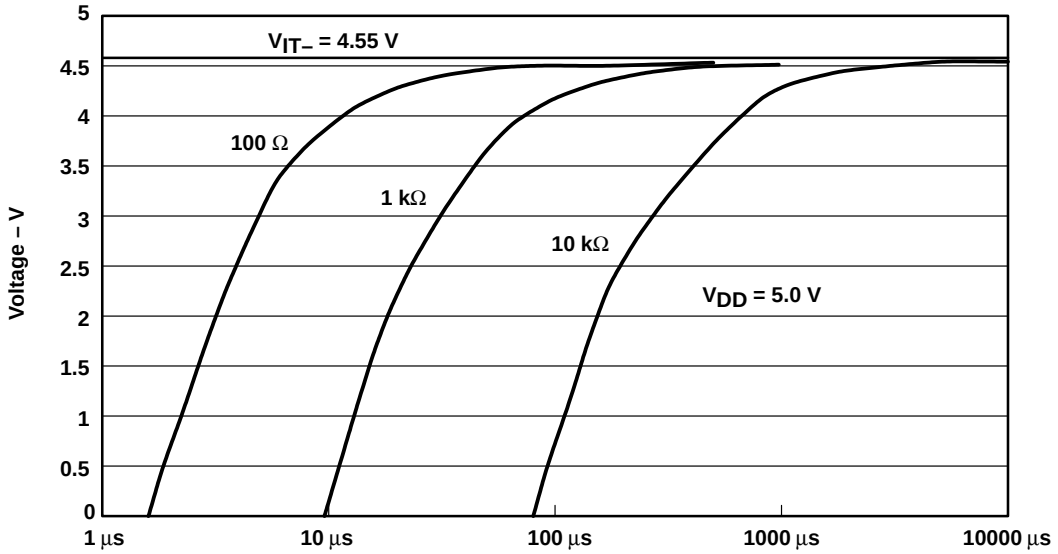


Figure 17. Breakdown Voltage Over Pulse Width With a Low-Pass Filter at SENSE1

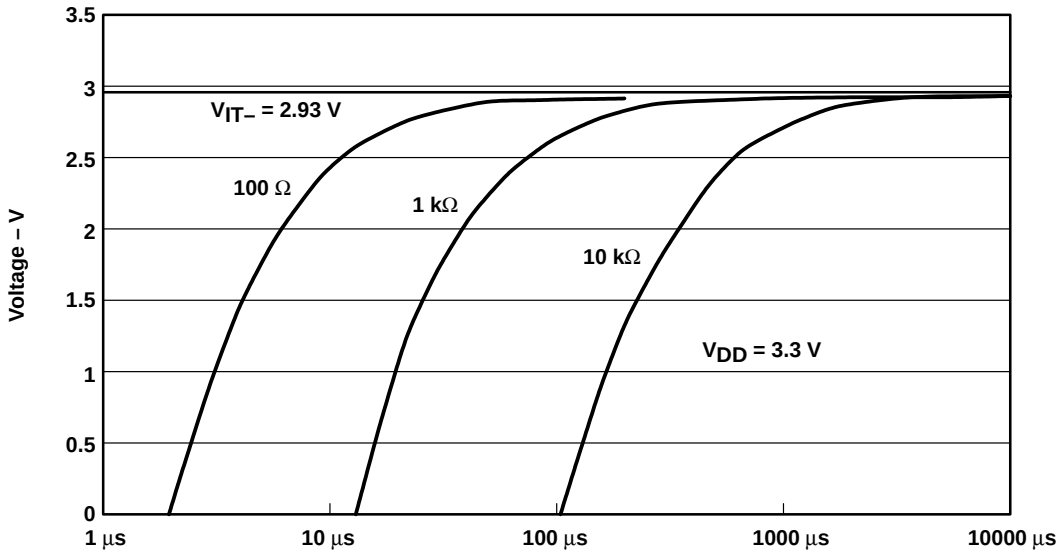


Figure 18. Breakdown Voltage Over Pulse Width With a Low-Pass Filter at SENSE2

4 Manual Reset

Pin 5 : $\overline{\text{RESET}}$ ⇔ reset output – active low
Pin 6 : RESET ⇔ reset output – active high
Pin 7 : $\overline{\text{MR}}$ ⇔ manual reset

4.1 Functional Description

The manual reset is an input for triggering a reset by an external component. For example, a pushbutton switch, a microcontroller, or a DSP port can provide the manual reset. The minimum condition for a reset is a low pulse of 0.3 x V_{DD} for at least 100 ns at $\overline{\text{MR}}$. These values are specified in the data sheet. The reset will be asserted for the time of low signal at $\overline{\text{MR}}$ plus delay time.

4.2 A Measurement at the Manual Reset

Figure 19 illustrates a measurement of a 50-ms low pulse at manual reset and the resulting reset pulse at $\overline{\text{RESET}}$.

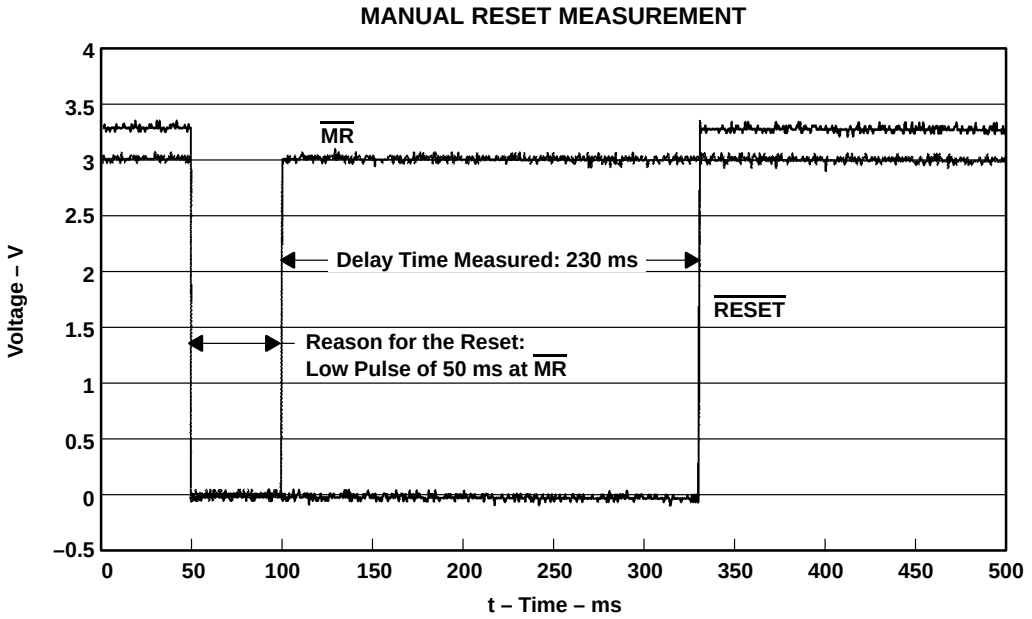


Figure 19. Measurement of a Reset Pulse Triggered by Manual Reset

4.3 Saving Current When Using Manual Reset

Saving current when using the manual reset function is a system design consideration. Figure 20 shows the internal structure of the $\overline{\text{MR}}$ circuit.

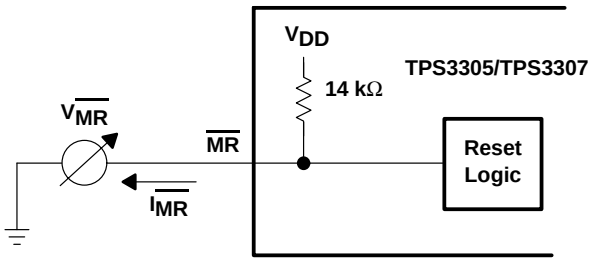


Figure 20. Internal Structure of the $\overline{\text{MR}}$ Circuit

To avoid generating a reset, the manual reset input has to be driven with a voltage between $0.7 \times V_{DD}$ and V_{DD} as specified in the data sheet. But a steady current flow occurs if the voltage at $\overline{\text{MR}}$ differs from V_{DD}. Equation 3 calculates this current.

$$I_{\overline{MR}} = \frac{V_{DD} - V_{\overline{MR}}}{14\ k\Omega} \tag{3}$$

The maximum current occurs if $\overline{\text{MR}}$ is pulled down to ground; therefore, the time should be kept as short as possible.

5 Watchdog (TPS3305 and TPS3306)

Pin 3 : WDI ⇔ watchdog input (TPS3305)

Pin 7 : WDI ⇔ watchdog input (TPS3306)

Pin 5 : $\overline{\text{RESET}}$ ⇔ reset output – active low – push-pull stage (TPS3305)

Pin 5 : $\overline{\text{RESET}}$ ⇔ reset output – active low – open-drain output (TPS3306)

Pin 6 : RESET ⇔ reset output – active high – push-pull stage (TPS3305 and TPS3306)

5.1 Functional Description

In a microprocessor or DSP-based system, it is important to supervise the supply voltage, as well as to ensure correct program execution. The task of a watchdog is to ensure that the program does not stall in an infinite loop. The system must toggle the watchdog input within 1.1 s to avoid a reset pulse. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. The watchdog resets itself if the input is unconnected.

5.2 Measurements

The following measurements demonstrate the watchdog function and behavior. They were taken with the TPS3305–25, but are also valid for the other devices. The difference is in the TPS3306 output configuration, which needs to be tied to V_{DD} with a pullup resistor.

5.2.1 Measurement Circuit

Figure 21 shows the circuit used in the watchdog measurements.

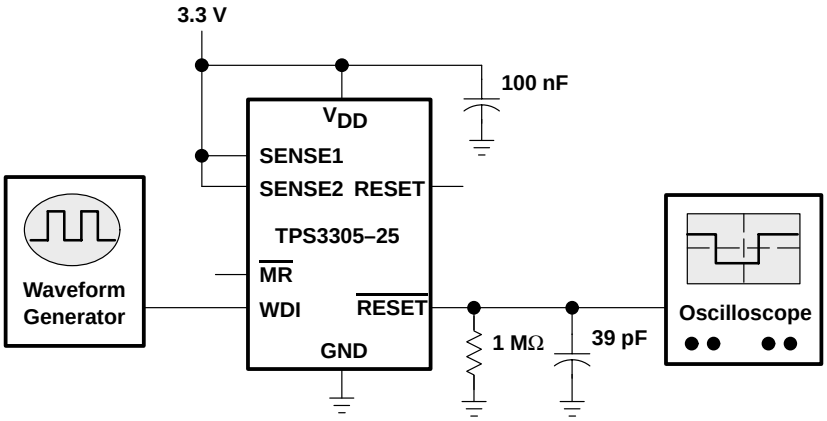


Figure 21. Measurement Circuit for Testing the Watchdog

5.2.2 Time-Out Occurs

As shown in Figure 22, the waveform generator delivers a transition every 2.5 s. This time is not in the time-out range so that the reset output becomes active periodically.

Signal characteristics:

- Signal waveform: rectangular
- High-level voltage: 2.8 V
- Low-level voltage: 0 V
- Frequency: 0.2 Hz
- Duty cycle: 50%

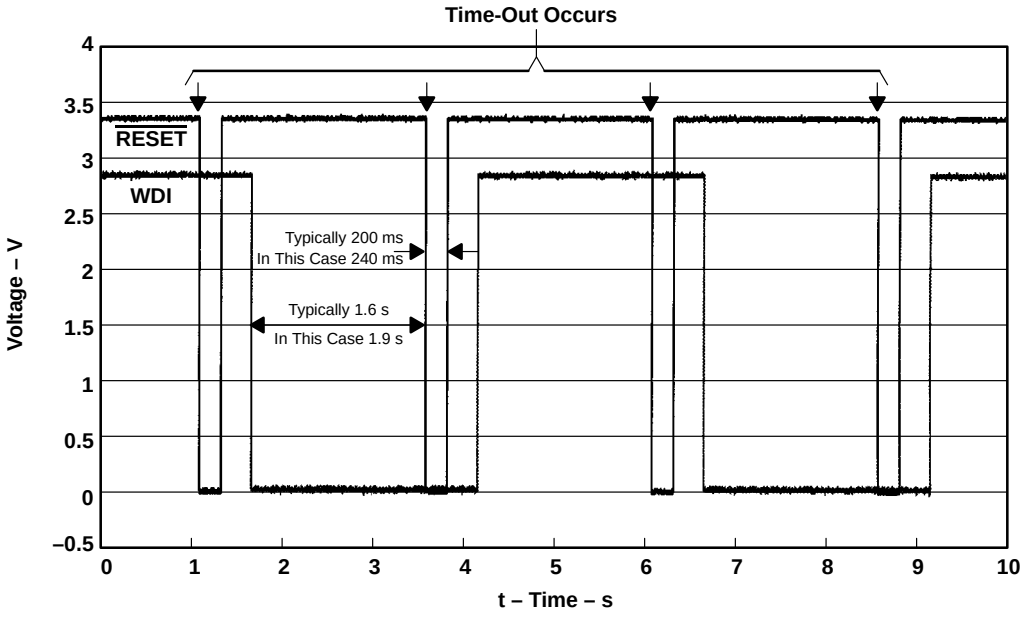


Figure 22. Watchdog Measurement 1 – Time-Out

5.2.3 Time-Out Does Not Occur

As shown in Figure 23, the waveform generator delivers a transition every second. This is less than the minimum time-out specified in the data sheet, so the internal watchdog timer is reset in time and no reset pulse occurs.

Signal characteristics:

- Signal waveform: rectangular
- High-level voltage: 2.8 V
- Low-level voltage: 0 V
- Frequency: 0.5 Hz
- Duty cycle: 50%

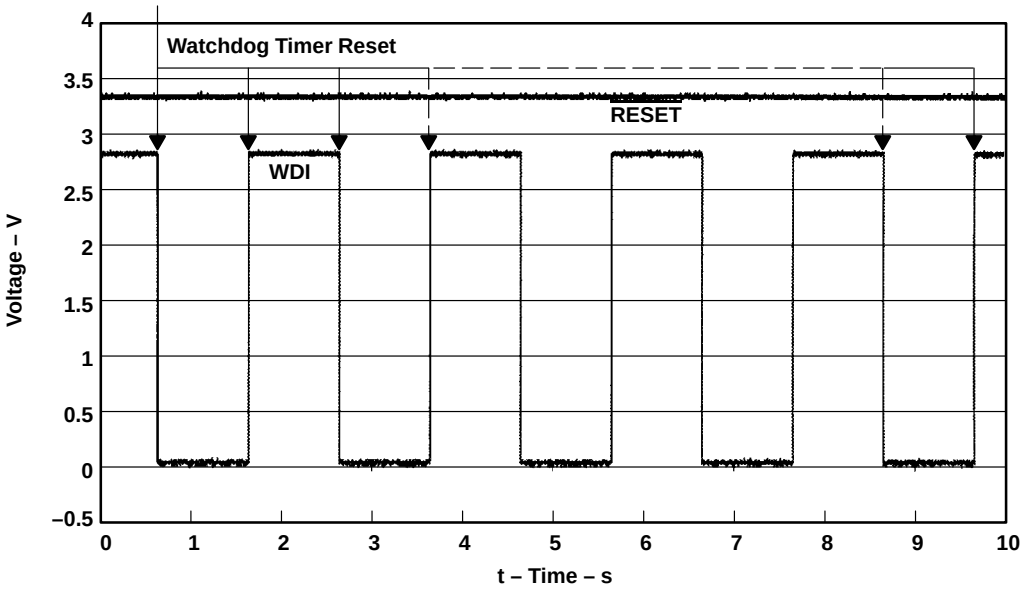


Figure 23. Watchdog Measurement 2 – No Time-Out

5.2.4 Summary of Watchdog Measurements

Figure 24 gives a summary of the time-out parameters. The measurement values can be compared with the values specified in the data sheet.

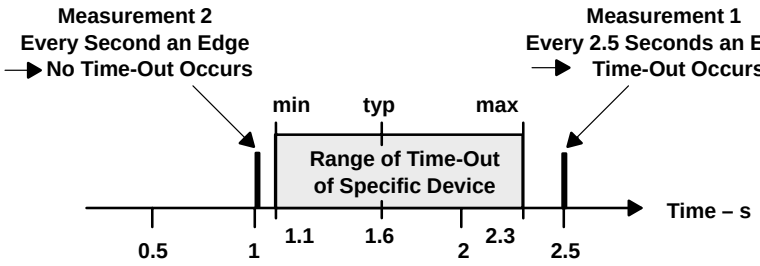


Figure 24. Overview of Watchdog Time-Out Condition

5.3 Saving Current While Using the Watchdog

A positive or a negative transition can be used to reset the watchdog timer. If saving energy is an important system concern, the high time of the external signal should be kept low as long as possible. If there is no concern about saving current, a rectangular signal at WDI with a 0.5-Hz frequency (⇒ an edge every second) is sufficient to reinitialize the internal watchdog and to avoid a time-out.

The internal driver drives a 0 during seven-eighths of the time-out period, then it changes to a logic 1. If WDI is unconnected externally, the change to 1 resets the internal watchdog timer and drives it to logic 0 again.

If WDI is driven by an external voltage as shown in Figure 25, the internal signal is overwritten, and the external voltage determines the behavior of the watchdog. If the external voltage source delivers 0 V, there is almost no current flow; if it delivers 3.3 V, a current of about 3.3 V/40 kΩ ≈ 80 μA flows in the device. So a 0 is the recommended external driving signal with a periodically-recurring small logic pulse.

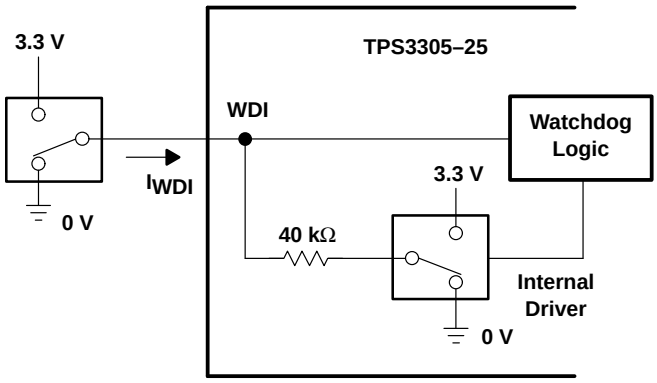


Figure 25. Internal Structure of the Watchdog Autoreset Driver

6 Applications

This section describes typical TPS330x applications.

6.1 TPS3305 Supervising the Dual-Voltage DSP TMS320VC5402

The TPS330x is well suited for supervising dual voltage DSPs such as the members of the ’C5000 and ’C6000 families from Texas Instruments.

The TPS330x-18 has a SENSE1 input for sensing 3.3 V and a SENSE2 input for sensing 1.8 V. The TPS330x-25 is the proper device if the core voltage, CV_{DD}, is 2.5 V.

In the application example shown in Figure 26, the TPS3305-18 supervises a TMS320VC5402 supplied by a TPS77633 LDO capable of delivering 500 mA in a PowerPAD™ package as the 3.3 V I/O supply. A TPS76918 is recommended to provide1.8 V to the core. Both voltages are generated from a 5-V source.

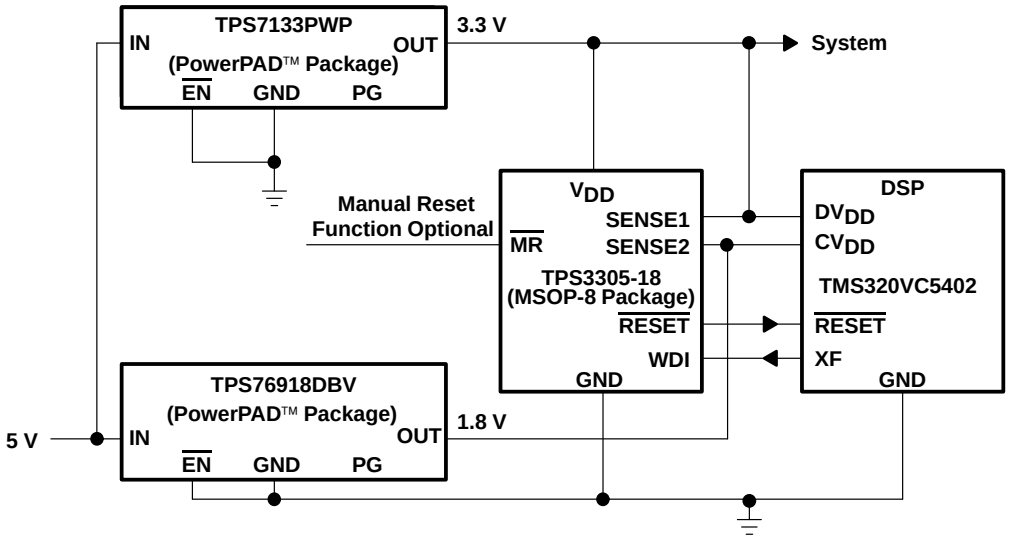
During power up, the $\overline{\text{RESET}}$ output of the SVS keeps a low level at the $\overline{\text{RESET}}$ input of the DSP until the supply voltages and the internal oscillator are stable. This prevents the DSP from executing invalid code before the required voltages are available.

The watchdog of the SVS ensures that the DSP does not stalled in an infinite loop. The ’C5402 has to trigger the SVS at least every 1.1 s minimum t_{tout} (0.5 s for the TPS3306) with the external flag (XF) to avoid a reset.

LDOs like the TPS776xx series also provide a power-good (PG) signal. A comparator monitors the LDO output voltage internally. When it drops between 92% and 98% of its nominal value, the PG open-drain output stage turns on taking the signal to low. This function is not implemented in the application example.

A TPS76918 is used to generate the 1.8 V required from the DSP core.

The $\overline{\text{MR}}$ of the SVS offers the capability to be connected to an external reset source such as a pushbutton or another logic device.



The necessary decoupling capacitors are not shown to increase the clearness of the figure.

Figure 26. TPS3305-33 Supervising a Dual-Voltage DSP

6.2 Supervising Three Voltages

Some present-day systems may need more than one supply voltage to fulfill the requirements of newer ICs working with a reduced supply voltage to save energy.

Before the introduction of the TPS3307-xx, two supply voltage supervisors were needed to supervise three voltages simultaneously. The TPS3307-xx solves this problem by offering supervision for two fixed voltages and a third one that can be customized with two external resistors.

The TPS3307-33 shown in Figure 26, for example, supervises 5 V at SENSE1 and 3.3 V at SENSE2. The SENSE3 input is available if there is a need to supervise 2.5 V. The negative-going threshold V_{IT-} voltage is adjusted to:

$$V_{IT-} = \frac{R1 + R2}{R2} \times 1.25\ V = \frac{470\ k\Omega + 620\ k\Omega}{620\ k\Omega} \times 1.25\ V = 2.20\ V \quad (4)$$

which is well suited for the 2.5-V supply voltage. This is illustrated in Figure 27. See Section 3.3 for more information about the SENSE3 input.

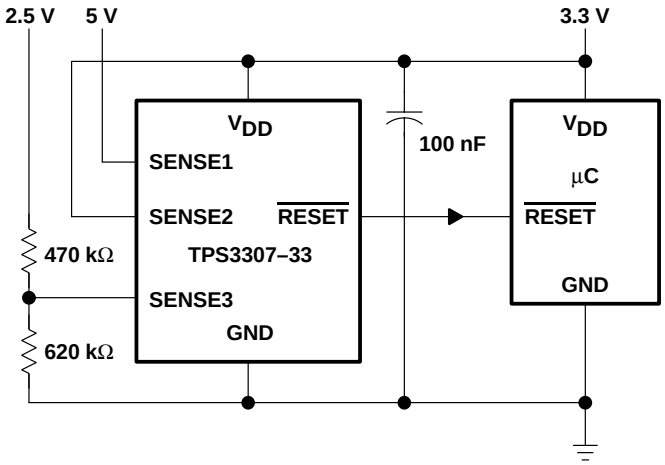


Figure 27. Supervising 2.5-V, 3.3-V, and 5-V Supplies With One Device

6.3 Supervising a Battery-Powered Dual-Voltage DSP System With TPS3306

In the application example shown in Figure 26, a battery is used to source a system. A buck-converter topology is implemented to power the DSP with the proper voltages. The heart of the power monitoring is the TPS3306–18 which supervises the two supply voltages provided. Extended overall system reliability is gained by monitoring the battery voltage via the power-fail input option.

The buck converter TPS5602 EVM–121 is an evaluation module available from TI that provides two fixed-output voltages of 3.3 V and 1.8 V out of a single source. Currents of up to 4 A at 1.8 V and 3 A at 3.3 V can be achieved with this module. Both voltages get monitored by the TPS3306–18.

The power-fail input is connected via a voltage divider to V_{IN} of the buck converter TPS5602 EVM–121 to monitor the actual voltage provided by the battery. Different application topologies and different battery types make it impossible to offer a general suggestion of how to calculate the right trip point of a particular application.

A general example of a NiCd battery constellation of seven single cells was chosen to describe a possible monitor function of the power-fail input. Fully charged NiCd cells provide a voltage level of approximately 1.2 V each during 80% of the discharge period of operation. Their voltage drops very quickly after this discharge period. To prevent the battery from discharging too deeply or to loose control over the system because of power failure, the system gets informed via the power-fail comparator implemented.

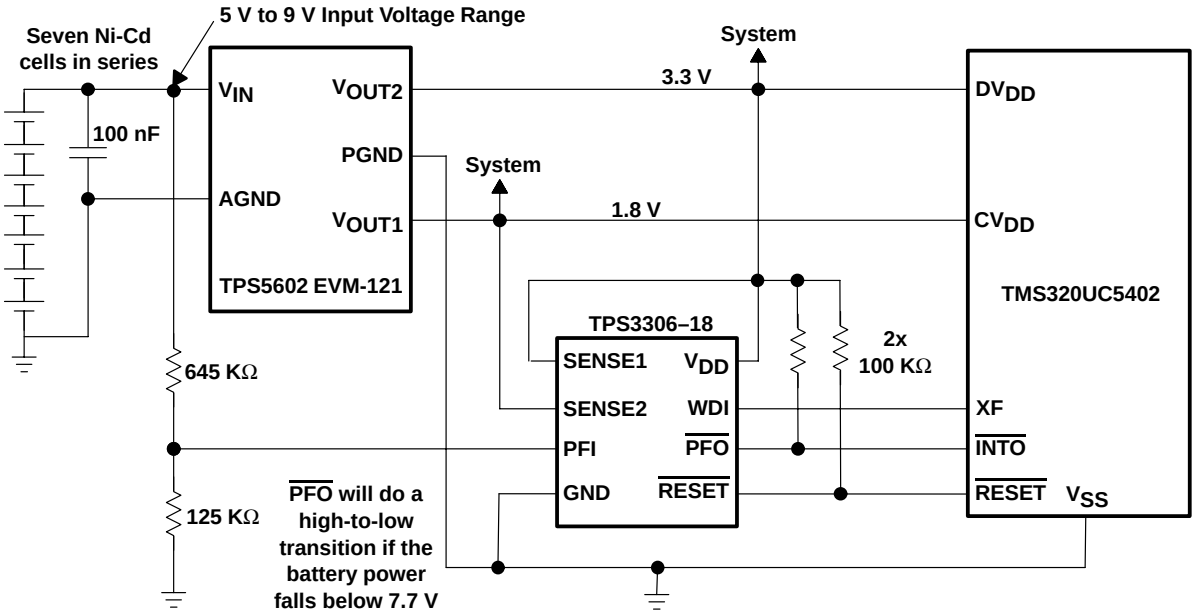
A value of 1.1 V for each of the seven cells was chosen to keep this example simple.

To calculate an individual trip point, the following equation should be used.

$$V_{IT-} = \frac{R1 + R2}{R2} \times 1.25\ V = \frac{645\ k\Omega + 125\ k\Omega}{125\ k\Omega} \times 1.25\ V = 7.7\ V \qquad (5)$$

If the trip point is calculated and implemented as a voltage divider, the power fail input compares the value provided with the 1.25 V reference voltage. If the battery voltage decreases to 7.7 V or lower, the $\overline{PFO}$ will do a high-to-low transition and the DSP will detect an interrupt via $\overline{INT0}$ pin. The recognition can be handled by software. There can be various possibilities here, such as:

- Informing the operator of the critical battery value
- Finishing all operations and shutting down the system
- Informing the operator and switching to another source, if available



The necessary decoupling capacitors are not shown to increase the clearness of the figure.

Figure 28. Supervising Supply Voltages of 3.3 and 1.8 V and Monitoring the Battery

The TPS5602 is a dual-channel synchronous buck switch-mode power-supply controller featuring very fast feedback control and minimal component count. Its use of the hysteretic control method makes it ideal in high-transient current applications, such as multiple C6000 and multiple C5000 DSPs. The TPS5602 is designed specifically for DSP applications that require high efficiency. The wide-input voltage and adjustable-output voltage make the TPS5602 suitable for many applications. An EVM is available.

The TPS5602 operation is slightly dependent on the discharge current.

7 Layout Considerations

This section describes layout considerations when designing with the TPS330x devices.

7.1 Five Layout Principles

Figure 29 shows a typical board layout. The following points should be considered in the layout to ensure proper operation:

- Connections to external components should be kept as short as possible.

- If the circuit includes a device with a high current consumption, the value of the common-ground resistor of both devices should be kept low. This can be achieved by keeping the ground line separated as far as possible (star-shaped connection).
- The SVS should be located in an interference-free environment.
- Use a blocking capacitor of 100 nF between supply voltage and ground to ensure proper operation.
- If WDI is not driven by an external signal, ensure that only a small pad, rather than long traces, is connected to this pin in the layout. Otherwise external signals may be coupled in and may affect the performance and proper operation of the WDI's internal self-reset logic.

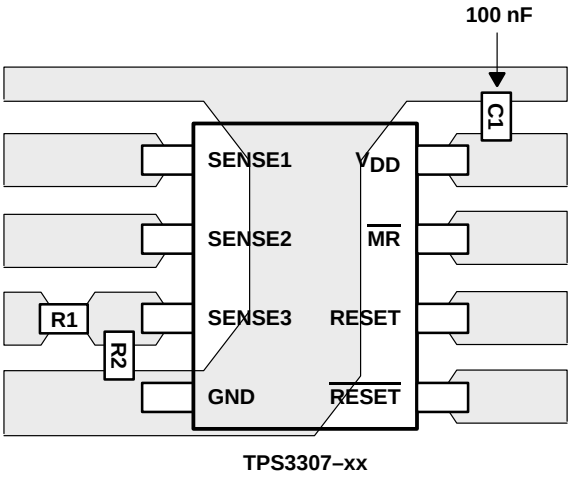


Figure 29. Suggested Layout for a Circuit With the TPS3307-xx

7.2 Capacitor Between V_{DD} and GND

Four measurements were made to demonstrate the influence of the blocking capacitor. The first two measurements, illustrated in Figures 30 and 31, show the $\overline{\text{RESET}}$ high-to-low transition output and the V_{DD} supply voltage during a reset condition caused by a voltage drop at the SENSE2 input. The reset outputs switch due to the totem-pole outputs, and a lateral current flows for a short time. The figures also show the measurement of V_{DD}. No oscillations can be observed. The recommended 100 nF capacitor is needed between V_{DD} and ground to prevent oscillations.

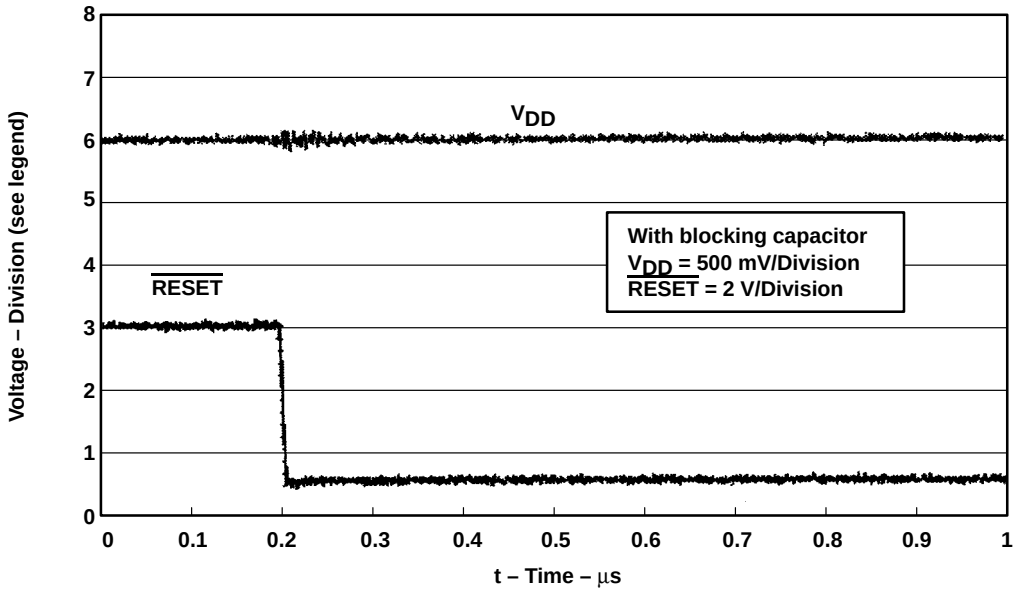


Figure 30. V_{DD} – Line of TPS3305-33 With a Capacitor

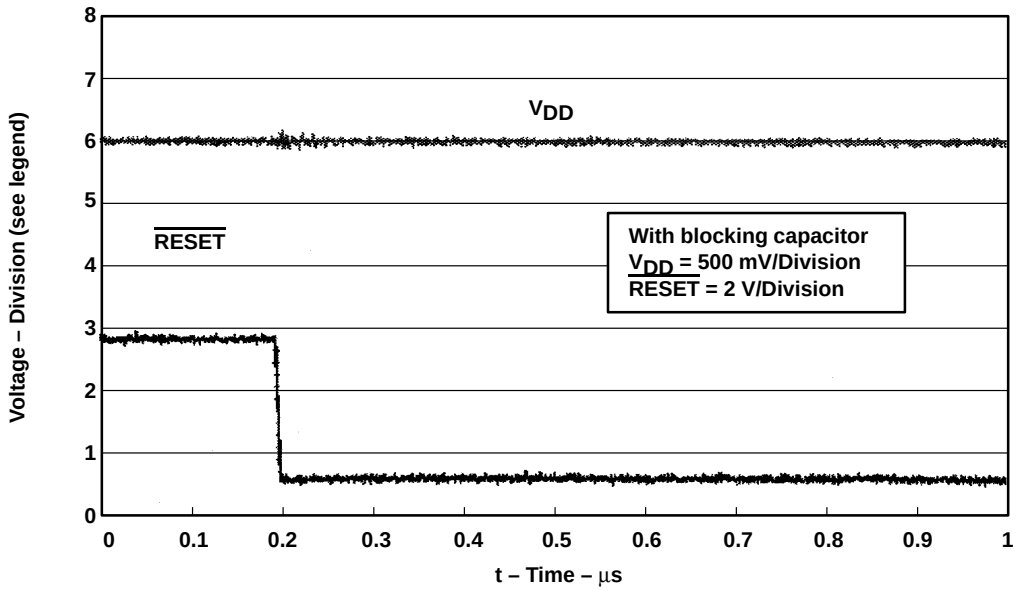


Figure 31. V_{DD} – Line of TPS3306-33 With a Capacitor and 100-kΩ Pullup Resistor at the $\overline{\text{RESET}}$ Output

The capacitor between V_{DD} and ground was replaced for the third and fourth measurements shown in Figures 32 and 33. Oscillations with amplitudes higher than 0.5-V for over 400 ns can be observed.

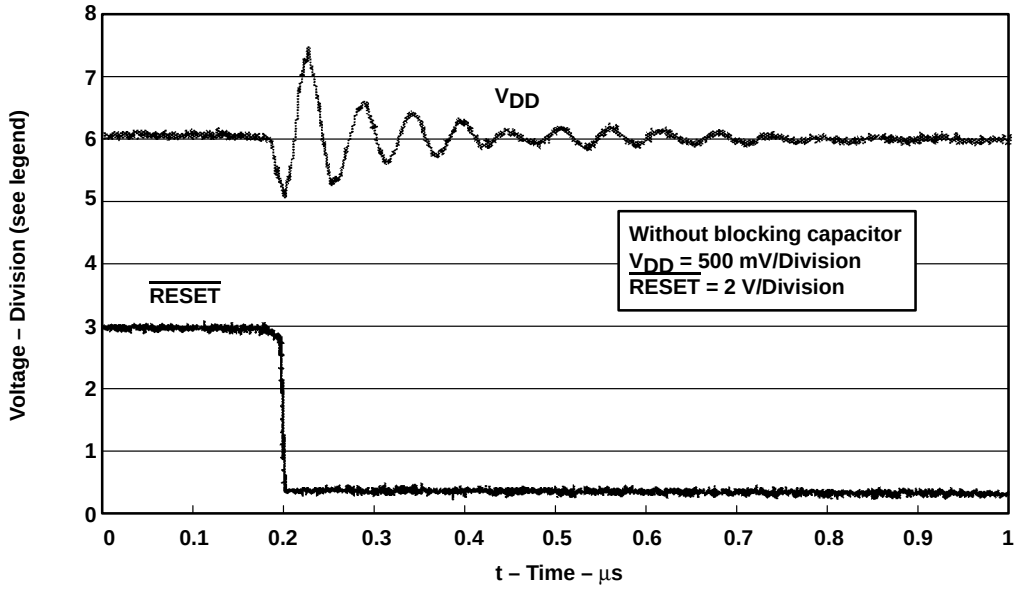


Figure 32. V_{DD} – Line of TPS3305–33 Without a Capacitor

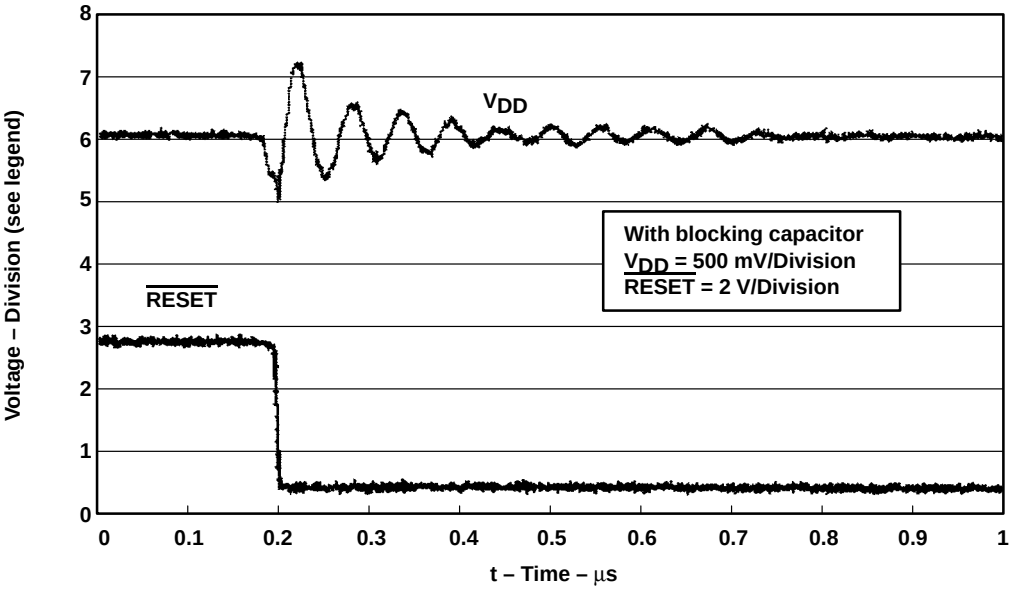


Figure 33. V_{DD} – Line of TPS3306–33 Without a Capacitor and 100-kΩ Pullup Resistor at the $\overline{\text{RESET}}$ Output

The 100-nF blocking capacitor between V_{DD} and ground is absolutely necessary. If the capacitor is omitted, malfunction is probable. A possibility is that the reset output starts to oscillate due of the internal-reference voltage instantly becoming unstable.

To understand the high current that flows through the device for a short time, the output– and the driver stage must be considered. They are implemented as push-pull or totem pole stages. The explanation follows.

7.3 An Optimized Output Stage

The problem with a conventional totem pole output stage, like that shown in Figure 34, is that if the input voltage is $V_{DD}/2$, both transistors conduct momentarily. This causes a relatively-high current peak from V_{DD} to ground for a short time.

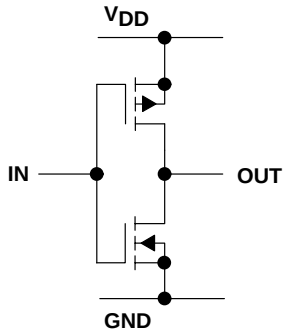


Figure 34. Conventional Totem Pole Output Stage

To achieve better behavior, the transistors should switch with a little delay time. In this way, the output stages of TPS3305 and TPS3307 achieve a factor of 3 reduction in the current peak. All the internal driver stages are also totem-pole; consequently, even the open-drain version is drawing more current during the high-to-low transition phase, and vice versa.

8 Summary

The TPS330x family offers the possibility of supervising up to three supply voltages. Therefore, they fit very well into multivoltage systems that use dual-voltage DSPs.

Each member of the TPS330x-family has two SENSE inputs for supervising voltages, a manual reset input for triggering the reset by an external source, and low-active resets. The TPS3305 and TPS3307 also have a high-active reset.

The TPS3305 and TPS3306 have an integrated watchdog function instead of a third SENSE input like the TPS3307. The additional SENSE input on the TPS3307 can control an adjustable voltage greater than 1.25 V. It can be customized using two external resistors. The TPS3306 is capable of monitoring and comparing the external voltage with a 1.25-V reference. If PFI drops below 1.25 V, the power-fail output ($\overline{PFO}$) pin changes from high to active low. This comparator can be used for a variety of purposes.

The devices are available in SO and MSOP packages for the the most popular supply voltages. Due to the BiCMOS technology, the current consumption is only 40 μA maximum.

Using one of the new TPS330x supply-voltage supervisors adds significant system reliability to DSP or processor-based applications.

9 References

1. TPS3305-xx data sheet, literature number SLVS198
2. TPS3306-xx data sheet, literature number SLVS190
3. TPS3307-xx data sheet, literature number SLVS199
4. *Designer's Guide* and Data Book – InfoNavigator CD-ROM, SLYC005A
5. *The TPS370x Family Application Report*, literature number SLVA045
6. *TPS382x Microprocessor Supervisory Circuits with Watchdog Function*, literature number SLVA039
7. *TLC77XX Series of BiCMOS Supply Voltage Supervisors*, literature number SLVAE03
8. *Supply voltage Supervisor TL77xx Series*, literature number SLVAE04
9. Linear Design Seminar, literature number SLYDE05
10. Internet : http://www.ti.com/sc/docs/products/msp/pwrmgmt/index.html
11. *Dual, Fast, High Efficiency Controller for DSP Power,* literature number SLVS217
12. Internet : http://www.ti.com/sc/docs/products/analog/tps5602.html

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