Application Report
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Using Dual Current Limited TPS2140/41/50/51 for USB and Portable Applications

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ABSTRACT

An issue in USB and other hot-swap environments is the unpredicted inrush current during plug-in. Depending on the load capacitance, the initial turn-on inrush current varies from miliamps to several amps. The high inrush current can drag the input supply voltage down to reset the upstream system. USB 1.0 and 2.0 specifications limit the inrush current by limiting the maximum input capacitance on the USB power source to 10-µF. The Texas Instruments TPS2140/41/50/51 family of switches are designed to help meet this inrush current requirement and allow the designer to optionally have a larger load capacitor.

Contents

List of Figures

Introduction

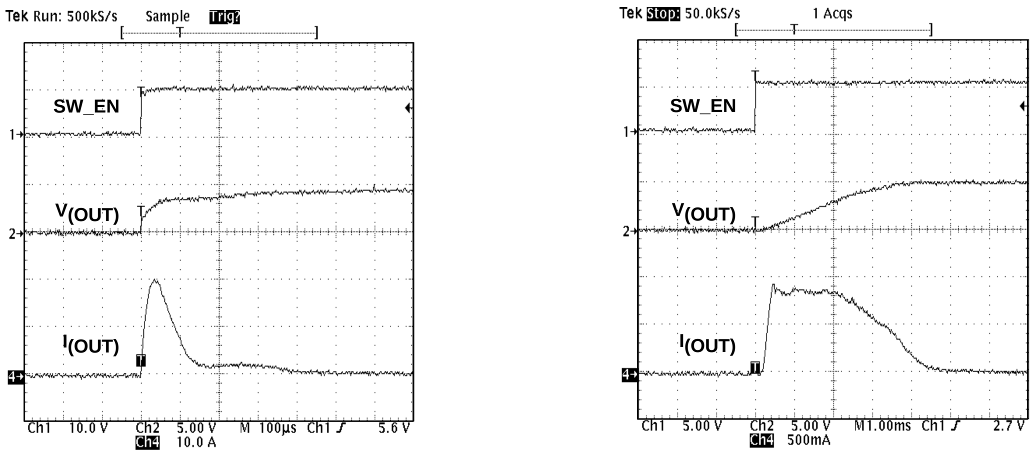
The TPS2140/41/50/51 integrates a dual-current-limiting power switch and an adjustable low dropout regulator (LDO). Depending on the input voltage range and the polarity of the enabling signal, this family of devices provides four options to meet different USB and portable design requirements. With a 5-V power switch, the TPS2150 and TPS2151 are suitable for USB applications.

During the power up period, the switch in the TPS2140/41/50/51 precisely limits current at under 100mA. After the output of the switch is charged up to 93% of the input voltage, the current limit of the switch increase to allow delivery of at least 500 mA from its input supply to the output.

The device also integrates a 250-mA adjustable LDO that can regulate from 2.7–5.5 V down to 0.9–3.3 V for low-voltage portable functions. Power-good reporting and output discharge transistors for both the power switch and the LDO are integrated, which are very useful features in many applications.

Inrush Current With a Discrete or USB Power Switch

If a discrete MOSFET is used for switching the power from a supply to a capacitive load, the inrush current that charges the output capacitor can be very high, as shown in Figure 1(a). In this example, the inrush current peaks at about 20 A for about 100 µs and then falls down to approximately 2 A for about 200 µs before reaching the miliamp level. The major limiting factor for the current is the on-resistance of the MOSFET, which is typically very small in order to reduce voltage drop and power dissipation. With that much inrush current, the supply can be easily dragged down to an unacceptable level, thereby creating problems. The waveform in Figure 1(b) shows the result for a typical USB power switch, which has a current limit range of 600 mA to 1.5 Amps. Although the inrush current is better controlled, USB requires that the peripheral draw less than 100 mA during enumeration. A system requiring a larger load capacitor would not meet this requirement. The load capacitor takes as much current as the power switch can deliver. With the TPS2140/41/50/51 devices, a larger load capacitor would only charge with a maximum of 100 mA during enumeration.



(a) Using a MOSFET **(b) Using A Typical USB Power Switch**

Figure 1. Inrush Current During Power on With a 470-µF Capacitive Load

Powering Large Capacitive Load With TPS2150/51

To understand how the power switch of TPS2150 or TPS2151 works, different loads are used to evaluate the performance of the power switch. A test diagram with both capacitive and resistive loads is shown in Figure 2.

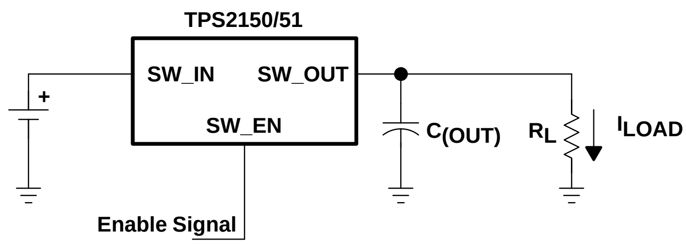
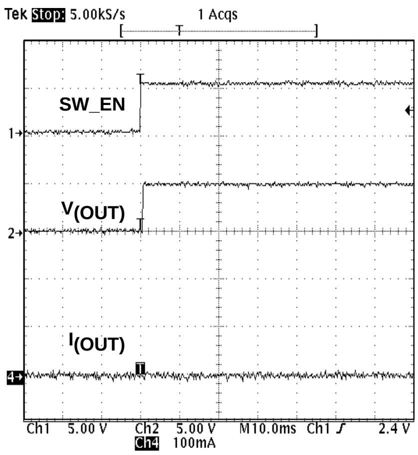
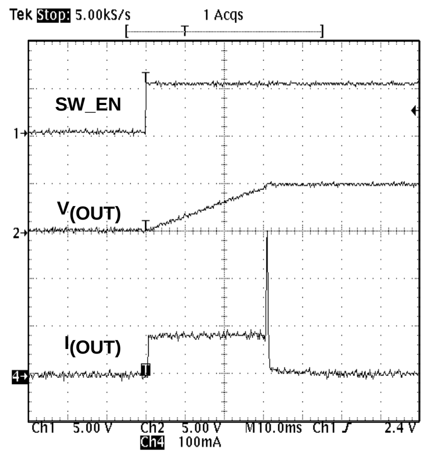


Figure 2. Simple Application Diagram for Power Switch

With only capacitive loads (C_O), the output voltage and the current going through the power switch are shown in Figure 3. The waveforms on the left show almost no inrush current for a 4.7-µF load while the waveforms on the right demonstrate that the inrush current is limited even with a very large load capacitor (470 µF). The inrush current to the capacitor is limited to about 75 mA. Once the capacitor charges up to 93% of the input, the higher current limit is activated. The activation of the higher current limit can be seen in Figure 3(b). A small magnitude current spike occurs when the higher current limit circuit is activated. This current spike only occurs for a very small amount of time, since the output voltage is very close to the input supply level before the low current limit is released.



(a) C_O = 4.7 µF



(b) C_O = 470 µF

Figure 3. Power Switch Power-Up Into a Pure Capacitive Load

To clearly show the peak current in Figure 3(b), a *zoomed-in* view of the waveform is illustrated in Figure 4. The spike current peaks at about 350 mA. Comparing Figure 3(b) to the waveforms in Figure 1, shows that using the TPS2151 yields a much lower inrush current.

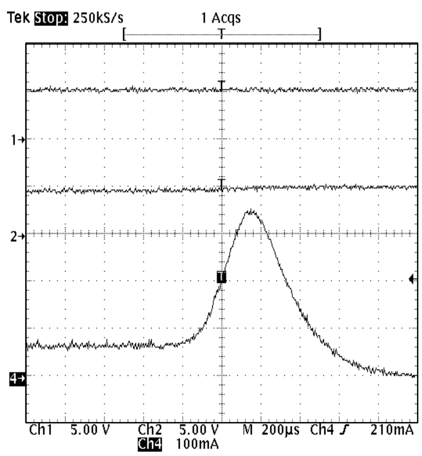
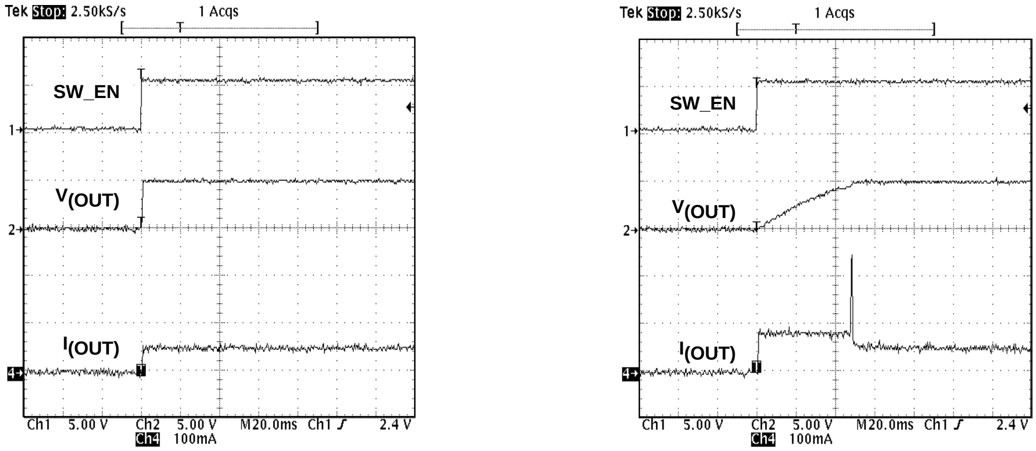


Figure 4. Power Switch Power-Up Into a Pure Capacitive Load
(*Zoomed-in* View of Figure 3(b))

Powering Large-Current Loads With the TPS2150/51

The features of the TPS2150/51 allow the designer the flexibility to design in various applications. If a high dc current load is present at the output, power sequencing may be needed to avoid start-up issues.

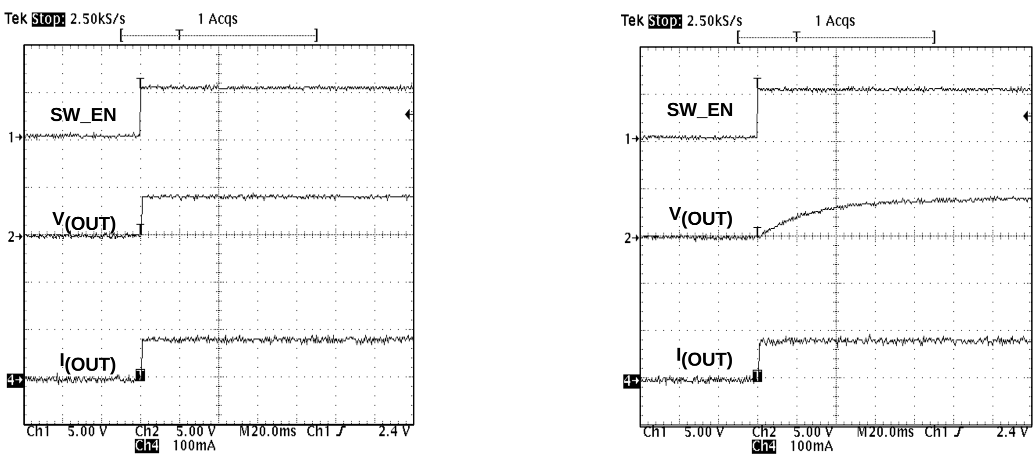
If the dc load current during the turnon period is lower than or equal to 50 mA (which is lower than the low current limiting of the power switch), the device successfully powers up as shown in Figure 5(a) and 5(b) with different output capacitance.



(a) C_O = 4.7 μF **(b) C_O = 470 μF**

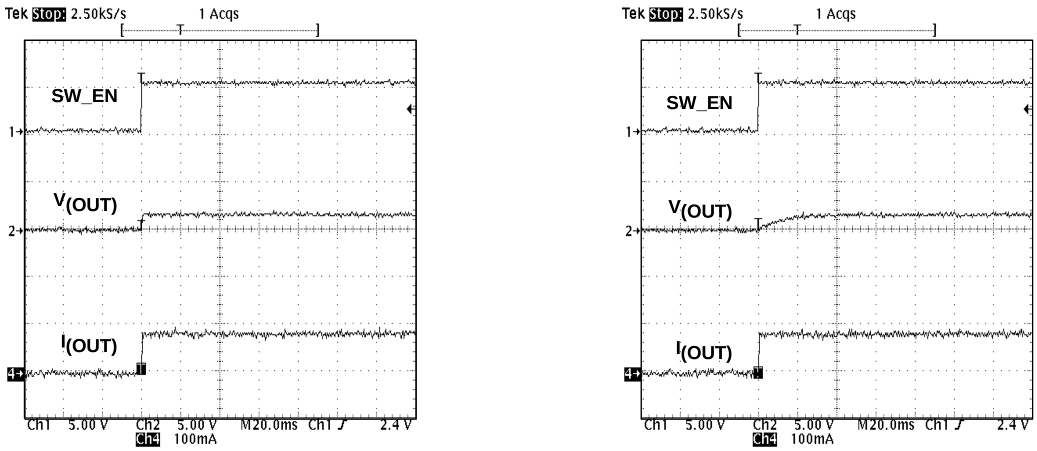
Figure 5. Power Switch Power-Up With Small DC Load (R_L = 100 Ω)

In contrast, Figure 6 and Figure 7 show the results with heavier loads. The load capacitance does not charge up to the input voltage level, due to the low current limit on the power switch. With a load that is larger than the equivalent low current limit I_{LMT_LO} (about 75 mA), the output voltage can only be charged up to $I_{LMT\_LO} \times R_L$.



(a) C_O = 4.7 μF **(b) C_O = 470 μF**

Figure 6. Power Switch Power-Up With 50-Ω DC Load



(a) C_O = 4.7 μF **(b) C_O = 470 μF**

Figure 7. Power Switch Power-Up With 20-Ω DC Load

With the power-good reporting feature of the device, applications with large dc current loads can be powered with power sequencing control through the SW_PG signal of the device, as shown in Figure 8. The load is turned on or off by the signal at the ON input. If an active-high control signal of the load is not available, the logic of SW_PG can be inverted externally before feeding it to the control signal of the load.

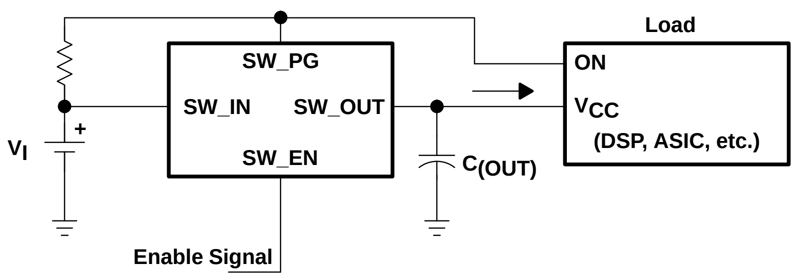
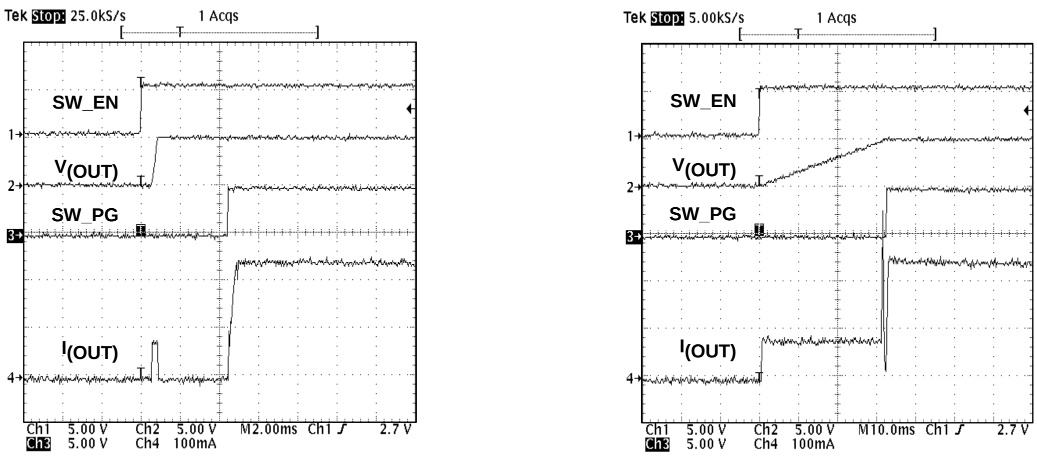


Figure 8. Power Large Load Through Power Sequencing

Figure 9 shows the results for a 250-mA load that is controlled by SW_PG. The load turns on after the output voltage is fully charged, indicated by SW_PG. Because the SW_PG has an internal deglitch filter, a delay from the output voltage being available to the power–good signal going active is noticed.



(a) C_O = 4.7 µF **(b) C_O = 470 µF**

Figure 9. Powering Large-Current Load With TPS2150/51

It is very rare that an enable (ON/OFF or similar) pin is not available for portable or USB functions. However, if such a control signal is not available, a simple power distribution switch, like the TPS2051A, can be used to transfer the power from the TPS2150/51 switch output to the load as shown in Figure 10.

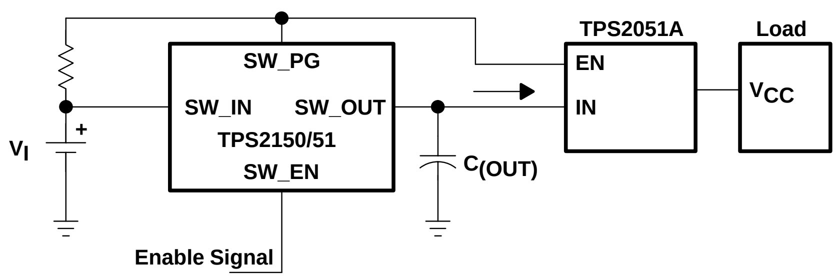
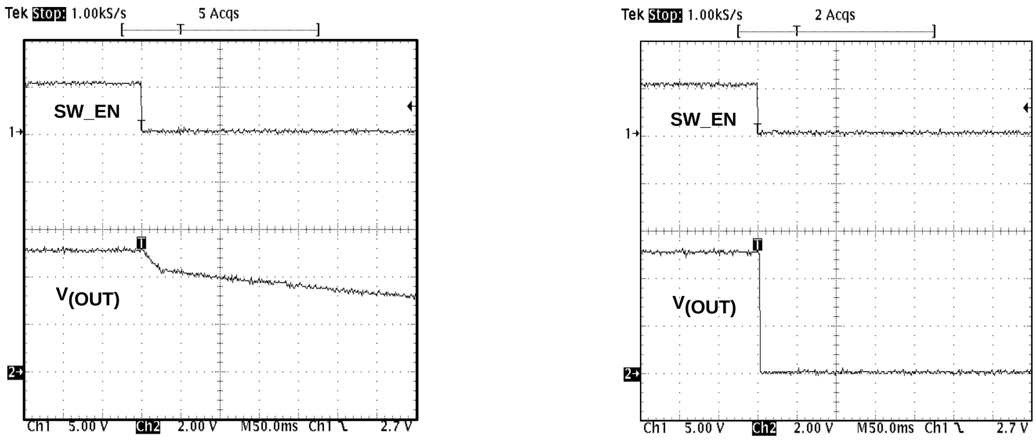


Figure 10. Powering Large Load Through Power Sequencing for Loads Without an Enable

Fast Turnoff Discharge With TPS2150/51

Another useful feature of the TPS2140/41/50/51 is the availability of two integrated discharge transistors. The power switch output can be discharged by using the SW_PLDN pin and the LDO output can be discharged by using the LDO_PLDN pin. For example, if a quick discharge is required for the power switch output (SW_OUT), connect SW_PLDN to SW_OUT. When the power switch is enabled, the discharge transistor connected to SW_PLDN is off, thereby not affecting the performance of the power switch. If the power switch is turned off, the discharge transistor turns on and quickly discharges the output voltage.

Figure 11 demonstrates the effect of the integrated pulldown transistor, using the power switch as an example. Even if the output capacitance (4.7 µF) is small, the natural discharge time can be very long when there is no load other than the capacitor. When SW_PLDN is connected to SW_OUT, the discharge speed is much faster, as shown in Figure 11(b).



(a) SW_PLDN Not Connected **(b) SW_PLDN Shorted to SW_OUT**

Figure 11. Turnoff Output Voltage Waveforms With C_O = 4.7 μF

If a fast discharge is not necessary for the application, the SW_PLDN and LDO_PLDN pins can be left unconnected.

Design Example for Portable USB Application

A design diagram for a typical portable USB application is shown in Figure 12.

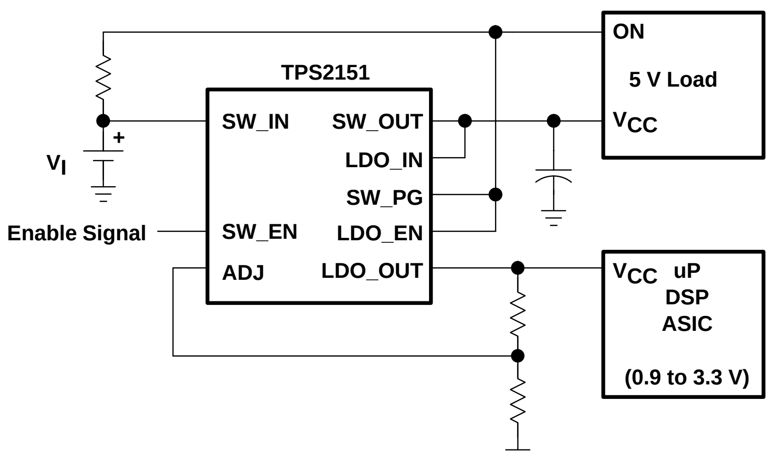


Figure 12. Design Diagram of a Typical Portable USB Application

The SW_PG is used to enable the 5-V load and the internal LDO that powers the lower voltage load. If the lower voltage load needs power sequencing after LDO power-up, the power-good reporting signal LDO_PG of the LDO (not shown in the diagram) can be used in the same way as SW_PG.

Conclusion

The TPS2150 and TPS2151 power managers provide a perfect and cost-effective way to control power-up inrush current and meet USB 1.0 and 2.0 specifications. They also include a low-dropout voltage regulator and some other unique features, so the devices can power different loads for portable and USB applications.

IMPORTANT NOTICE

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