

APPLICATION NOTE

GC2011-AN9801

Filtering TDM Data Using the GC2011 Digital Filter Chip

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Revision 0.0

This application note describes how to simultaneously filter 4 or 8 sampled signals in a single GC2011 Digital filter chip. The input data is multiplexed in a time division multiplexed (TDM) format. In the dual path mode the chip will process two TDM data streams, each containing four signals for a total of 8 signals. In the cascaded mode the chip will process a single TDM stream containing four signals.

1.0 TDM DATA MODE

Four signals can be processed in each filter path in the TDM mode. In the Dual path mode the GC2011 can process a total of 8 signals, in the cascaded mode the chip can process a total of 4 signals. In the TDM mode each filter cell stores four data samples and multiplies them separately times the same coefficient. The cells' delay lines are adjusted so that four feed-forward and four feedback data samples are delayed within each filter cell. The accumulator at the end of the filter path is disabled so that the filtered outputs are output in the same TDM fashion. The chip is configured in the TDM data mode using the control settings shown in Table 1.

Symmetry	Dual Path or Cascaded	# of Taps (N)	A-PATH		B-PATH		Cascade	Latency
			REG0	REG1	REG0	REG1	REG	Latency
None	Dual	16	20D8	0200	00D8	0200	2000	50
	Cascaded	32	20D8	0228	00D8	0200	5E00	66
Even	Dual	32	20D8	0211	00D8	0211	2000	50
	Cascaded	64	20D8	0228	00D8	0211	5E00	66
Odd	Dual	31	20D8	0284	00D8	0284	2000	50
	Cascaded	63	20D8	0228	00D8	0284	5E00	66

Table 1: TDM Mode Control Register Settings

The coefficients are stored in coefficient register 1 of each filter cell using the formula:

Store h(k) in memory address BASE+4*k+1

where BASE is 128 for A-path or cascaded filters and is 192 for B-path filters. To use coefficient register 3 of each cell use addresses BASE+4*k+3 and change REG0 in Table 1 to 20F8 for A-PATH and 00F8 for the B-PATH.

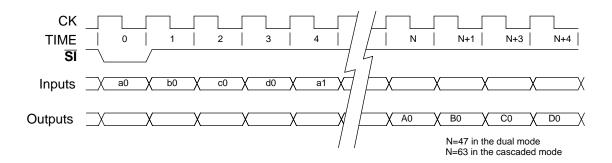


Figure 1. TDM Mode I/O timing

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