Simple DSP interface for ADS784x/834x ADCs

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Introduction

The 12-bit ADS7841 and 16-bit ADS8341/3 are pin-compatible, 4-channel analog-to-digital converters (ADCs) with a synchronous serial interface. Typical power dissipation is 2 mW at a 200-kHz throughput rate on the ADS7841 and 8 mW at 100 kHz on the ADS8341/3. The 12-bit ADS7844 and 16-bit ADS8344 are pin-compatible, 8-channel ADCs with the same typical power requirements as their 4-channel cousins.

The low power, high speed, and onboard multiplexer of these devices make them ideal for battery-operated systems such as personal digital assistants, portable multichannel data loggers, and measurement equipment.

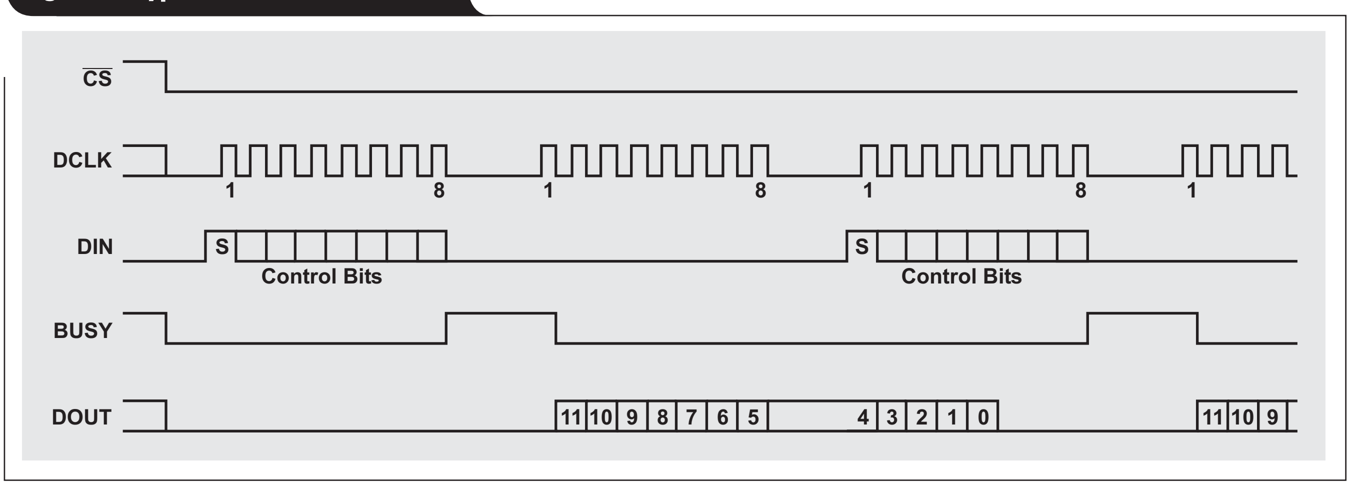
The datasheets for these devices show various ways to interface the parts to microcontrollers with a serial peripheral interface (SPI), but they do not mention how to use these parts with high-performance digital signal processors (DSPs). This article provides an easy way to connect these parts with any Texas Instruments (TI) DSP that contains at least one multichannel buffered serial port (McBSP). The information here pertains to the TMS320F2812 and all devices in the TMS320C5000™ and TMS320C6000™ DSP platforms.

Digital interface for microcontrollers

The digital interface section of the datasheet for all five of these devices shows a typical SPI with burst clock mode of operation based on 8 or 16 clock cycles. While an SPI interface is certainly not difficult to implement, there can be a bit of difficulty associated with getting the received data into a format that the processor can actually use. Figure 1 shows a typical 8-bit SPI interface.

The difficulty many users run into with this interface is in formatting return data with minimal software overhead. At first glance, it is not always obvious to new users of these parts that the most significant bit (MSB) is presented on the 9th clock cycle. With a microcontroller like the MSP430 series of devices and the SPI interface shown in Figure 1, the 7 MSBs of data are stored in an 8-bit register, with the 5 least significant bits (LSBs) stored in a second 8-bit register. In order to store the converted data in a meaningful fashion, both the upper and lower bytes would need to be shifted (left or right) and then concatenated before being stored into a data array for future processing. In applications such as motor control, the software latency of these data manipulations proves too costly.

Figure 1. Typical 8-bit SPI interface



The process can be simplified a little if the microcontroller is capable of running with a 16-bit SPI interface, such as the TMS470 series of devices from TI. For the 12-bit parts, all returned data can be captured in a single 16-cycle transmission. To accomplish this, simply shift the command byte to the left by 7 bits as shown in Figure 2. The SPISCS line shown in Figure 2 could be tied to the chip select line of the ADC if multiple devices share the SPI bus.

The modified 16-clock SPI interface of Figure 2 sends the BUSY signal high on the falling edge of the 15th clock. In some applications, this approach might still require a data shift. The 12-bit data is MSB-aligned and the MSB is provided twice. The software overhead becomes less of an issue in this case since the shift can be done during the actual data reception in the SPI routine.

There are two drawbacks to this approach—first, the LSB is lost. The LSB is cut short during the switch from sample to hold mode and the host processor will always read it as a “one.” The second issue is latency. These converters enter their acquisition phase after the A0 bit is read into the part. The data shown in Figure 2 would be the conversion results from the previous cycle, which adds latency to the system.

When the 16-bit parts are used, the problem is aggravated even further. An 8- or 16-bit SPI device like the MSP430 or TMS470 would need to issue at least 24 SCLKs to complete a 15-bit transfer. If the entire 16 bits of data are needed, a total of 32 clocks would be required. Data manipulation would still need to be done, adding software overhead.

Digital interface for TI DSPs

Using the high speed and flexible capabilities of the McBSP ports found on the TMS320F2812 or the C5000™ and C6000™ DSP platforms can virtually eliminate the software overhead associated with the microcontroller and the SPI interface.

The McBSP ports have independent transmitter and receiver functions. Since transmit and receive sections are independent, transmit and receive frame sync (FS) signals are also independent. If the chip select (/CS) signal is tied low, the BUSY signal can be used as the frame sync return (FSr) to indicate that a serial stream is on its way into the receiver. The data transfer to the DSP is done without any further need for manipulation. Setting the data transfer length in the DSP to 16 bits allows exactly the same software routine to be used with the 12-bit ADS7841 or the 16-bit ADS834x devices.

Figure 2. Modified 16-clock SPI interface

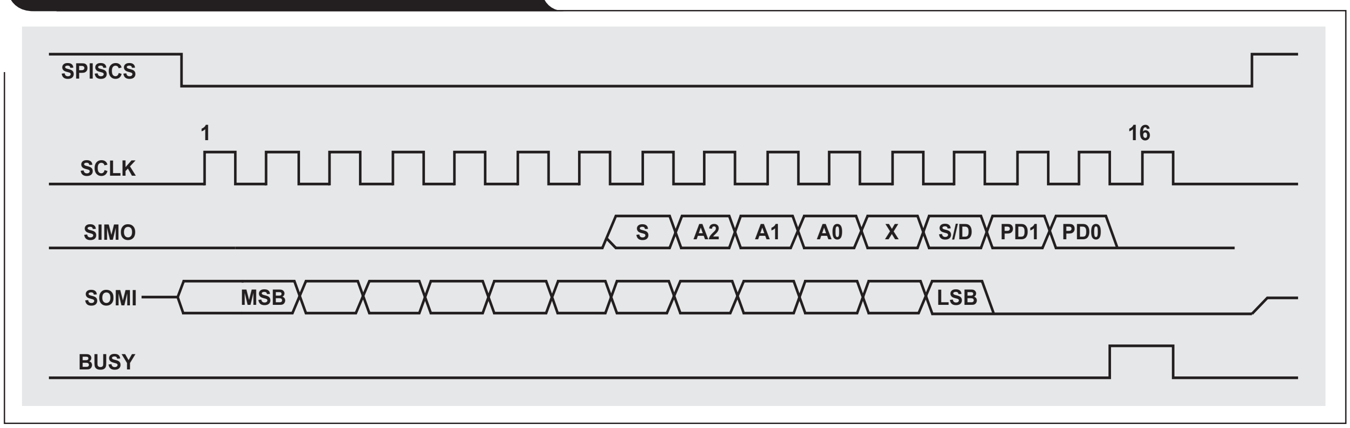
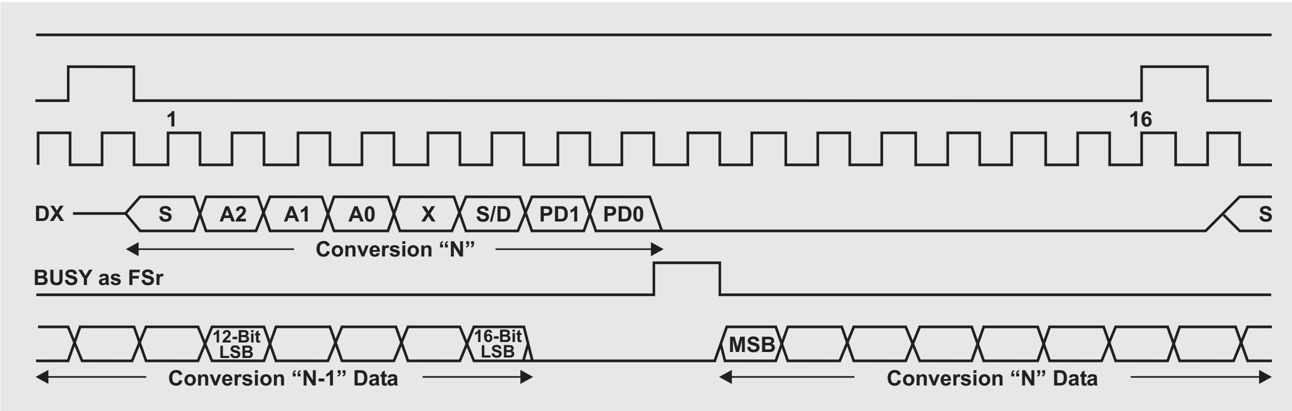


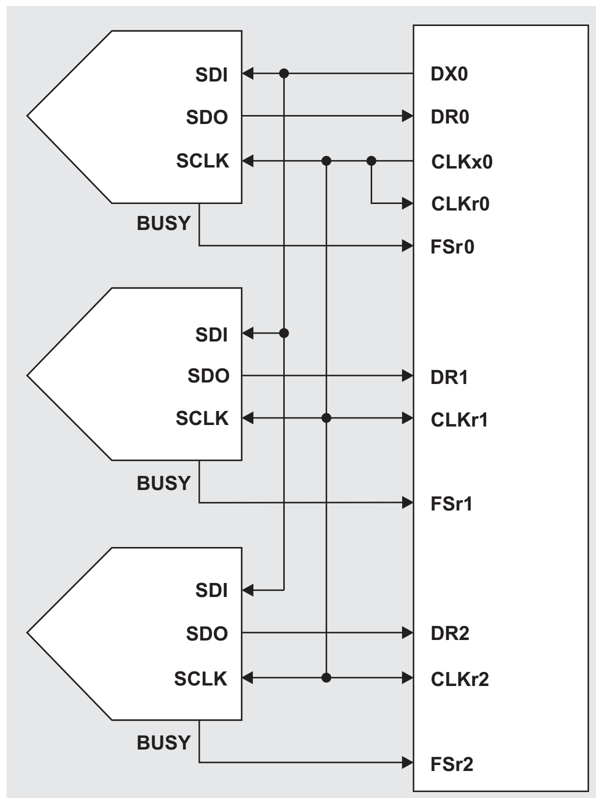
Figure 3. DSP transfer with 16 clock cycles



As shown in Figure 3, the output data is actually wrapped between conversion start commands so that there is minimal latency between conversion cycles. Data is presented to the DSP MSB first from both the 12-bit and 16-bit devices. If LSB alignment is required, a 4-bit shift could be implemented to the received data as it is sampled.

Another added advantage of using the DSP is the possibility to realize simultaneous sampling on up to three devices on a DSP with multiple serial ports. This would be done by using a single "master" transmitter tied to all three ADCs and returning the master clock to all three "slave" receiver ports. The BUSY signal from each of the three ADCs would again act as the FSr to each receiver. Figure 4 shows a potential method for implementing multiple ADCs in a simultaneous sampling application.

Figure 4. Multiple ADC configuration



Conclusion

The ADS784x/ADS834x data converters are truly versatile with their simple serial interface, low power, high-speed operation, and ease of use. They are ideal for portable and handheld applications that require excellent performance capability and upgrade flexibility. For additional information on the devices mentioned in this article, please contact your local distributor, the TI Product Information Center listed on the last page of this document, or the Data Converter Applications team at dataconvapps@list.ti.com

Related Web sites

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