A low-cost, non-isolated AC/DC buck converter with no transformer

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Introduction

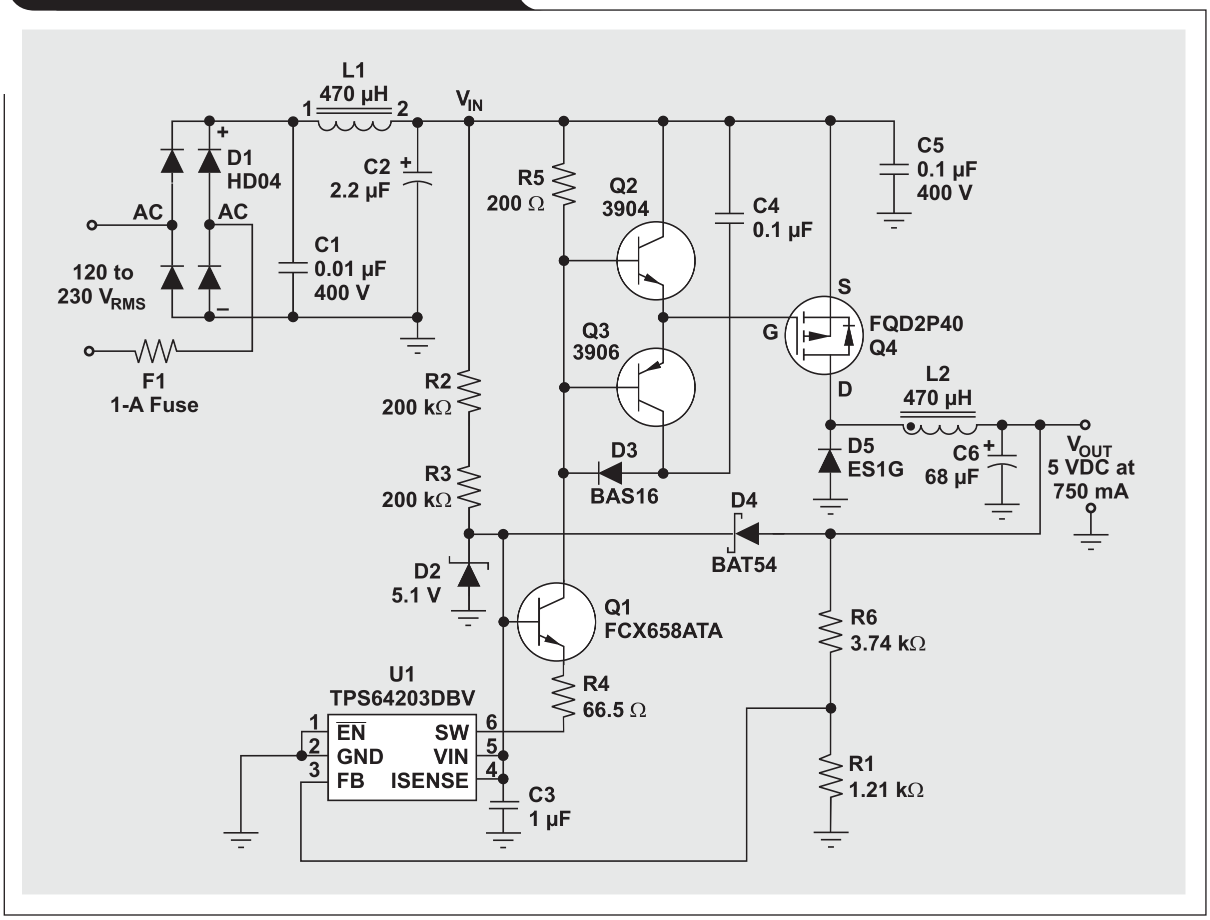
Off-line equipment such as a smart meter or a power monitor has electronics that require non-isolated DC power under 10 W. Until recently, the only practical options for providing a low-power DC power rail from an AC source were to use an extremely inefficient, unregulated resistive/capacitive divider following the rectifier, or a flyback DC/DC converter that was cumbersome to design. Advances in MOSFET technology and an innovative gate-drive circuit for a hysteretic buck controller have resulted in an ultra-low-cost DC power rail.

Figure 1 shows the entire converter. The rectifier circuit uses a standard, fast-switching rectifier diode bridge (D1) and an LC filter (L1 and C2). The remaining components will be explained in more detail.

The basic buck converter

The TPS64203 is a hysteretic buck controller designed to drive a high-side pFET and has minimum turn-on and minimum turn-off switching-time requirements. Unlike a traditional hysteretic converter with a switching frequency that varies with load current, the minimum on and off times essentially clamp the switching frequency when the converter begins to run in continuous-conduction mode at high output-power levels. Other members of the TPS6420x family actively avoid switching in the audible frequency range, effectively having a maximum on and off time. Originally designed for battery-powered applications, the TPS6420x family has an input-voltage range of 1.8 V to 6.5 V and very low quiescent current (35 µA maximum). During start-up, the TPS64203 is biased by Zener diode

Figure 1. AC/DC buck-converter circuit



D2 and high-voltage resistors R2 and R3. After the 5-V rail is up, Schottky diode D4 allows the 5-V output rail to power the controller.

Power FET Q4 must have a high enough V_{DS} voltage rating not to be damaged by the input voltage, and a high enough current rating to handle $I_{PMOS(RMS)} = I_{OUT(max)} \times \sqrt{D_{max}}$. It must also be in a package capable of dissipating $P_{Cond} = (I_{OUT(max)} \times \sqrt{D_{max}})^2 \times R_{DS(on)}$. Traditionally, high-voltage p-channel FETs have had a gate capacitance or turn-on/off times that were too large, a drain-to-source resistance ($R_{DS(on)}$) that was too high, a threshold voltage (V_{TH}) that was too large, and/or have simply been too expensive to make a circuit like the one in Figure 1 practical (i.e., efficient enough relative to cost). Since the high line of 230 V_{RMS} + 10% tolerance comes from the 350-V_{PK} AC line, the FET, filter, and input capacitors need to be rated for 400 V.

The FQD2P40 is a relatively new, 400-V p-channel MOSFET. With an $R_{DS(on)}$ of 5.0 Ω from a 10-V gate drive and a total gate charge of less than 13 nC, this FET can easily be switched by the controller—with relatively fewer conductive and switching losses than older FETs—with the help of the innovative drive circuit consisting of Q2, Q3, C4, and D3. The converter's rectifying Schottky diode, D5, is selected with a voltage rating capable of blocking the input voltage, a peak-current rating slightly higher than the output voltage, and an average current rating of $I_{Diode(Avg)} = (1 - D) \times I_{OUT(max)}$. With a D_{max} of 5 V/120 V = 0.04 and such low output power, the peak-current rating and the power dissipation are not a concern in either switch.

The buck power stage's LC filter is designed as explained in the TPS6420x family data sheet. With the input voltage being much larger than the output voltage, all of the TPS6420x controllers will run in minimum-on-time mode. Equation 1 computes the recommended buck-converter inductance at high line, assuming that K = 0.4 for the inductor's ripple-current factor.

$$L = \frac{(V_{IN} - V_{OUT}) \times t_{on(min)}}{\Delta I_L} = \frac{(230\ \text{V} - 5\ \text{V}) \times 0.65\ \mu\text{s}}{0.4 \times 0.750\ \text{A}} \quad (1)$$

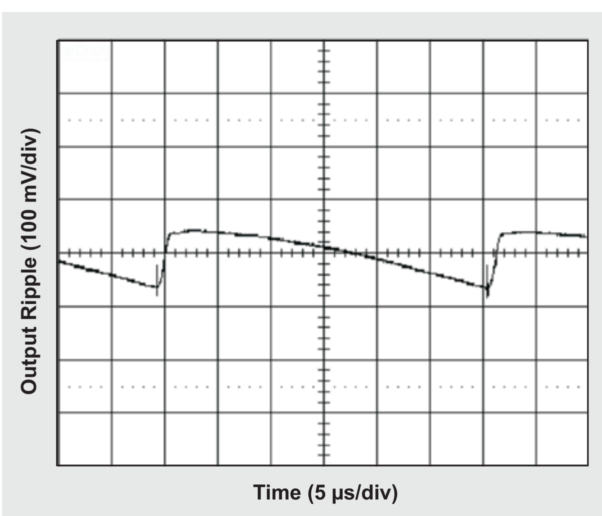
$$= 488\ \mu\text{H} \rightarrow 470\ \mu\text{H}$$

The relatively high K value minimizes inductor size and proves to be acceptable because the steady-state output-ripple requirement for this particular application was no larger than 0.02 × V_{OUT}, or 100 mV_{PP} at high load. Being hysteretic, the TPS6420x controllers typically work best with some ripple on the output voltage. An output capacitor with at least 50-mΩ ESR is recommended and would produce a ripple voltage of $\Delta V_{PP(ESR)} = \Delta I_L \times R_{ESR}$, which typically far exceeds the capacitive component of the voltage ripple. The measured ripple for this application is shown in Figure 2.

Because the TPS64203 is hysteretic, its output voltage will have higher ripple at lower output power when it is running in pulsed-frequency mode. The measured operating frequency of the converter is approximately 32 kHz, which agrees with the predicted value of

$$f_{SW} = \frac{D_{min}}{t_{on(min)}} = \frac{5\ \text{V}/250\ \text{V}}{0.65\ \mu\text{s}} = 31\ \text{kHz}.$$

Figure 2. Output ripple at V_{IN} = 250 VDC and I_{OUT} = 500 mA



How the drive circuit works

Bipolar transistor Q1 and resistors R4 and R5 form a constant-current-driven level shifter that allows the low-voltage TPS64203 controller to operate the discrete gate-drive circuit formed by Q2 and Q3. Like the controller, the level shifter is powered by Zener diode D2 at start-up and the regulated 5-V rail, through Schottky diode D4, after start-up. Power FET Q4's gate must be overdriven just enough to provide the required output current with an acceptable $R_{DS(on)}$. Too much drive increases switching losses, while too little increases conduction losses. From a review of the FQD2P40 data sheet and some trial and error, $V_{GS} \cong 12$ V was selected.

Capacitor C4 and diode D3 are critical to the drive circuit's functionality. Resistor R5 is selected to set the gate-drive level of 12 V below the voltage at the rectifier's output. Diode D3 clamps capacitor C4 to this level. Specifically, when U1's switch pin outputs a low signal to turn on the power FET, the signal gets level shifted to the base of Q3. Transistor Q3 turns on and quickly charges Q4's gate-to-source capacitance, C_{GS}, to 12 V. Without C4 and D3, turning off Q4 would have required Q3 to be an expensive, high-voltage bipolar transistor with its drain tied to ground. When U1's switch pin outputs a high signal to turn off the power FET, the signal gets level shifted to the base of Q2. Q2 turns on, effectively tying Q4's gate to the input voltage. It is important to note that without capacitor C4 acting as a local power supply, transistors Q2 and Q3 would not be able to provide the fast current spikes necessary to quickly —and therefore efficiently—pull up or pull down Q4's gate capacitance. Also, the level shifter's current, I_{LS}, set by R4, must be high enough to move Q4's gate charge, Q_{Gate}, during the $t_{on(min)}$. That is,

$$I_{LS} = \frac{V_{Z(D4)} - V_{BE}}{R4} >> \frac{Q_{Gate}}{t_{on(min)}}.$$

Capacitor C4 is sized to be much larger than Q4's gate capacitance, but it must be small enough that it can be recharged during the shorter of the controller's minimum on and off times. Figure 3 shows the gate and drain turn-on/off times during one switching cycle with an input voltage of 300 V and a 500-mA load. Measured conversion efficiency is shown in Table 1.

Current limit and soft start

In low-voltage applications, the TPS6420x uses a high-side current-limit circuit to compare the drop across a current-sense resistor, placed between the VIN and ISENSE pins, to a reference voltage. If the voltage across the sense resistor exceeds that voltage, the circuit turns off the switch, thereby implementing a pulse-by-pulse current limit. In a high-voltage application, the current-limit circuit cannot be used without overvoltage on the ISENSE pin, so the ISENSE pin is tied high to VIN. Therefore, the circuit in Figure 1 does not have a current limit. A high-side series fuse is recommended to provide short-circuit protection.

In typical applications during start-up, the TPS64203's current-limit value is slowly ramped up to provide a current-limited, controlled soft start. In this application, the current-limit circuit and therefore the soft start are disabled; therefore, the start-up inrush current may be large and the output voltage may overshoot slightly, as shown in Figure 4.

Conclusion

Using a level shifter and gate driver with a localized power source allows the use of a low-voltage buck controller to provide a DC voltage from an AC power source. Conversion efficiency near 60% can be achieved by using a simple circuit and no transformer. This circuit can also be used for DC/DC conversion where the input DC voltage is above the maximum rating of the TPS6420x.

Related Web sites

power.ti.com
www.ti.com/sc/device/TPS64200

Figure 3. Q4 gate and drain voltages during one switching cycle

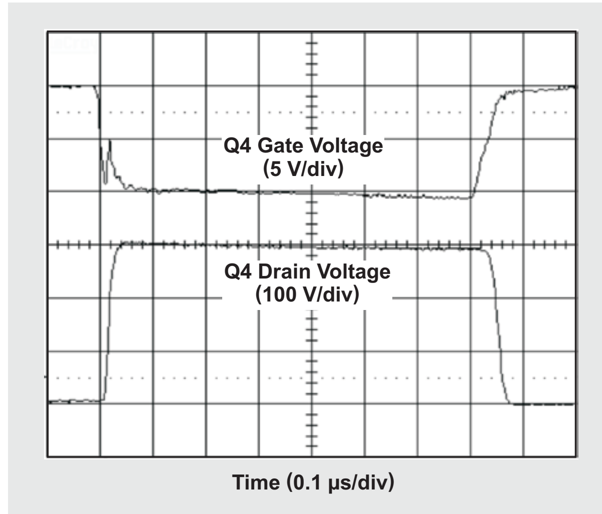
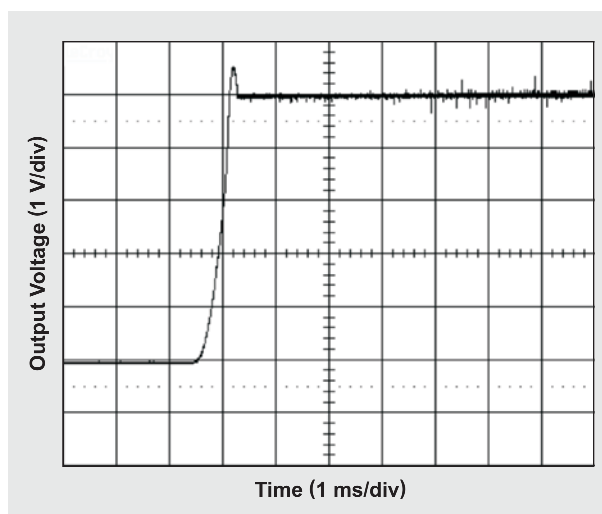


Table 1. Measured conversion efficiency

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	I_{OUT} (A)	V_{OUT} (V)	P_{OUT} (W)	EFFICIENCY (%)
100	0.043	4.3	0.5	5.023	2.5115	58.40698
200	0.021	4.2	0.5	5.023	2.5115	59.79762
300	0.015	4.5	0.5	5.023	2.5115	55.81111
100	0.066	6.6	0.75	5.023	3.76725	57.07955
200	0.031	6.2	0.75	5.023	3.76725	60.7621
300	0.022	6.6	0.75	5.023	3.76725	57.07955

Figure 4. Start-up into a 10-Ω load with V_{IN} = 300 V



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