Application Report
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AN-1463 Design and Layout Guidelines for SCAN25100

ABSTRACT

The SCAN25100 is a 2457.6, 1228.8, and 614.4 Mbps serializer/deseralizer (SerDes) for high-speed bidirectional serial data transmission over FR-4 printed circuit board backplanes, balanced cables, and optical fiber. This high-speed operation is achieved without significant layout and overall PCB design constraints. However, adhering to a few specific layout guidelines will optimize signal integrity and performance.

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The SCAN25100 is a 2457.6, 1228.8, and 614.4 Mbps serializer/deserializer (SerDes) for high-speed bidirectional serial data transmission over FR-4 printed circuit board backplanes, balanced cables, and optical fiber. This high-speed operation is achieved without significant layout and overall PCB design constraints. However, adhering to a few specific layout guidelines will optimize signal integrity and performance.

1. AC coupling capacitor placement, size and value
2. High speed differential signaling options (microstrip / stripline / twin-ax cable)
3. REFCLK terminations
4. DDR impedance recommendations
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2 AC Coupling On D_{OUT} and R_{IN}

In many cases the SCAN25100 will be interfacing to a SFP (Small Form Factor Pluggable) or similar Optical Transceiver. This type of connection is always AC coupled, many optical modules available today already include AC coupling. This means the PCB connection between the SCAN25100 and the optical module will be a direct interconnect and will not require any additional passive components.

In applications that involve copper cables, the transmission distance will be limited by the loss characteristics of the cable. The ability of the SCAN25100 CML IO to use de-emphasis and equalization will extend the transmission distance beyond 20 meters in most cases. For when cables are used between sub-systems that reside 10's of meters apart, significant ground shifts often occur. To combat this issue, external AC coupling capacitors must be inserted in the signal path. Though the placement of these DC blocking capacitors is not critical, choosing the correct value and minimum body size will minimize any impedance discontinuities in the signal path.

The most common serial encoding used with the SCAN25100 will be 8B/10B. This scheme limits the maximum run length of consecutive 0's or 1's to 5 bits, thereby defining our minimum frequency of interest when selecting an AC coupling capacitor value. For the SCAN25100 a capacitor value of 1.0 µF will give excellent signal fidelity at all CPRI rates. A smaller capacitor may be chosen if only the fastest rate of 2.4576 Gbps will be used in the application. For the physical size smaller is better, microstrip lines that support 50 ohm single-ended or 100 ohm differential impedance will always be less then 20 mils wide and in some differential cases, much less. Keeping the body width of the AC coupling capacitor nearly the same size as the microstrip line width minimizes signal losses and impedance discontinuities. Figure 1 illustrates the AC coupling capacitors.

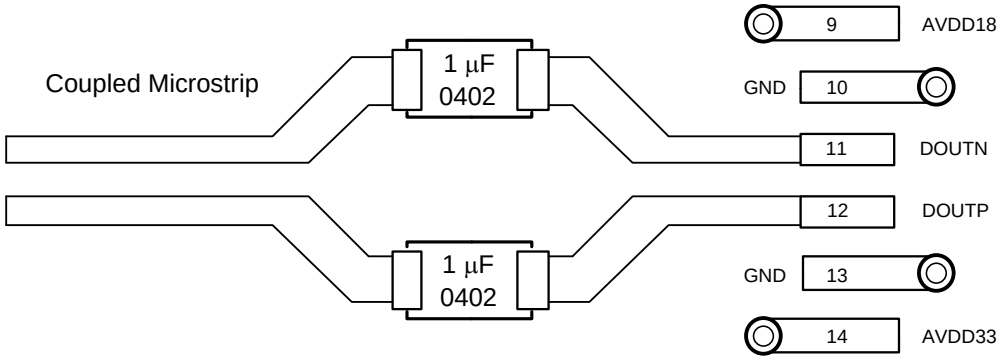

Figure 1. AC Coupling on the SCAN25100 CML IO

Component to component spacing constraints will not allow running differential lines to the capacitors. As the spacing between the lines is increased the coupling is reduced and the PCB traces begin to act as single-ended traces instead of differential traces. To compensate for this the width of the PCB traces will have to be enlarged to maintain a constant impedance profile. An example 100Ω differential microstrip is shown in Figure 2. To maintain the impedance at 100Ω when the traces are uncoupled (S >> W), the width must be increased by 3.4 mils to 12 mils.

If the PCB trace width in Figure 1 had not been increased, a short segment of 115Ω transmission line would be seen in the signal path resulting in increased jitter.

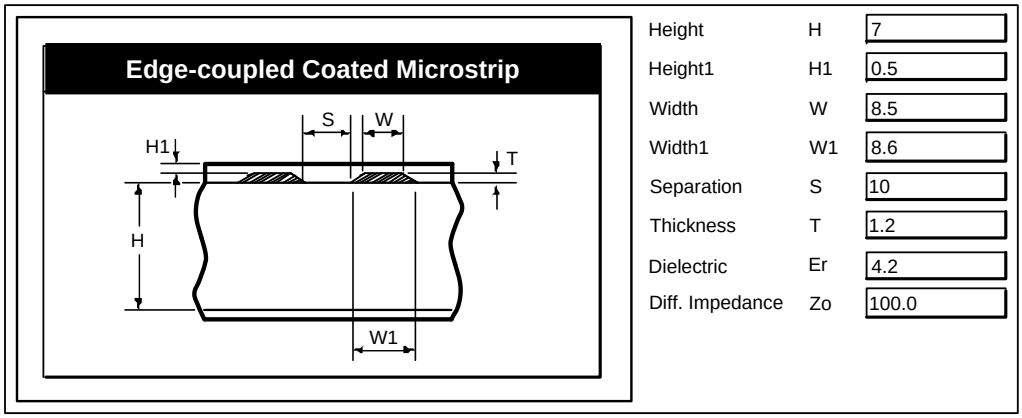

Figure 2. Edge-Coupled Microstrip Line with 100Ω Impedance

3 High-Speed Signaling Options

In many cases the SCAN25100 will be interfacing to a SFP (Small Form Factor Pluggable) or similar Optical Transceiver. This type of connection is likely to be very short. Due to the relatively short length it is possible to route the signals on the top layer as differential microstrip. When longer connections are required it is preferable to utilize internal signal layers to minimize the opportunity to pick up interference from other noise sources. Using internal PCB layers for high speed signaling will also minimize emissions from the high-speed CML signals. Vias are used to move between PCB layers, an example of this is shown in Figure 3.

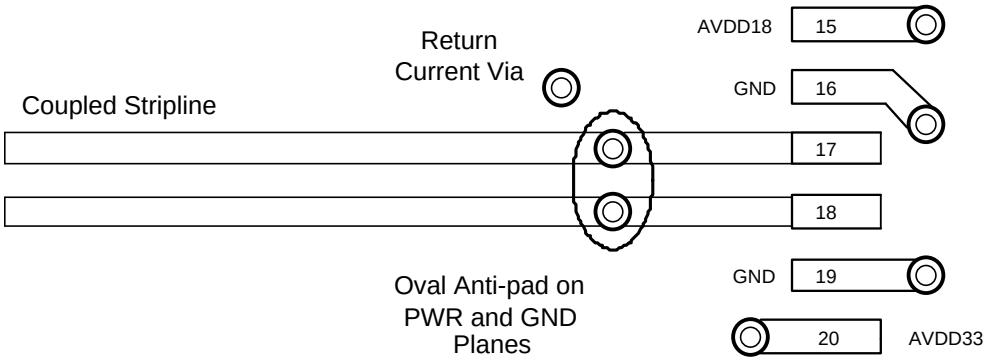

Figure 3. Differential Vias with Oval Anti-pad

Small vias, with a drill size of 8 mils or less, should be used to minimize mutual capacitive coupling between via and nearby ground or power planes. Differential via structure with shared oval-shaped anti-pad can further reduce parasitic capacitance. Placing a return current via immediately adjacent to the signal vias will improve signal fidelity at multi-gigabit speeds. The return current via allows a low inductance path between reference planes in the PCB minimizing the impedance discontinuity across the via structure.

4 REFCLK Termination

There are several possibilities for input termination on REFCLKP/N. The most common termination, especially for LVDS outputs like SYSCLK will be a simple 100Ω resistor across the differential input. This resistor should be placed the minimum distance from the REFCLK inputs as shown in Figure 4.

For LVPECL style outputs the termination requirements may vary. The termination style can generally be determined from the manufacturers datasheet. Most common is a 2x50Ω center tapped termination to V_{DD} – 2.1 volts.

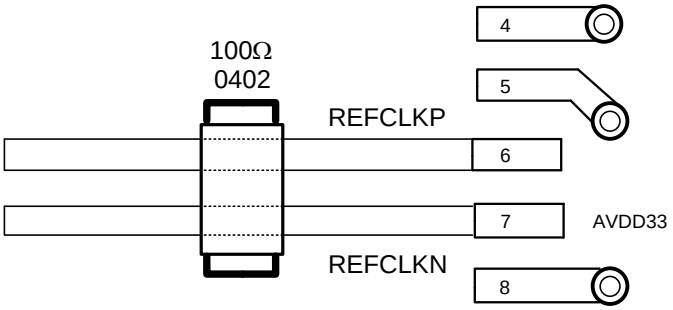

Figure 4. 100Ω Termination on REFCLK Inputs

5 DDR Impedance Recommendations

The SCAN25100 has been designed with DDR outputs intended to drive transmission lines with a nominal impedance of 60–65Ω. The outputs ROUT[0:9] and RXCLK rely on reflected wave switching for good signal integrity and low dynamic power. For this interface no internal or external termination is required at the load. The only requirement is for the PCB layout to be designed to achieve a nominal impedance of 60Ω–65Ω. This matches the nominal output impedance of the DDR outputs.

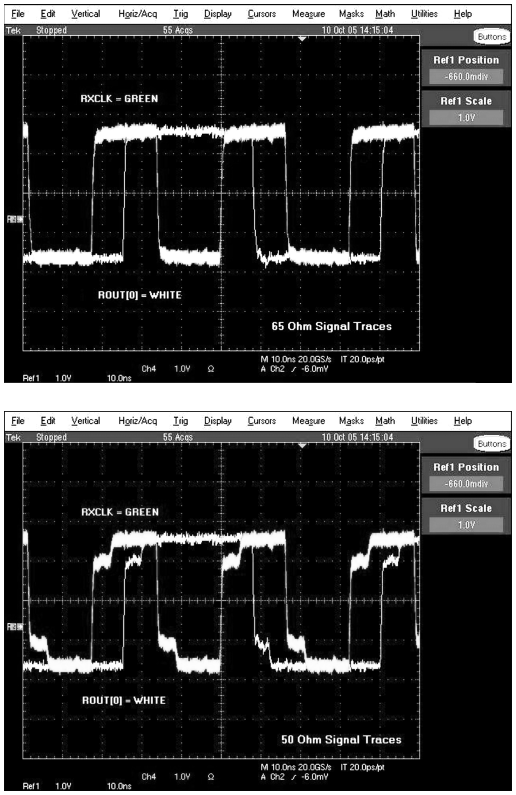

Figure 5. 65Ω Environment on Left and 50Ω Environment on Right.

As shown in Figure 5, choosing a PCB impedance lower then 60Ω will result in reduced noise margins, PCB impedance above 65Ω will result in some overshoot and undershoot noise at the load.

6 Decoupling

Each power or ground lead of the SCAN25100 should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding trace inductance. Placing power plane closer to the top of the board reduces effective via length and its associated inductance.

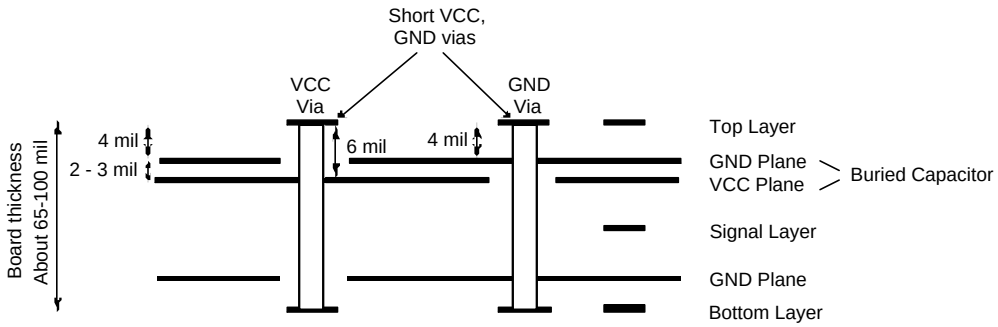

Figure 6. Low Inductance, High Capacitance Power Connection

Bypass capacitors should be placed close to VDD pins. They can be conveniently placed near the corners of the TQFP package. Small physical size capacitors, such as 0402, X7R, surface mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor. An X7R surface mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 µF, and 0.1 µF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2–3 mils. With a 2 mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. An example of this is shown in Figure 6.

The center dap of the TQFP package housing the SCAN25100 should be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the TQFP package.

7 Power Filtering

The PVDD33 supply is used to provide power to the onboard PLL and CDR units. Keeping this supply free of noise ensures optimal device performance. Isolating the PLL supply from the other SCAN25100 supply connections and more importantly large sources of digital noise like FPGAs is the easiest way to keep noise low. Figure 7 shows an island VDD connection for the PLL and CDR supply pins. Input power to this island is routed through either an LC low pass filter. Local decoupling for the PLL and CDR supply connections must also be provided on-board to further filter and stabilize this supply voltage. While creating this filtered power island it is important to consider the effects on other supply pins and return currents on the PCB. Reducing the size of the island to the area under the SCAN25100 eases PCB constraints, specific implementations should be checked to ensure no other supply issues have been created due to this area of isolation under the SCAN25100.

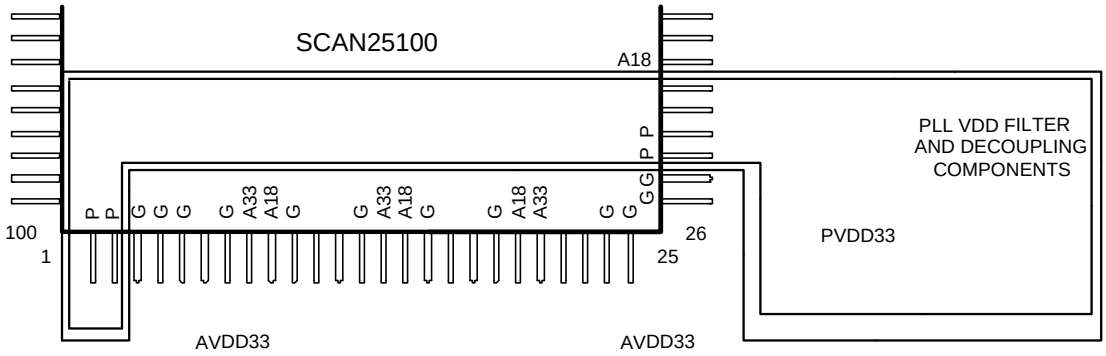

Figure 7. Isolated 3.3V Supply for PVDD33 Connections on the SCAN25100

The PVDD33 supply LC filter components should be chosen to provide significant attenuation at and above power supply switching frequencies in the system. Generally switching power supply frequencies have been increasing to reduce component size and cost. This trend in switching power supply design aids component selection for the SCAN25100 power supply filter. The external LC filter is a relatively simple 2nd order low pass design. Although the RC network is slightly cheaper, the solution limits the maximum attenuation that can be achieved.

1. The series R of an RC filter reduces the voltage on the PVDD33 pins. This constraint limits the value of resistance to relatively low values. Requiring a physically larger capacitor to achieve reasonable attenuation characteristics.
2. With only one reactive element, the RC filter is a 1st order design. This limits attenuation to 20 dB/decade at higher frequencies.

To design an effective LC network it is best to start by defining the source and load impedances that are expected in the application. The PVDD33 has a typical current consumption of 80 mA with an absolute maximum of almost 100 mA. With a nominal supply voltage of 3.3V, the worst-case current consumption is equivalent to a 33Ω load on our LC network. Since the input to our LC network is a power supply, the source impedance is certainly very low. Using 1Ω for the source impedance is a good approximation. This is illustrated in Figure 8.

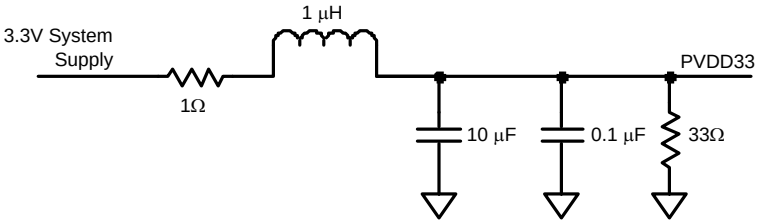

Figure 8. Typical LC Network Circuit

The design goal for this filter network was chosen to be –30 dB at a typical switching power supply frequency of 250 KHz. The response curve is shown in Figure 9.

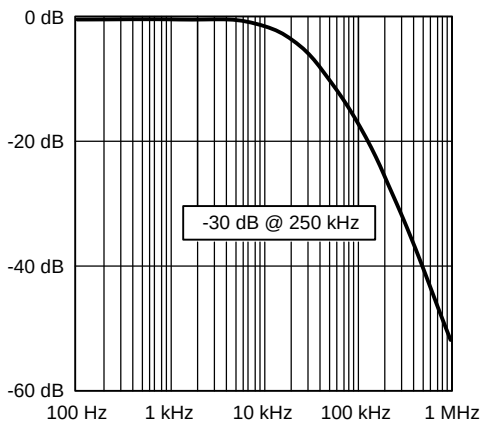

Figure 9. Filter Network Response Curve

Due to the variables in any system design, no single LC filter can be considered optimal. The values selected in this example would likely exceed the filter requirements in most applications. An analysis for specific applications should be taken to ensure this SCAN25100 supply remains noise free.

8 Thermal Recommendations

The exposed GND pad on the TQFP-100 must be connected to GND using a copper land and multiple vias to ensure optimal thermal performance. Thermal vias connect the copper land to internal or external copper planes and should have a drill diameter sufficiently small so that the hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the thermal land on the surface of the board during solder reflow. Generally, a drill diameter of 0.33mm (13 mils) or smaller keeps solder wicking to a minimum.

To assure the optimum thermal transfer through the GND vias to internal planes or the reverse side of the PCB, the vias used in the thermal land should not be thermally relieved. Thermal relief or "Web" construction on PCB vias is a standard technique used in most PCBs today to facilitate soldering, by constructing the via so that it has a high thermal resistance. This is not desirable for heat removal from the TQFP-100 exposed GND package. It is recommended that all vias used under the package make internal connections to the planes using a continuous connection completely around the hole diameter for optimal thermal performance.

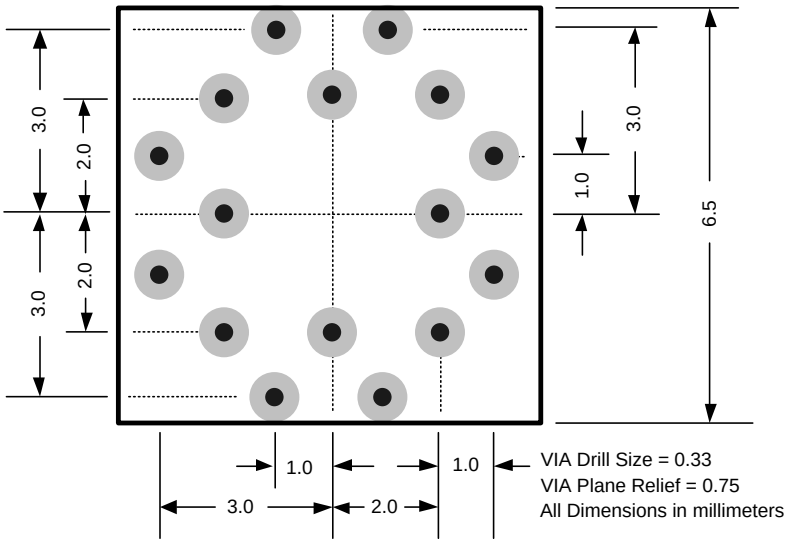

Figure 10. GND Via Placement for Optimal Heat Transfer

In many system designs airflow is routed across heat sinks attached to the bottom of the PCB. In cases like this, an external GND pad on the backside of the board will be needed to achieve the most efficient heat transfer (see Figure 10). This pad should be at least as big as the DAP package connection. The board stackup will also affect how efficiently heat can be transferred from the TQFP-100 package.

Keeping the distance from the TOP and/or BOTTOM of the board to the GND plane is essential to good thermal conductivity. This minimizes the effective length and thermal resistance of the GND vias, maximizing the heat transfer to the PCB. In some cases two SCAN25100 devices will be mounted back to back to save PCB space. In this type of layout it is important that the PCB stackup has at least 2 GND planes so each SCAN25100 has its own primary GND plane for thermal dissipation. With only a single GND plane, package thermal performance will be impacted due to the combined power dissipation of two SCAN25100 devices connected to a common heat sink.

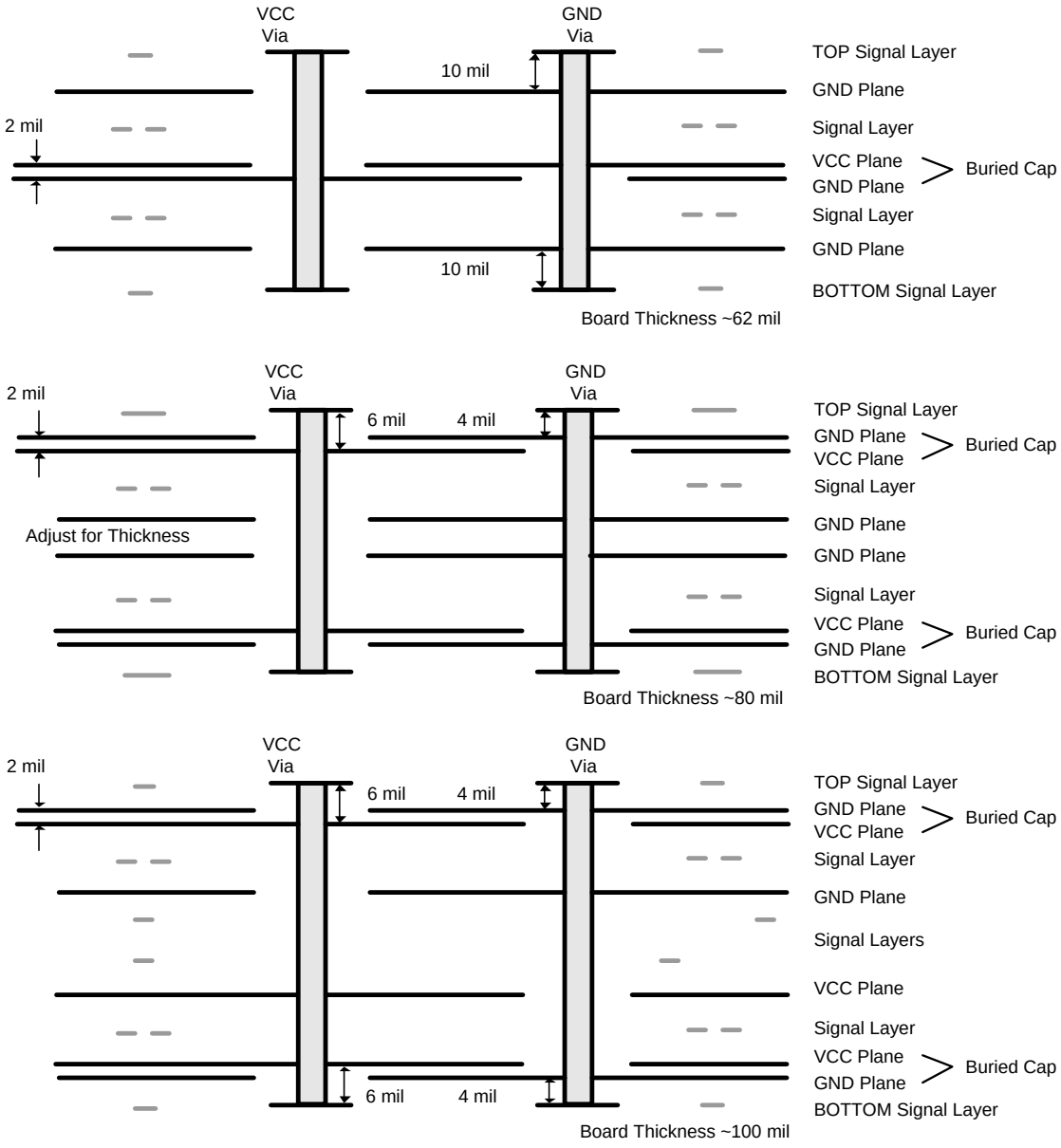

Figure 11. PCB Stackup

In this type of layout it is important that the PCB stackup (see Figure 11) has at least two GND planes so each SCAN25100 has its own primary GND plane for thermal dissipation. With only a single GND plane, package thermal performance will be impacted due to the combined power dissipation of two SCAN25100 devices connected to a common heat sink.

In all PCB stack-up designs shown there is at least one VCC-GND pair specified with the minimum manufacturing dielectric thickness. At the minimum spacing the planes create a very low inductance parallel plate capacitor for high frequency decoupling.

The SCAN25100 device is centered above the 6.5 mm DAP connection inside the TQFP-100 package. Therefore heat from the SCAN25100 will also be centered within the DAP area, as illustrated in Figure 12.

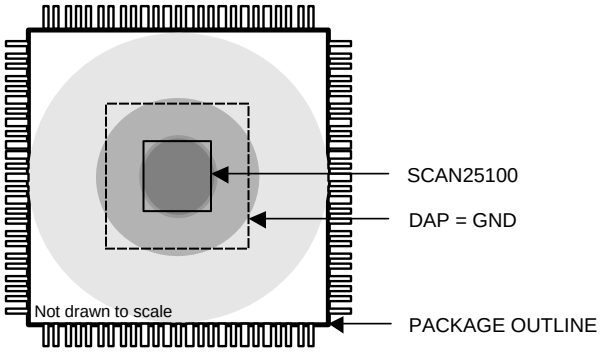

Figure 12. TQFP-100 Temperature Profile

It is not recommended to add more then 16 vias under the DAP area. Increasing the via count further will not significantly improve the SCAN25100 thermal performance. The vias must also cut through the power planes. Too many local via reliefs in the power plane will reduce the plane-to-plane decoupling capacitance and increase plane inductance in this critical supply area under the SCAN25100 component.

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