

AN-1957 LVDS Signal Conditioners Reduce Data-Dependent Jitter

ABSTRACT

Jitter is a phenomenon troubling many designers of high-speed interfaces. It reduces available timing margin, limits transmission distance between a transmitter and a receiver, and increases system cost by demanding better performing and more expensive interconnects. LVDS interfaces are not spared from these ill effects as they now operate at bit rates exceeding the 3 Gbps mark. Texas Instruments LVDS signal conditions can be used to significantly reduce data-dependant jitter.

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1 Introduction

Texas Instruments has developed a family of LVDS signal conditioners that mitigates transmission line losses, reduces data-dependent jitter and maximizes noise margin. Optimal use of these devices not only requires understanding of their fundamental principles of operation but also basic comprehension of jitter and its types.

The aim of this application report is to assist those looking to improve timing and noise margins in their high-speed links with the use of signal conditioners. The document first discusses jitter, its categories and causes, then it overviews the LVDS signal conditioners and explains how they compensate for transmission line losses. It then presents experimental results showing jitter accumulation as a function of FR-4 stripline length and jitter reductions that can be realized with the use of LVDS signal conditioners.

2 What is Jitter?

Jitter is fundamentally defined as a short-term deviation of a digital signal's active edge or a transition from its ideal position in time. Test and measurement industry classifies it into two categories: random and deterministic jitter. These two components constitute what is typically referred to as total jitter (TJ). Deterministic jitter may be further subdivided into periodic, data-dependent and duty-cycle dependent jitter. [Figure 1](#) illustrates a hierarchy of different jitter types.

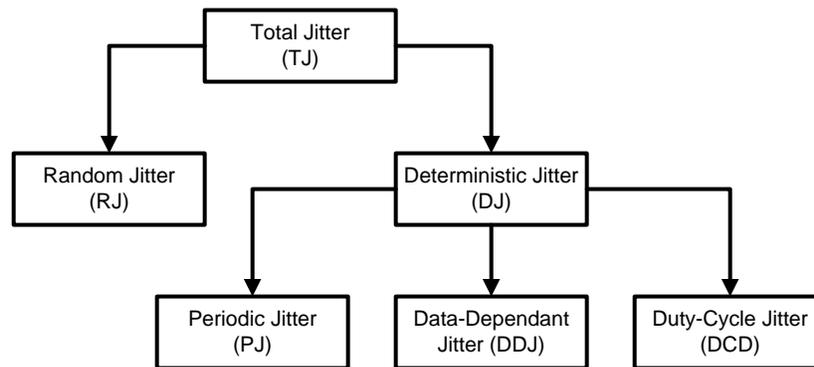


Figure 1. Jitter Categories

Random jitter (RJ) is mostly caused by thermal noise. It is assumed to have a Gaussian distribution and as such is quantified using standard deviation (RMS – root mean square) of the distribution. Peak-to-peak value of random jitter is also helpful when predicting the total jitter of a link. However, due to the unbounded nature of a Gaussian distribution (its tails approach infinity), peak-to-peak value of the RJ can only be estimated given the desired bit error rate (BER). [Table 1](#) lists coefficients that can be used to estimate the RJ (p-p) for a given BER and RJ (RMS). For example, the coefficient used to calculate the probability of exceeding the RJ (p-p) at 10⁻¹² is 14.1. If a value of 1.2 ps (RMS) is measured, the peak-to-peak value is 14.1 * 1.2 ps = 16.92 ps.

Table 1. RJ (p-p) as a Function of Bit Error Rate (BER)

BER	RJ (p-p)
10 ⁻¹⁰	12.7 * RJ (RMS)
10 ⁻¹¹	13.4 * RJ (RMS)
10 ⁻¹²	14.1 * RJ (RMS)
10 ⁻¹³	14.7 * RJ (RMS)
10 ⁻¹⁴	15.3 * RJ (RMS)
10 ⁻¹⁵	15.9 * RJ (RMS)
10 ⁻¹⁶	16.4 * RJ (RMS)

LVDS signal conditioners add very small amounts of random jitter to a signal when inserted into the signal's path. The random jitter contribution (tRJ) of an LVDS signal conditioner is specified in the device-specific data sheet as an RMS value and is typically less than 1 ps rms. When two or more random jitter sources are added in the signal path, their random jitter contributions are summed geometrically. Furthermore, random jitter is the type of jitter LVDS signal conditioners cannot eliminate or minimize. If random jitter is excessive, other means of jitter cleaning may be needed (for example, use of retimers).

Deterministic jitter (DJ) is the type of jitter that is bounded (has a finite peak-to-peak value), repeatable and predictable. It may be caused by power supply switching, interconnect losses, reflections and filtering. Based on these different jitter causes, the deterministic jitter is further classified into the three categories as shown in Figure 1. LVDS signal conditioners add small amounts of deterministic jitter to a signal when inserted into the signal's path. The deterministic jitter contribution (tDJ) of an LVDS signal conditioner is specified in its data sheet as a peak-to-peak value. The units for deterministic jitter can be either seconds (ps) or unit intervals (UI). One unit interval has duration of one bit. For example, 1 UI of a 1 Gbps signal has duration of 1ns. If the 1 Gbps signal has DJ of 100 ps, one can also state that the DJ is 0.1 UI. When two or more deterministic jitter sources are added in the signal path (signal repeaters), their deterministic jitter contributions are added algebraically. Unlike random jitter, deterministic jitter can be minimized by LVDS signal conditioners.

Periodic or sinusoidal jitter (PJ) it typically caused by low frequency power supply switching noise or similar noise sources asynchronous to the bit stream affected. LVDS signal conditioners don't cause any periodic jitter when inserted in the signal path.

Duty-cycle dependent jitter (DCD) is a direct result of duty-cycle distortion. Duty-cycle distortion can be caused by differences between signal's rising and falling transition times and receiver threshold offsets. LVDS signal conditioners cause minimal DCD jitter when inserted in the signal path as they output very symmetric waveforms and have receivers with tight input voltage thresholds. Both PJ and DCD are jitter types that cannot be fixed by LVDS signal conditioners.

Data-dependent jitter (DDJ) or ISI jitter (jitter caused by inter-symbol interference) is the type of jitter caused by cables, printed circuit board (PCB) traces or any other passive channels with frequency responses resembling a response of a low pass filter. Figure 2 illustrates a 50-bit long 2.5 Gbps pseudo-random bit stream (PRBS-7) after it has passed through a lossy channel (a 30" FR-4 stripline). It displays the following bits (each occupying approximately 400 ps) starting from the left: '1011010001000110011010101000000011111011111001111'. As it can be seen from Figure 2, the '010101" segment has bits with significantly lower amplitudes or V_{OH} and V_{OL} levels than the amplitudes of bits in the subsequent '0000000111111' segment. This is the result of the lossy channel attenuating the bit stream's higher frequency components (found in the '010101" segment) more than the bit stream's lower frequency components (found in the '0000000111111' segment).

Varying V_{OH} and V_{OL} levels result in data-dependent jitter as well as in reduction of vertical noise margin. These phenomena are best observed using an eye diagram as illustrated in Figure 3. Figure 3 shows a 2.5 Gbps PRBS-7 after a 30" FR-4 stripline. As it can be seen, lossy channels cause data-dependent jitter, reduce noise margin, and increase likelihood of bit errors. Data-dependent jitter is the dominant jitter type in high-speed links containing long and lossy interconnects. Fortunately, the DDJ is the type of jitter that LVDS signal conditioner can reduce. The following sections introduce LVDS signal conditioners and the jitter reducing benefits they bring.

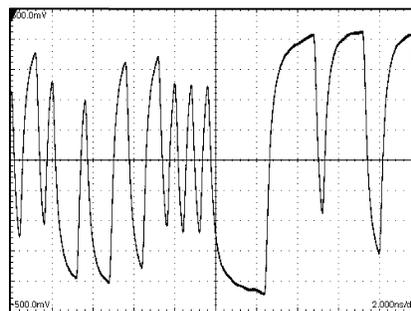


Figure 2. A 50-Bit 2.5 Gbps PRBS-7 After a 30" FR-4 Stripline

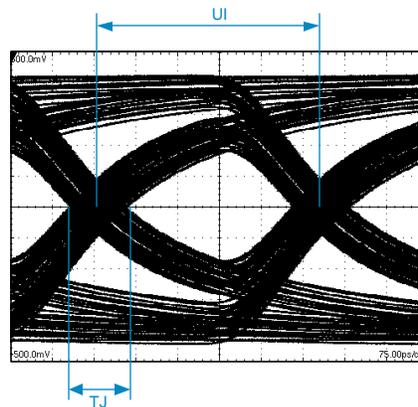


Figure 3. An Eye Diagram of a 2.5 Gbps PRBS-7 After a 30" FR-4 Stripline

3 LVDS Signal Conditioners

As discussed in the earlier section, transmission line losses increase jitter, limit transmission distance or reach and reduce noise margin. In response to a need for devices that mitigate these undesired effects, Texas Instruments has developed a family of LVDS devices with built-in pre-emphasis and equalization circuits or so called LVDS signal conditioners. LVDS signal conditioners are basic building blocks of high-speed interfaces such as buffers, repeaters and crosspoint switches that have built-in pre-emphasis and equalization circuits – circuits that can undo negative effects of transmission lines. Table 2 lists currently available LVDS signal conditioners.

Both, pre-emphasis and equalization circuits compensate for transmission line losses and as a result minimize data-dependent jitter and increase noise margin. Knowing basic principles of their operation is critical when deciding how, when, and where to use them. The following two sections provide an overview of pre-emphasis and equalization circuits and explain how these circuits compensate for transmission line losses.

Table 2. Selected LVDS Devices With Integrated Pre-Emphasis and Equalization Circuits

NSID	Function	Pre-emphasis (PE)	Equalization (EQ)
DS25BR100 DS25BR101	LVDS Buffer / Repeater	0 dB ~6 dB at 1.56 GHz	~4 dB at 1.56 GHz ~8 dB at 1.56 GHz
DS25BR110	LVDS Buffer / Repeater	N/A	0 dB ~4 dB at 1.56 GHz ~8 dB at 1.56 GHz ~16 dB at 1.56 GHz
DS25BR120	LVDS Buffer / Repeater	0 dB ~3 dB at 1.56 GHz ~6 dB at 1.56 GHz ~9 dB at 1.56 GHz	N/A
DS25CP102	LVDS 2x2 Crosspoint Switch	0 dB ~6 dB at 1.56 GHz	0 dB ~4 dB at 1.56 GHz
DS25CP104A DS25CP114	LVDS 4x4 Crosspoint Switch	0 dB ~3 dB at 1.56 GHz ~6 dB at 1.56 GHz ~9 dB at 1.56 GHz	0 dB ~4 dB at 1.56 GHz ~8 dB at 1.56 GHz ~16 dB at 1.56 GHz
DS25BR440	LVDS Quad Buffer	0 dB ~6 dB at 1.56 GHz	0 dB ~4 dB at 1.56 GHz
DS25BR204	LVDS 1:4 Repeater	0 dB ~6 dB at 1.56 GHz	0 dB ~4 dB at 1.56 GHz

3.1 Pre-Emphasis

Pre-emphasis circuits boost the magnitudes of high frequency components of a signal with respect to the magnitudes of low frequency components of the signal. In time domain, signals boosted with the pre-emphasis circuits appear as signals with overshoots and undershoots at each transition. To better visualize the “boosted” signals and the benefits of the pre-emphasis circuits, consider a simple test setup shown in [Figure 4](#). The test setup consists of a pattern generator, DS25CP102 evaluation board (DS25CP102EVK), a lossy channel (30” FR-4 stripline) and an oscilloscope. Waveforms acquired at the two test points and two pre-emphasis circuit conditions (OFF and ON) are shown in [Figure 5](#), [Figure 6](#), [Figure 7](#), and [Figure 8](#).

The waveform of [Figure 5](#) is a 2.5 Gbps PRBS-7 signal measured at the output of the DS25CP102 with the pre-emphasis circuit disabled (TP1). After the lossy channel (TP2), the higher frequency components of the signal are attenuated more than the lower frequency components as illustrated in [Figure 6](#).

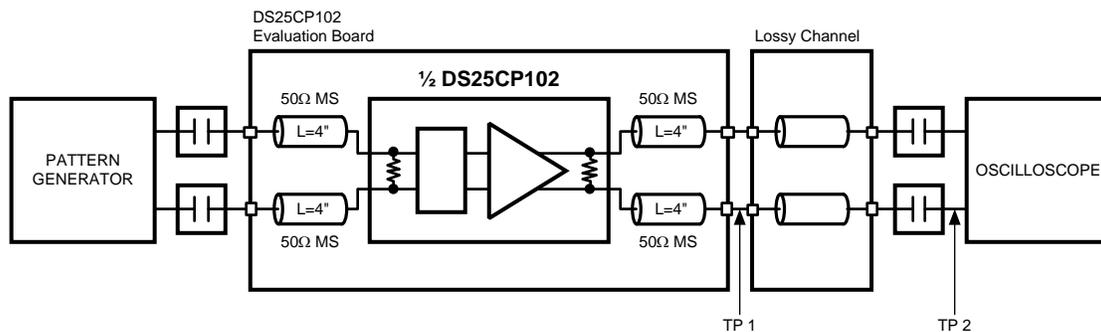


Figure 4. Pre-Emphasis Test Setup

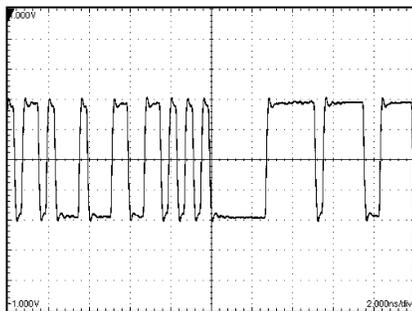


Figure 5. Bit Stream at TP1 with Pre-Emphasis OFF

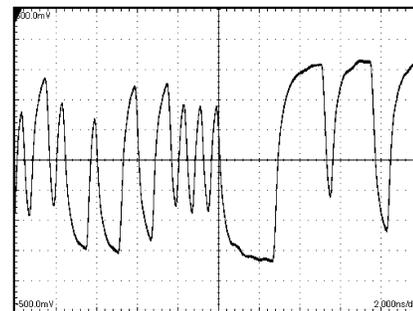


Figure 6. Bit Stream at TP2 with Pre-Emphasis OFF

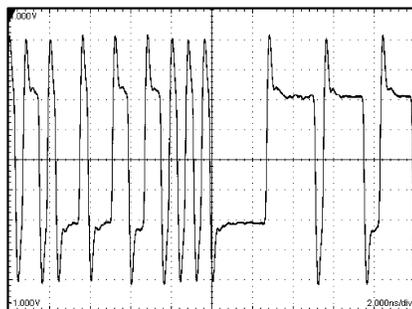


Figure 7. Bit Stream at TP1 with Pre-Emphasis ON

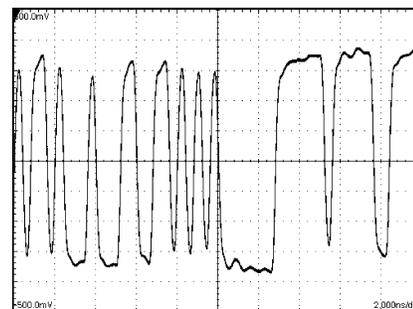


Figure 8. Bit Stream at TP2 with Pre-Emphasis ON

By enabling the pre-emphasis circuit, the signal at the TP1 appears distorted ([Figure 7](#)), however, after the lossy channel (TP2), the signal of [Figure 8](#) looks similar to the undistorted non-attenuated signal of [Figure 5](#). The VOH and VOL level of all bits are close to being equal. It can be said that the levels have been equalized, thus the second name for the pre-emphasis – transmit equalization.

Figure 9, Figure 10, Figure 11, and Figure 12 show the same waveforms of Figure 5, Figure 6, Figure 7, and Figure 8 now in form of eye diagrams. Figure 9 is a low jitter output signal from the DS25CP102 with the pre-emphasis circuit disabled. The lossy channel introduces significant amount of data-dependent jitter and reduces noise margin as shown in Figure 10. The signal at the output of the DS25CP102 with the pre-emphasis circuit enable is distorted at the transmit side (Figure 11), however, at the receive side, after the lossy channel, the eye diagram shows low jitter and maximum noise margin (Figure 12). Clearly, the pre-emphasis circuits significantly reduce data-dependent jitter and increase noise margin.

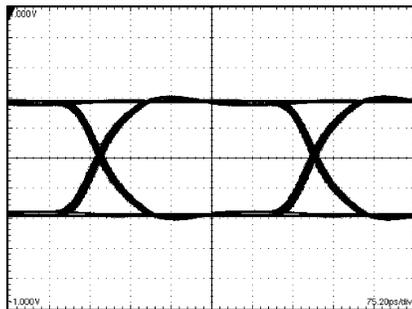


Figure 9. Eye Pattern at TP1 with Pre-Emphasis OFF

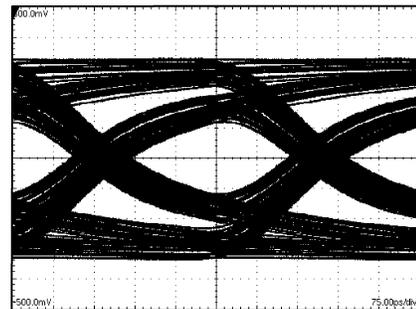


Figure 10. Eye Pattern at TP2 with Pre-Emphasis OFF

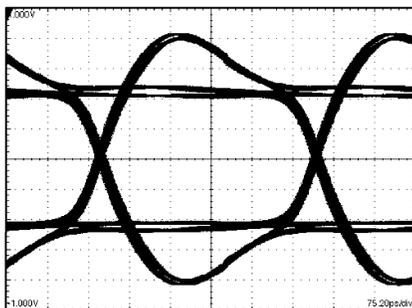


Figure 11. Eye Pattern at TP1 with Pre-Emphasis ON

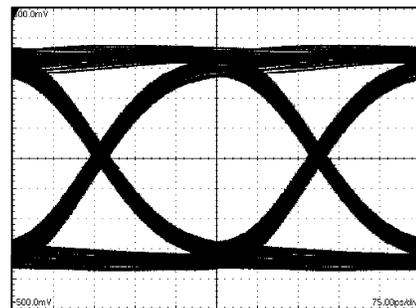


Figure 12. Eye Pattern at TP2 with Pre-Emphasis ON

For system designers, an important parameter of a pre-emphasis circuit is the boost or gain it provides. The higher the boost, the more attenuation the circuit can compensate for and ultimately transmit over a longer transmission medium. As an example, Figure 13 illustrates an output signal from a driver with four pre-emphasis boost levels and the signal's time domain characteristics. The signal is a pattern starting with one bit high (H), followed by one to N bits H, followed by one bit low (L), followed by one to N bits L, followed by an H and an L. Note the signal's nominal amplitude of VOD_L and three distinct boost amplitudes (VOD_H1-3). The boost is simply 20 times log of the ratio of the VOD_H and VOD_L expressed in dB. It is also important to note that the duration of the boost pulse (tVOD_H) should optimally be about 75% of the unit interval (tUI); shorter boost pulse duration will provide lower gain. LVDS signal conditioners from Table 2 feature pre-emphasis circuits that provide up to four pre-emphasis levels.

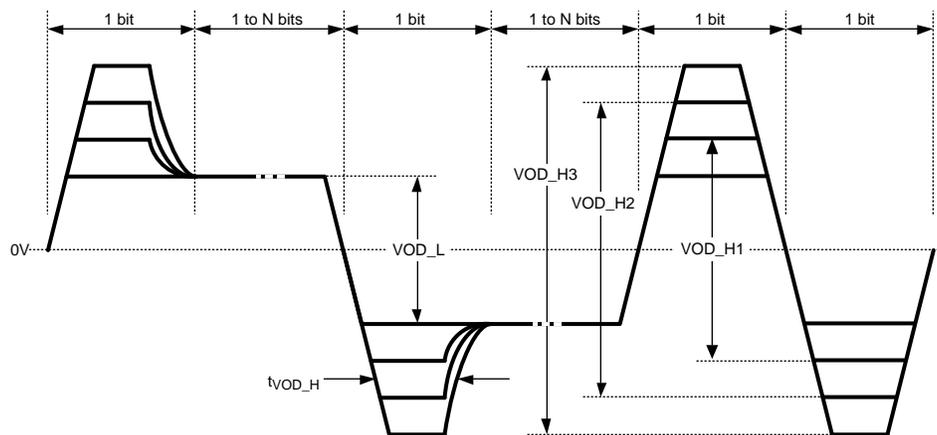


Figure 13. Pre-Emphasis Circuit is Most Useful When the Boost Pulse Duration (t_{VOD_H}) is About 75% of the UI

3.2 Equalization

Equalizers are typically devices with integrated peaking filters whose frequency response curve from the center frequency, f_C , to some lower frequency on the left from the f_C is closely matched to the inverse of the transmission medium's frequency response. As an example, [Figure 14](#) shows a frequency response of a peaking filter with a center frequency at 1 GHz and an inverse of a lossy channel response. Both responses are closely matched up to about 600 MHz. At this frequency, the equalization gain is approximately 6 dB.

Equalizers can be fixed, variable or adaptive. Fixed equalizers have fixed frequency response and may be employed in applications where transmission media have known fixed length. Variable equalizers may have several equalization boost settings, providing more flexibility with the interconnect length. The most flexible are adaptive equalizers that automatically determine the transmission media loss and apply optimal equalization boost.

LVDS signal conditioners listed in [Table 2](#) feature variable equalizers that provide up to four equalization levels.

When compared to pre-emphasis drivers, equalizers are less noisy as they don't require boosting of the signal amplitude, so an equalizer may be the preferred choice for EMI sensitive applications. On the other hand, equalizers have to deal with attenuated signals that bring lower signal-to-noise ratio (SNR). With lower SNR, extra caution is recommended to keep the SNR at desired levels.

To better visualize the benefits of the equalization circuits, consider a simple test setup shown in [Figure 15](#). The test setup consists of a pattern generator, DS25CP104A evaluation board (DS25CP104EVK), a lossy channel (63" FR-4 stripline) and an oscilloscope. Waveforms acquired at the three test points are shown in [Figure 16](#) through [Figure 21](#).

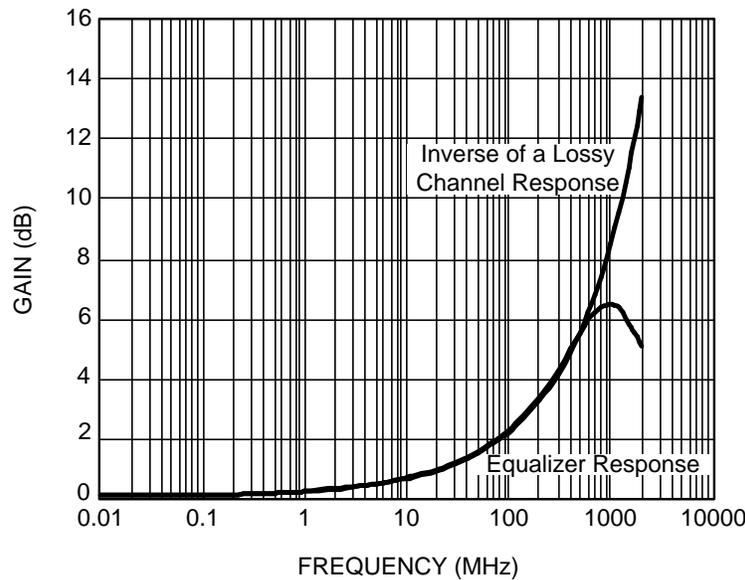


Figure 14. Response of a Peaking Equalizer With the Center Frequency at 1 GHz Closely Matches the Inverse of a Lossy Channel Response

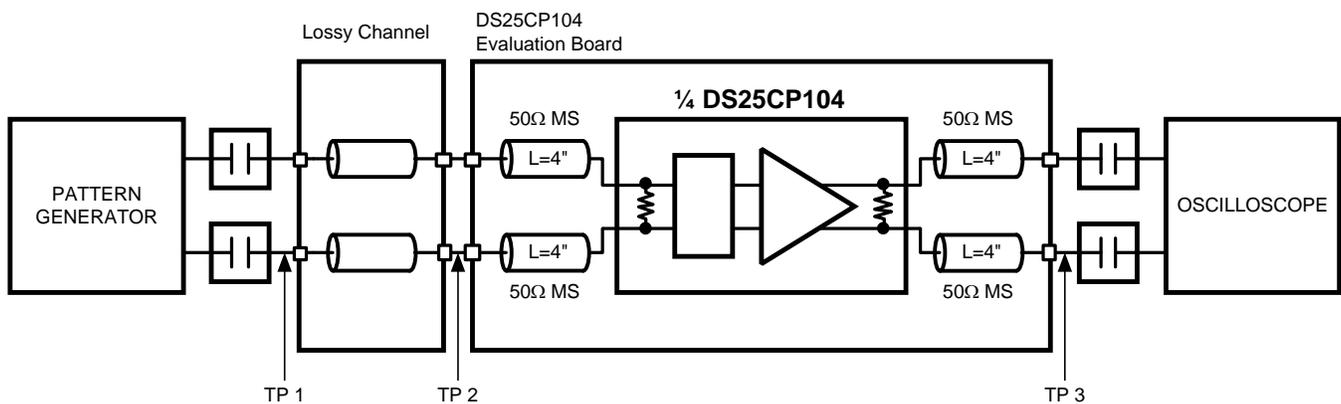


Figure 15. Equalization Test Setup

The waveform of Figure 16 is a 2.5 Gbps PRBS-7 signal measured at the output of the pattern generator (TP1). Figure 17 is the same waveform displayed as an eye diagram. After the lossy channel (TP2), the signal is severely attenuated with its higher frequency components more attenuated than its lower frequency components as illustrated in Figure 18. Figure 19 shows the same signal in form of an eye diagram. The eye diagram is fully closed and the noise margin is non-existent. An LVDS receiver without an equalizer and/or a CDR circuit cannot recover error free data from such an attenuated bit stream.

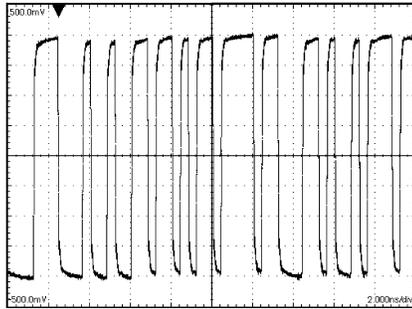


Figure 16. Pattern Generator Output, Bit Stream, TP1

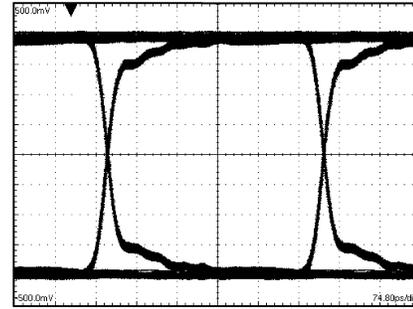


Figure 17. Pattern Generator Output, Eye Pattern, TP1

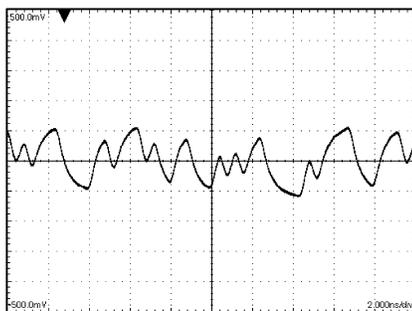


Figure 18. Lossy Channel Output, Bit Stream, TP2

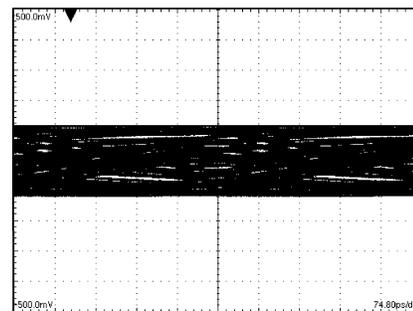


Figure 19. Lossy Channel Output, Eye Pattern, TP2

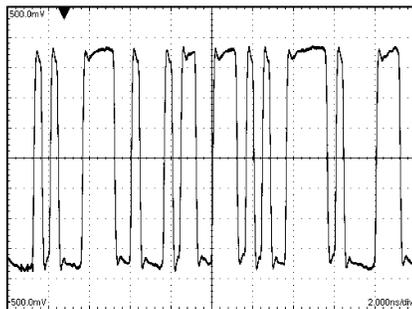


Figure 20. Signal Conditioned Output, Bit Stream, TP3

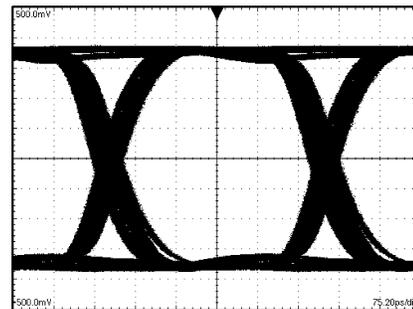


Figure 21. Signal Conditioned Output, Eye Pattern, TP3

Figure 20 and Figure 21 show the waveform after it has been equalized. The high gain equalizer in the DS25CP104A is able to undo the attenuation of the lossy channel and as a result minimize data-dependent jitter and restore noise margin.

4 Jitter Experiment

The experiment consists of three segments:

- The goal of the first segment of the experiment is to collect data showing data-dependent jitter accumulation as a function of FR-4 stripline length and bit rate
- The goal of the second segment of the experiment is to acquire data showing DDJ reductions possible with the use of devices with built-in pre-emphasis circuits (DS25BR120).
- Similarly, the goal of the third segment is to obtain the data showing jitter reducing benefits of the devices with built-in equalizer circuits (DS25BR110).

For all experiment segments, FR-4 striplines of several different lengths are used. In each segment of the experiment, data-dependent jitter is measured at specified test points using Tektronix TDS6154C Digital Storage Oscilloscope with TDSJIT3 jitter analysis application. Advantest D3186 serves as a low jitter pattern generator.

5 FR-4 Striplines

For this experiment, several lossy channels, featuring FR-4 striplines of various lengths (see Table 3), were developed. Each lossy channel consists of an edge coupled 100-ohm differential stripline, two pairs of SMA connectors for interfacing with the instrumentation and the same number of short, one inch long, single-ended 50-Ω microstrips serving as breakout traces between the connectors and tightly coupled differential striplines. Figure 22 shows the block diagram of a lossy channel.

The lossy channels were fabricated with Polyclad PCL-FR-370-Laminate / PCL-FRP-370 Prepreg materials (Dielectric constant of 3.7 and Loss Tangent of 0.02). The edge coupled differential striplines have the following geometries: Trace Width (W) = 5 mils, Gap (S) = 5 mils, Height (B) = 16 mils.

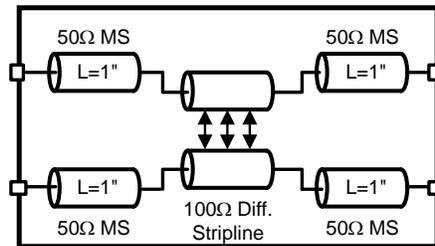


Figure 22. Block Diagram of a Lossy Channel

Table 3. FR-4 Stripline Length and Insertion Loss at 1 GHz

Lossy Channel	Stripline Length [in]	Stripline Length [cm]	Insertion Loss [dB]
SL1	7.5	19	~1.6 dB at 1.00 GHz
SL2	18.5	47	~4.0 dB at 1.00 GHz
SL3	29.5	75	~6.4 dB at 1.00 GHz
SL4	41.0	104	~8.9 dB at 1.00 GHz
SL5	52.0	132	~11.3 dB at 1.00 GHz
SL6	63.0	160	~13.7 dB at 1.00 GHz
SL7	74.0	188	~16.1 dB at 1.00 GHz

Table 3 shows stripline length of each lossy channel as well as their insertion losses at 1 GHz. The insertion loss per length as a function of frequency model is shown in Figure 23. The model was developed by averaging the empirical S-parameter data (SDD21) of each lossy channel. It can be used to determine approximate insertion loss of any lossy channel within the 10 MHz to 6 GHz frequency range.

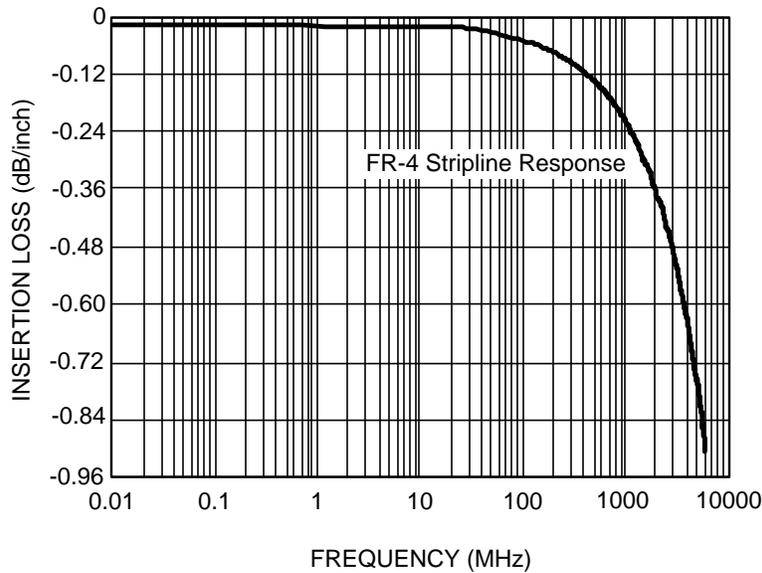


Figure 23. FR-4 Stripline Insertion Loss per Length as a Function of Frequency Model

6 DDJ as a Function of FR-4 Stripline Length

Test setup of Figure 15 is used to gather data-dependent jitter (DDJ) as a function of FR-4 stripline length data and bit rate. The test setup consists of the D3186 pattern generator, DS25BR120 evaluation board (DS25BR100EVK), a lossy channels, DS25BR110 evaluation board and the TDS6154C oscilloscope.

The DS25BR120 has its pre-emphasis circuit disabled and it only serves to set proper LVDS voltage levels and typical LVDS slew rate. The DS25BR110 has its equalizer disabled and it only serves to restore the signal amplitude needed for correct TDSJIT3 jitter analysis software operation. The pattern generator simulates PRBS-7. The jitter is measured with the oscilloscope and separated into all jitter components / types using the jitter analysis software. The bit rate is varied from 250 Mbps to 3250 Mbps in 250 Mbps steps. The DDJ exceeding 0.5 UI is not recorded as the instrumentation and the jitter analysis software is unable to measure / compute the jitter and its components beyond that point. Figure 25 shows the test results.

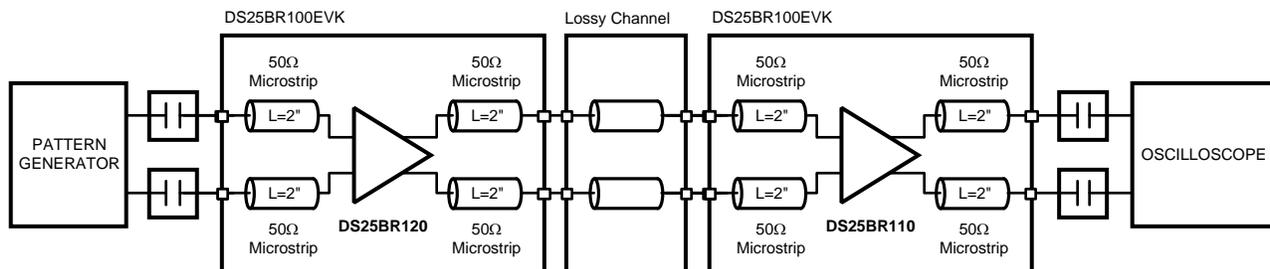


Figure 24. Experiment Setup

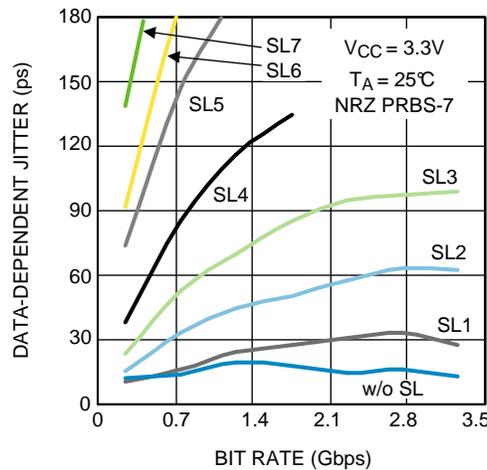


Figure 25. Data-dependent Jitter as a Function of Bit Rate and FR-4 Stripline Length

As expected, the DDJ dramatically increases with higher bit rates and longer FR-4 striplines. The lossy channels with FR-4 striplines longer than 30 inches (SL4, SL5, SL6 and SL7) introduce more than 0.5 UI of DDJ below 2 Gbps point. Other jitter components (RJ, DCD, PJ) have insignificant dependence on the bit rate and the FR-4 stripline length, so the results showing these jitter components are not reported in this application report. The following two subsections present data that shows DDJ reductions that can be realized with the use of LVDS signal conditioners.

7 DDJ Reductions With Pre-Emphasis

As reported in [Section 4](#), the long FR-4 striplines cause significant amounts of data-dependent jitter. It was also confirmed that the increase in the DDJ is proportional to the bit rate. This section reports the data showing DDJ reductions that can be realized with the use of LVDS signal conditioners featuring integrated pre-emphasis circuits.

The experiment setup as shown in [Figure 15](#) is used to gather jitter as a function of FR-4 stripline length, bit rate, and pre-emphasis level data. In this experiment, the DS25BR120 serves as an LVDS signal conditioner featuring four pre-emphasis levels. The DS25BR110 has its equalizer disabled and it only serves to restore the signal amplitude needed for correct TDSJIT3 operation. The pattern generator simulates PRBS-7. The jitter is measured with the oscilloscope and separated into all jitter components / types using the jitter analysis software. The bit rate is varied from 250 Mbps to 3250 Mbps in 250 Mbps steps. For each bit rate step and FR-4 stripline length, all four pre-emphasis levels are exercised and measured DDJ recorded. The DDJ exceeding 0.5 UI is not recorded due to the instrumentation limitations explained earlier. [Figure 26](#) through [Figure 41](#) show the DDJ as a function of bit rate and pre-emphasis level data for all seven FR-4 stripline lengths as well as the case without the lossy channel.

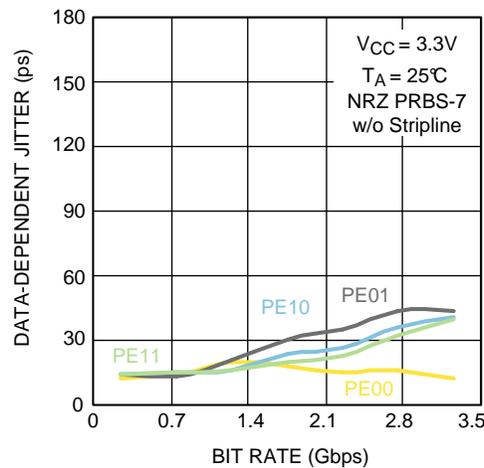


Figure 26. Without Stripline: DDJ as a Function of Bit Rate and Pre-Emphasis Level

When a channel has a minimal loss, as is the case with the setup without the lossy channel, enabling the pre-emphasis circuit results in an increase in DDJ. However, increase in the DDJ caused by the DS25BR120 pre-emphasis circuitry is relatively minor. This is an indicator of a well optimized pre-emphasis circuit.

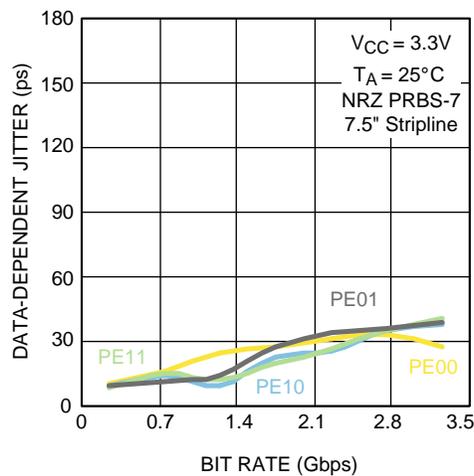


Figure 27. 7.5" Stripline: DDJ as a Function of Bit Rate and Pre-Emphasis Level

The lossy channel with 7.5" stripline does not introduce significant amounts of DDJ to warrant the use of pre-emphasis circuits.

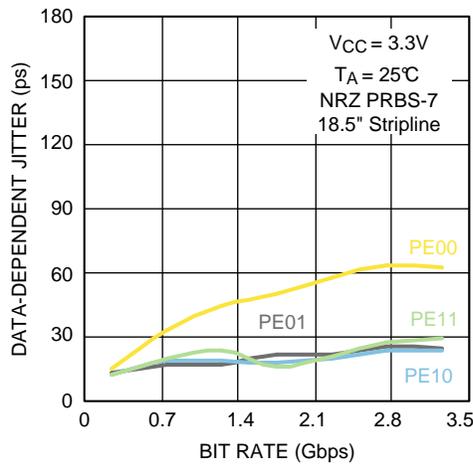


Figure 28. 18.5" Stripline: DDJ as a Function of Bit Rate and Pre-Emphasis Level

With the lossy channel featuring 18.5" stripline, an increase in DDJ can be observed as well as its reduction enabled with the use of the pre-emphasis. Above 1.5 Gbps, the reduction of DDJ is about 50%. The pre-emphasis level PE01 is recommended for the FR-4 stripline lengths around 10 to 20 inches.

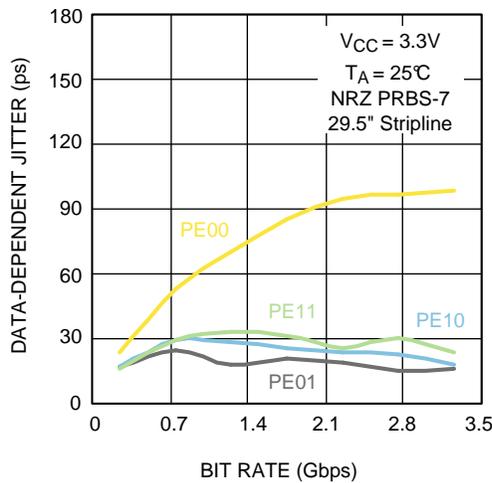


Figure 29. 29.5" Stripline: DDJ as a Function of Bit Rate and Pre-Emphasis Level

With the lossy channel featuring 29.5" stripline, a significant increase in DDJ can be observed above 1 Gbps. Above 1.0 Gbps, the reduction of DDJ is considerable. While all pre-emphasis levels provide similar reductions in DDJ, the vertical noise margin is different and highest with the PE11 setting. It is always recommended to check vertical noise margin in addition to the amount of DDJ when determining the optimal pre-emphasis setting.

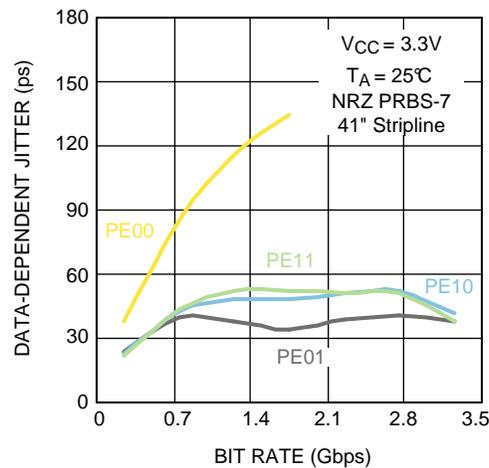


Figure 30. 41" Stripline: DDJ as a Function of Bit Rate and Pre-Emphasis Level

With the lossy channel featuring 41" stripline, the increase of DDJ is significant above 1 Gbps and exceeds 0.5 UI at 1.75 Gbps. Above 1.0 Gbps, the reduction of DDJ is considerable. Again, all pre-emphasis levels provide similar reductions in DDJ, however, highest pre-emphasis setting (PE11) provides the highest the vertical noise margin and is recommended for links in the excess of 30 inches.

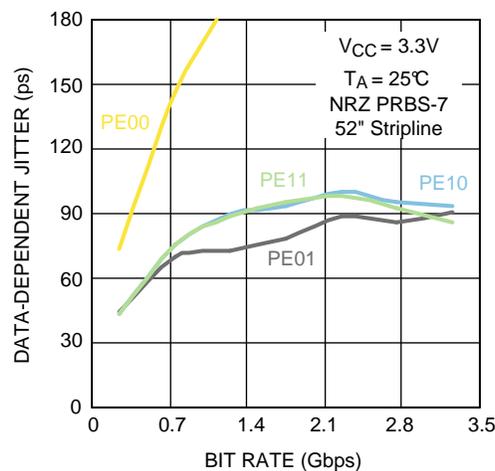


Figure 31. 52" Stripline: DDJ as a Function of Bit Rate and Pre-Emphasis Level

With the lossy channel featuring 52" stripline, the increase of DDJ is significant above 500 Mbps and exceeds 0.5 UI at 1.25 Gbps. Above 500 Mbps, the reduction of DDJ is considerable. Again, the highest pre-emphasis setting is recommended to ensure the maximum noise margin is available.

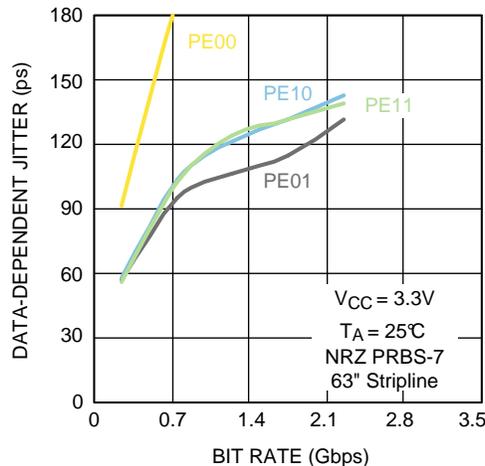


Figure 32. 63" Stripline: DDJ as a Function of Bit Rate and Pre-Emphasis Level

With the lossy channel featuring 63" stripline, the increase of DDJ is significant above 500 Mbps and exceeds 0.5 UI at 1.0 Gbps. Above 500 Mbps, the reduction of DDJ is considerable but it only enables transmission at 2 Gbps or lower bit rates.

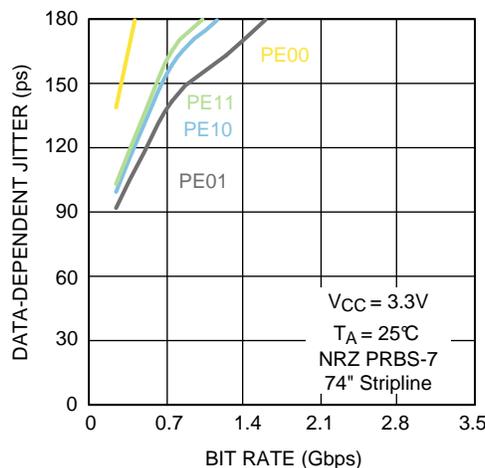


Figure 33. 74" Stripline: DDJ as a Function of Bit Rate and Pre-Emphasis Level

With the lossy channel featuring 74" stripline, the increase of DDJ is enormous and exceeds 0.5 UI already at 500 Mbps. The reduction of DDJ is observed, but it only enables transmission at 1 Gbps or lower bit rates.

8 DDJ Reductions With Equalization

This section reports the data that shows DDJ reductions that can be realized with the use of LVDS signal conditioners with integrated equalizers.

The experiment setup as shown in Figure 15 is used to gather jitter as a function of FR-4 stripline length, bit rate, and equalization level data. In this experiment, the DS25BR120 has its pre-emphasis circuit disabled and it only serves to set proper LVDS voltage levels and typical LVDS slew rate. The DS25BR110 serves as an LVDS signal conditioner with four levels of equalization. It compensates for the FR-4 stripline losses and restores the signal amplitude needed for correct TDSJIT3 operation. The pattern generator simulated PRBS-7. The jitter is measured with the oscilloscope and separated into all jitter

components / types using the jitter analysis software. The bit rate is varied from 250 Mbps to 3250 Mbps in 250 Mbps steps. For each bit rate step and FR-4 stripline length, all four equalization levels are exercised and measured DDJ recorded. The DDJ exceeding 0.5 UI is not recorded due to the instrumentation limitations explained earlier. [Figure 34](#) through [Figure 41](#) show the DDJ as a function of bit rate and equalization level data for all seven FR-4 lengths as well as the case without the lossy channel.

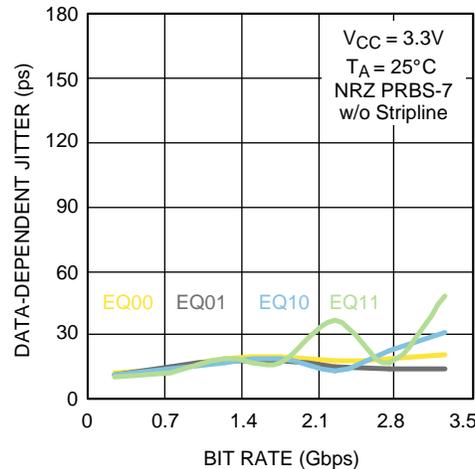


Figure 34. Without Stripline: DDJ as a Function of Bit Rate and Equalization Level

When a channel has a minimal loss, as is the case with the setup without the lossy channel, enabling the equalization circuit results in minimal to no increase in DDJ except the setting with the highest boost (EQ11). The high gain of the EQ11 setting may gain up noise and/or reflections on the signal, so it is recommended to avoid using the highest EQ setting for the lower loss channels.

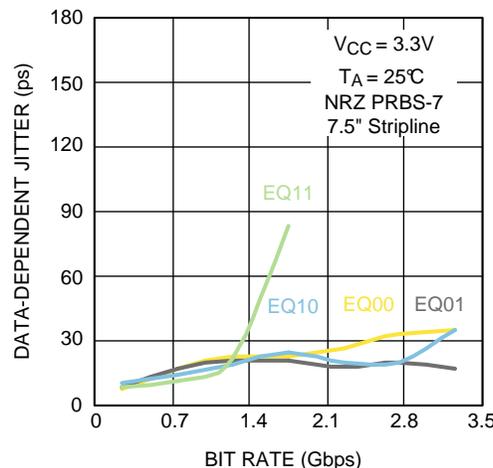


Figure 35. 7.5" Stripline: DDJ as a Function of Bit Rate and Equalization Level

The lossy channel with 7.5" stripline does not introduce significant amounts of DDJ to warrant the use of equalization circuits. The highest gain setting causes undesirable jitter above 1.5 Gbps as it gains up high frequency reflections common to signal transmitted in low loss channels.

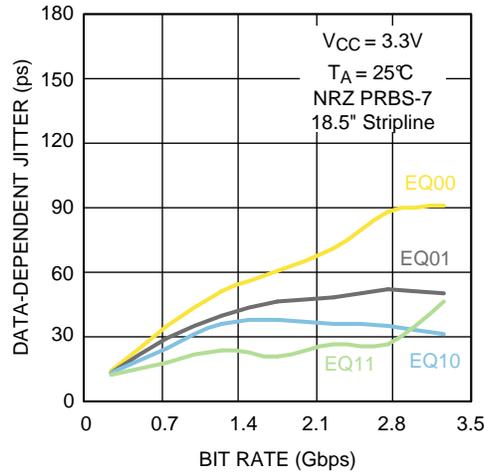


Figure 36. 18.5" Stripline: DDJ as a Function of Bit Rate and Equalization Level

The lossy channel with 18.5" stripline starts to introduce significant amounts of DDJ above 2.5 Gbps. The use of equalization circuits makes notable reductions of DDJ within the 2.5 to 3.25 Gbps range. While the EQ11 setting shows the best performance, the EQ01 or EQ10 setting are recommended to avoid the risk that the high gain equalization setting carries.

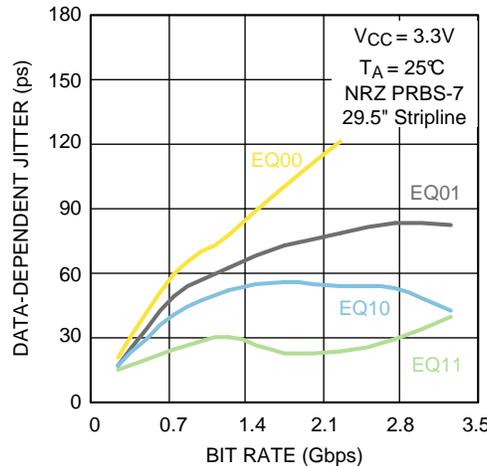


Figure 37. 29.5" Stripline: DDJ as a Function of Bit Rate and Equalization Level

The lossy channel with 29.5" stripline introduces significant amounts of DDJ above 1.5 Gbps. The use of equalization circuits makes notable reductions of DDJ within the 1.5 to 3.25 Gbps range. While the EQ11 setting shows the best performance, the EQ10 setting is recommended to avoid the risk that the high gain equalization setting brings.

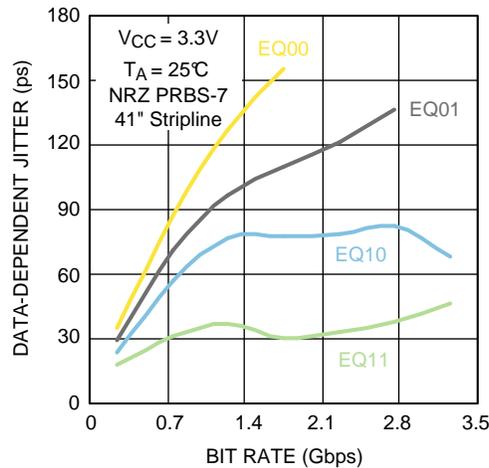


Figure 38. 41" Stripline: DDJ as a Function of Bit Rate and Equalization Level

The lossy channel with 41" stripline introduces significant amounts of DDJ above 1.0 Gbps. The use of equalization circuits makes notable reductions of DDJ within the 1.05 to 3.25 Gbps range. The EQ11 setting is recommended as it provides the highest DDJ reduction. This channel has high attenuation at high frequencies, so any high-frequency noise or reflections are well muted and unlikely pose a threat of being gained up by the highest gain equalization setting.

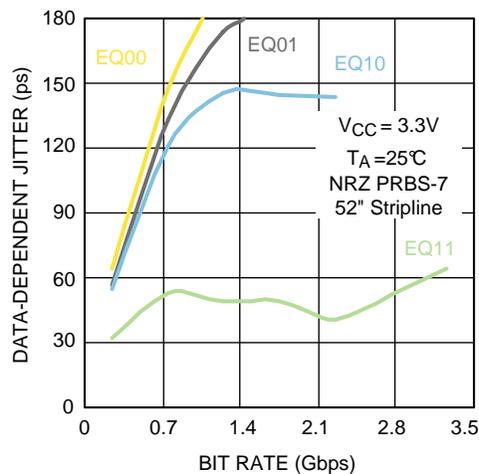


Figure 39. 52" Stripline: DDJ as a Function of Bit Rate and Equalization Level

The lossy channel with 52" stripline introduces significant amounts of DDJ above 500 Mbps. The use of equalization circuits makes notable reductions of DDJ within the 500 Mbps to 3.25 Gbps range. The EQ11 setting is recommended as it provides the highest DDJ reduction.

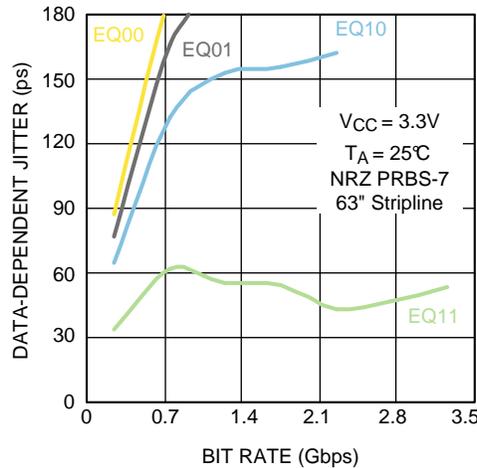


Figure 40. 63" Stripline: DDJ as a Function of Bit Rate and Equalization Level

The lossy channel with 63" stripline introduces significant amounts of DDJ above 500 Mbps. The use of equalization circuits makes notable reductions of DDJ within the 500 Mbps to 3.25 Gbps range. The EQ11 setting is recommended as it provides the highest DDJ reduction.

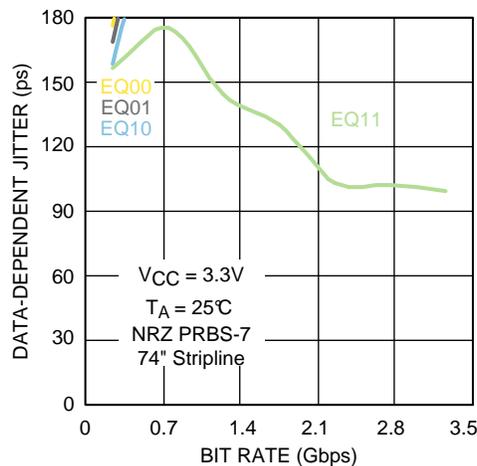


Figure 41. 74" Stripline: DDJ as a Function of Bit Rate and Equalization Level

The lossy channel with 74" stripline introduces significant amounts of DDJ above 500 Mbps. Only the highest equalization setting (EQ11) makes notable reductions of DDJ.

9 Conclusions

Data-dependent jitter is an ill effect of long and lossy PCB traces, cables and any other passive networks with frequency responses resembling the response of a low pass filter. TI's family of LVDS signal conditioners with integrated pre-emphasis and equalization circuits can significantly reduce data-dependent jitter, extend the transmission distance, and increase noise margin.

LVDS signal conditioners with integrated pre-emphasis circuits are ideal for placement on the transmit side of the transmission line. They are optimal for noisier environments while providing up to 9 dB of high-frequency boost.

LVDS signal conditioners with integrated equalization circuits are normally placed at the receive side of a transmission line while providing up to 16 dB of high frequency boost. The equalizers are less noisy as they don't require boosting of the signal's nominal amplitude. They are the preferred choice for EMI sensitive applications. As the equalizers have to deal with much attenuated signals that bring low signal-to-noise ratio (SNR), extra caution is recommended to keep the SNR at desired levels.

10 References

DS25BR110 3.125 Gbps LVDS Buffer with Receive Equalization Data sheet. November 06, 2007

DS25BR120 3.125 Gbps LVDS Buffer with Transmit Pre-emphasis Data sheet. November 06, 2007

Application Note AN-1826 – “Extending the Reach of a FPD-Link II Interface with Cable Drivers and Equalizers”. March 24, 2008

Tektronix Application - “Understanding and Characterizing Timing Jitter”. October 22, 2007

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