User's Guide

SNVA482A–May 2011–Revised April 2013

AN-2147 LM34923 Evaluation Board

1 Introduction

The LM34923 EVAL evaluation board provides the design engineer with a fully functional buck regulator, employing the constant on-time (COT) operating principle. This evaluation board provides a 5V output over an input range of 6V to 75V. The circuit delivers load currents to 500 mA, with current limit set at a nominal 1 Amp.

The board's specification are:

- Input Voltage: 6V to 75V
- Output Voltage: 5V
- Maximum load current: 500 mA
- Minimum load current: 0A
- Current Limit: 1 Amp (nominal)
- Measured Efficiency: 94.75% (V_{IN} = 6V, I_{OUT} = 100 mA)
- Nominal Switching Frequency: 200 kHz
- Size: 2.6 in. x 1.6 in.

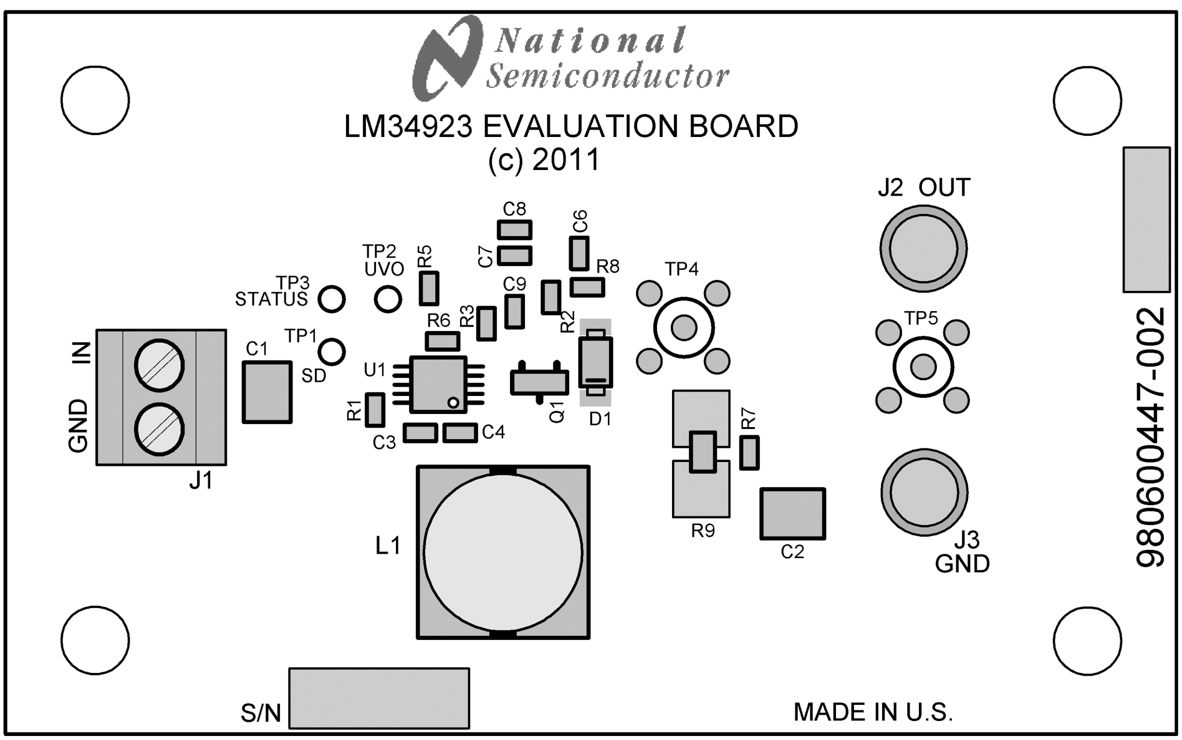

Figure 1. Evaluation Board - Top Side

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2 Theory of Operation

Figure 6 shows the evaluation board schematic. When the circuit is in regulation, the buck switch is on each cycle for a time determined by R1 and VIN according to Equation 1:

$$t_{on} = \frac{1.25 \times 10^{-10} \times (R1 + 500\Omega)}{V_{IN} - 0.5V} + 30\ ns \quad (1)$$

The on-time of this evaluation board ranges from ≅4.38 µs at VIN = 6V, to ≅351 ns at VIN = 75V. The on-time varies inversely with VIN to maintain a nearly constant switching frequency. At the end of each on-time the minimum Off-Timer ensures the buck switch is off for at least 260 ns. In normal operation, the off-time is much longer. During the off-time, the load current is supplied by the output capacitor (C2). When the output voltage falls sufficiently that the voltage at FB is below 2.5V, the regulation comparator initiates a new on-time period. For stable, fixed frequency operation, a minimum of 25 mV of ripple is required at FB to switch the regulation comparator. For a more detailed block diagram, and a complete description of the various functional blocks, see the *LM34923 80-V 600-mA Constant On-Time Buck Switching Regulator Data Sheet* (SNVS695).

3 Board Layout and Probing

The pictorial in Figure 1 shows the placement of the circuit components. The following should be kept in mind when the board is powered:

- When operating at high input voltage and high load current, forced air flow may be necessary.
- The LM34923 may be hot to the touch when operating at high input voltage and high load current.
- Use CAUTION when probing the circuit at high input voltages to prevent injury, as well as possible damage to the circuit.
- At maximum load current, the wire size and length used to connect the load becomes important. Ensure there is not a significant drop in the wires between this evaluation board and the load.

4 Board Connection/Start-up

The input connections are made to the J1 connector. The load is connected to the J2 (OUT) and J3 (GND) terminals. Ensure the wires are adequately sized for the intended load current. Before start-up a voltmeter should be connected to the input terminals, and to the output terminals. The load current should be monitored with an ammeter or a current probe. It is recommended that the input voltage be increased gradually to 6V, at which time the output voltage should be 5V. If the output voltage is correct with 6V at VIN, then increase the input voltage as desired and proceed with evaluating the circuit. DO NOT EXCEED 75V AT VIN.

5 Output Ripple Control

The LM34923 requires a minimum of 25 mVp-p ripple at the FB pin, in phase with the switching waveform at the SW pin, for proper operation. The required ripple can be supplied from ripple at V_{OUT}, through the feedback resistors as described in Section 5.1. Section 5.2 and Section 5.3 provide lower output ripple with one or two additional components.

5.1 Option A) Lowest Cost Configuration

In this configuration R7 is installed in series with the output capacitance (C2). Since ≥25 mVp-p are required at the FB pin, R7 must be chosen to generate ≥50 mVp-p at V_{OUT}, knowing that the minimum ripple current in this circuit is ≅51 mAp-p at minimum V_{IN}. Using 1Ω for R7, the ripple at V_{OUT} ranges from ≅51 mVp-p to ≅280 mVp-p over the input voltage range. If the application can accept this ripple level, this is the most economical solution. The circuit is shown in Figure 2, see Figure 8. R8, C6, C7, and C8 are not used in this configuration.

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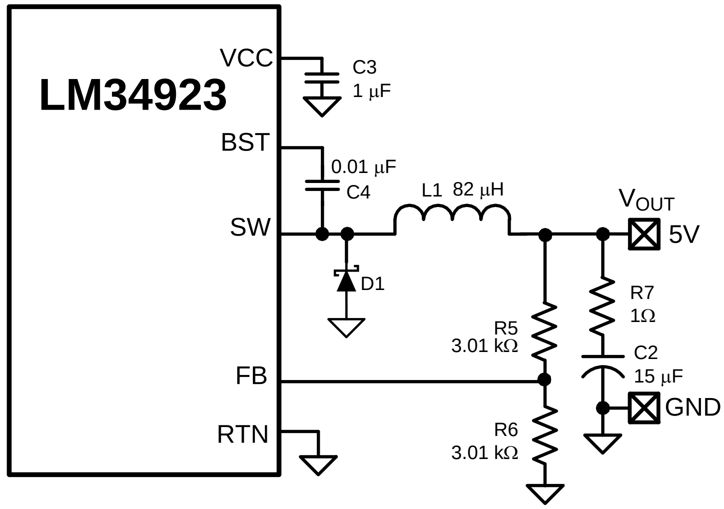

Figure 2. Lowest Cost Configuration

5.2 *Option B) Reduced Ripple Configuration*

This configuration generates less ripple at V_{OUT} than Section 5.1 by the addition of one capacitor (C8) across R5, as shown in Figure 3.

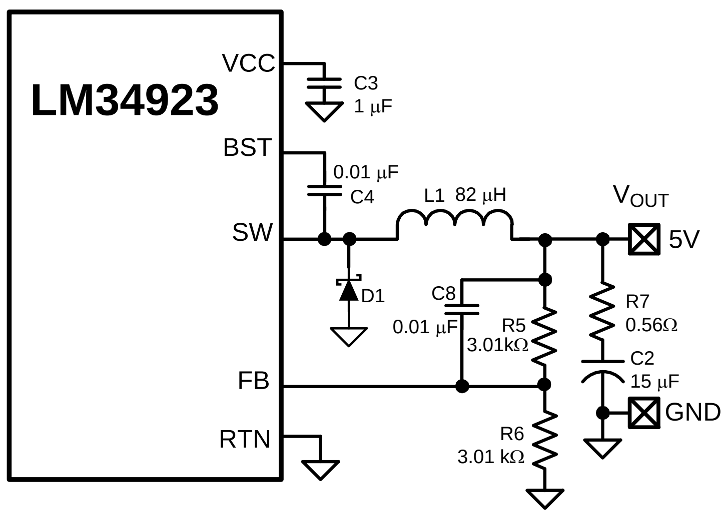

Figure 3. Reduced Ripple Configuration

Since the output ripple is passed by C8 to the FB pin with little or no attenuation, R7 can be reduced so the minimum ripple at V_{OUT} is ≅25 mVp-p. The minimum value for Cff is calculated from:

$$C8 \geq \frac{3 \times t_{ON\ (max)}}{(R5//R6)} \quad (2)$$

where $t_{ON(max)}$ is the maximum on-time (at minimum V_{IN}), and R5//R6 is the parallel equivalent of the feedback resistors. The ripple at V_{OUT} ranges from 28 mVp-p to 159 mVp-p over the input voltage range, see Figure 8.

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5.3 Option C) Minimum Ripple Configuration

To obtain minimum ripple at V_{OUT}, R7 is set to 0Ω, and R8, C6, and C7 are added to generate the required ripple for the FB pin. In this configuration, the output ripple is determined primarily by the characteristics of the output capacitance and the inductor's ripple current, see Figure 8.

The ripple voltage required by the FB pin is generated by R8, and C6 since the SW pin switches from –0.1V to V_{IN}, and the right end of C6 is a virtual ground. The values for R8 and C6 are chosen to generate a 30-100 mVp-p triangle waveform at their junction. That triangle wave is then coupled to the FB pin through C7. The following procedure is used to calculate values for R8, C6 and C7:

1) Calculate the voltage V_A:

$$V_A = V_{OUT} - (V_{SW} \times (1 - (V_{OUT}/V_{IN}))) \quad (3)$$

where V_{SW} is the absolute value of the voltage at the SW pin during the off-time, and V_{IN} is the minimum input voltage. For this circuit, V_A calculates to 4.98V. This is the approximate DC voltage at the R8/C6 junction, and is used in Equation 4.

2) Calculate the R8 x C6 product:

$$R8 \times C6 = \frac{(V_{IN} - V_A) \times t_{ON}}{\Delta V} \quad (4)$$

where, t_{ON} is the maximum on-time, V_{IN} is the minimum input voltage, and ΔV is the desired ripple amplitude at the R8/C6 junction, 40 mVp-p for this example.

$$R8 \times C6 = \frac{(6V - 4.98V) \times 4.38\ \mu s}{0.04} = 1.12 \times 10^{-4} \quad (5)$$

R8 and C6 are then chosen from standard value components to satisfy the above product. Typically, C6 is 3000 to 10000 pF, and R8 is 10 kΩ to 300 kΩ. C7 is chosen large compared to C6, typically 0.1 µF. The ripple at V_{OUT} is typically less than 10 mVp-p, see Figure 4 and Figure 8.

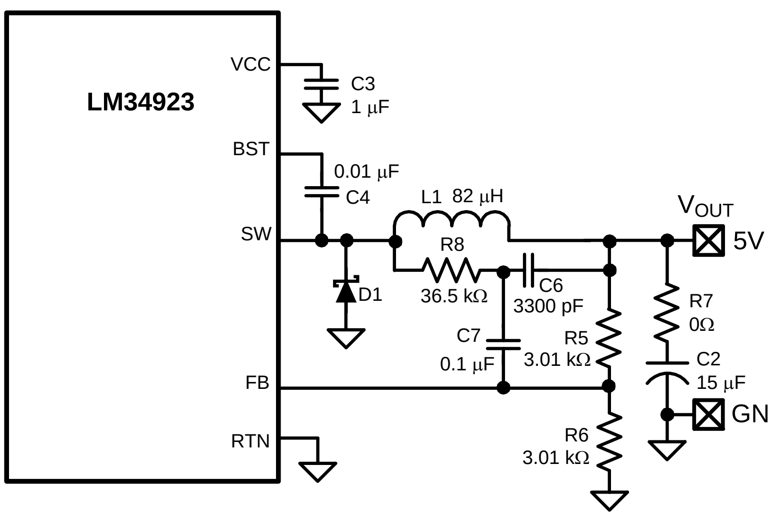

Figure 4. Minimum Output Ripple Configuration

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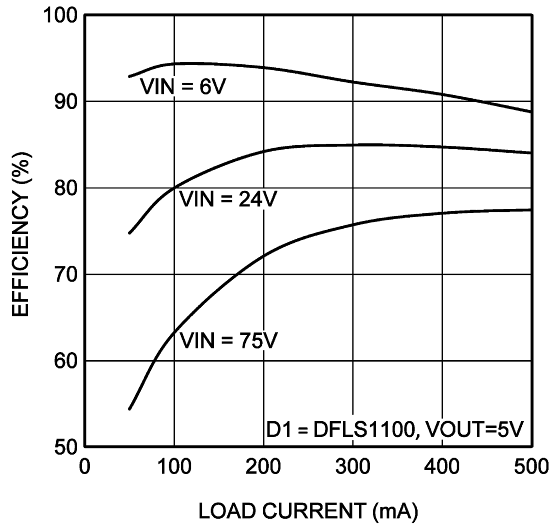

Figure 5. Efficiency at 200 kHz

6 Under-Voltage Detector

The under voltage detector can be used to monitor the input voltage, or any other system voltage as long as the voltage at the UV pin does not exceed its maximum rating. On this evaluation board, the input voltage is monitored via resistors R2 and R3.

An appropriate pull-up voltage less than 10 volts must be connected to test point TP2-UVO on this evaluation board. R4 is the pull-up resistor for the UVO output. The under-voltage status can then be monitored at the TP3-Status test point.

On this evaluation board the UVO output switches low when the input voltage exceeds 12V, and it switches high when the input voltage is less than 11V. If it is desired to change the thresholds, the equations for determining the resistor values are:

$$R2 = \frac{V_{UVH} - V_{UVL}}{5\ \mu A} = \frac{V_{UV(HYS)}}{5\ \mu A} \quad (6)$$

$$R3 = \frac{R2\ \text{x}\ 2.5V}{V_{UVL} - 2.5V} \quad (7)$$

where, V_{UVH} is the upper threshold at VIN, and V_{UVL} is the lower threshold. The threshold at the UV pin is 2.5V.

The UVO output is high when the VCC voltage is below its UVLO threshold, or when the LM34923 is shutdown by grounding the TP1-SD test point, regardless of the voltage at the UV pin.

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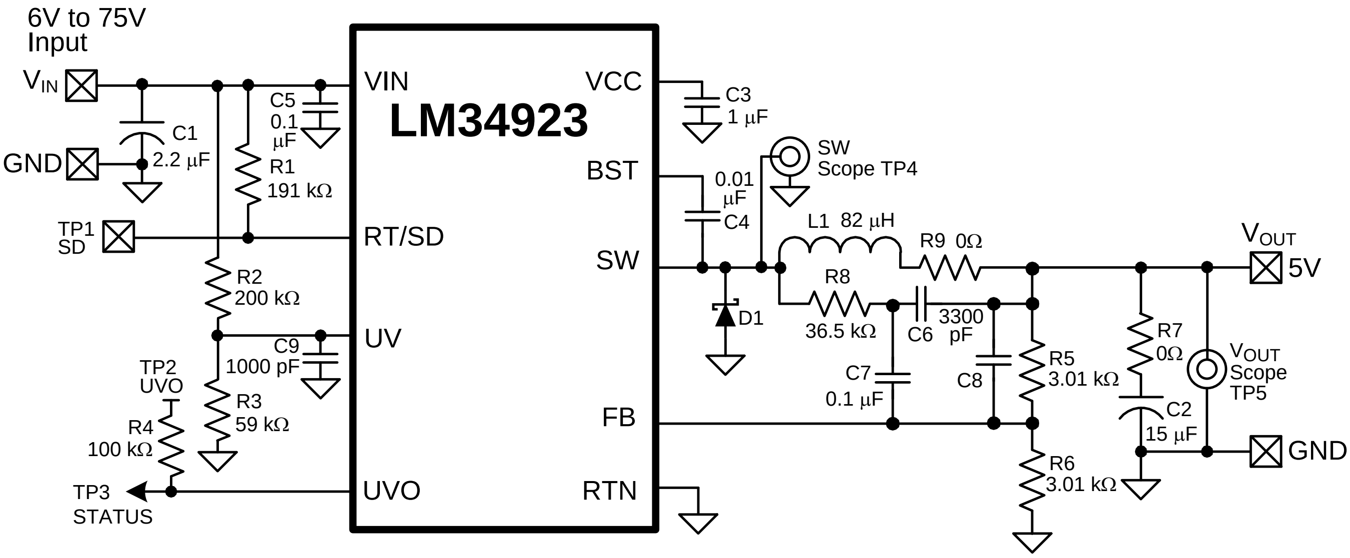

Figure 6. Complete Evaluation Board Schematic (As Supplied)

7 Monitor the Inductor Current

The inductor's current can be monitored or viewed on a scope with a current probe. Remove R9, and install an appropriate current loop across the two large pads where R9 was located. In this way the inductor's ripple current and peak current can be accurately determined.

8 Scope Probe Adapters

Scope probe adapters are provided on this evaluation board for monitoring the waveform at the SW pin, and at the circuit's output (V_{OUT}), without using the probe's ground lead that can pick up noise from the switching waveforms.

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8.1 Bill of Materials (BOM)

Table 1. Bill of Materials (BOM)

Item	Description	Mfg., Part Number	Package	Value
C1	Ceramic Capacitor	TDK C3225X7R2A225M	1210	2.2 µF, 100V
C2	Ceramic Capacitor	TDK C3225X7R1C156M	1210	15 µF, 16V
C3	Ceramic Capacitor	TDK C1608X7R1C105K	0603	1 µF, 16V
C4	Ceramic Capacitor	TDK C1608X7R2A103K	0603	0.01 µF, 100V
C5	Ceramic Capacitor	TDK C2012X7R2A104M	0805	0.1 µF, 100V
C6	Ceramic Capacitor	TDK C1608X7R2A332K	0603	3300 pF, 100V
C7	Ceramic Capacitor	TDK C2012X7R2A104M	0805	0.1 µF, 100V
C8	Unpopulated			
C9	Ceramic Capacitor	TDK C1608X7R2A102K	0805	1000 pF, 100V
L1	Inductor	Coiltronics DR74-820-R or Wurth Electronics 744771182		82 uH,1A
D1	Schottky Rectifier	Diodes Inc DFLS1100	Power DI123	100V, 1.0A
R1	Resistor	Vishay CRCW0603191KF	0603	191kΩ
R2	Resistor	Vishay CRCW0603200KF	0603	200kΩ
R3	Resistor	Vishay CRCW060359KOF	0603	59 kΩ
R4	Resistor	Vishay CRCW0603100KF	0603	100 kΩ
R5	Resistor	Vishay CRCW06033KO1F	0603	3.01 kΩ
R6	Resistor	Vishay CRCW06033KO1F	0603	3.01 kΩ
R7	Resistor	Vishay CRCW06030000Z	0603	0Ω jumper
R8	Resistor	Vishay CRCW060336K5F	0603	36.5 kΩ
R9	Resistor	Vishay CRCW06030000Z	0603	0Ω jumper
U1	Switching Regulator	LM34923	VSSOP-10	

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9 Circuit Performance

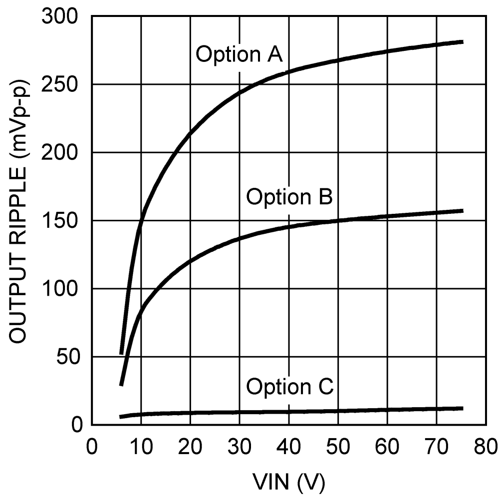

Figure 7. Output Voltage Ripple

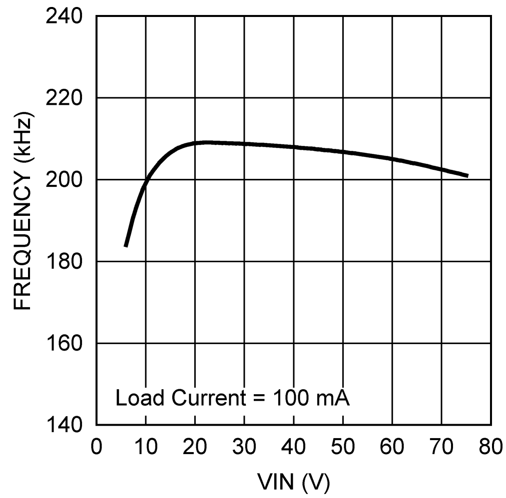

Figure 8. Switching Frequency vs. Input Voltage

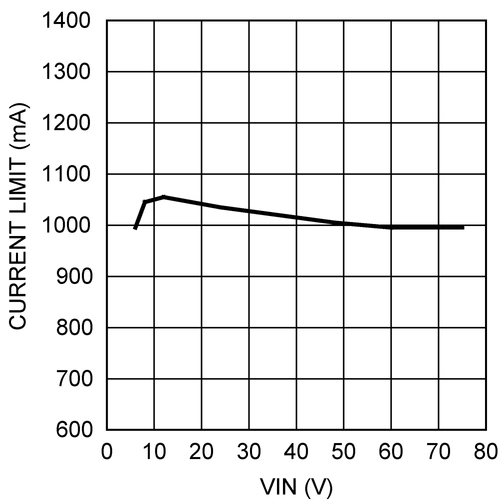

Figure 9. Current Limit vs. Input Voltage

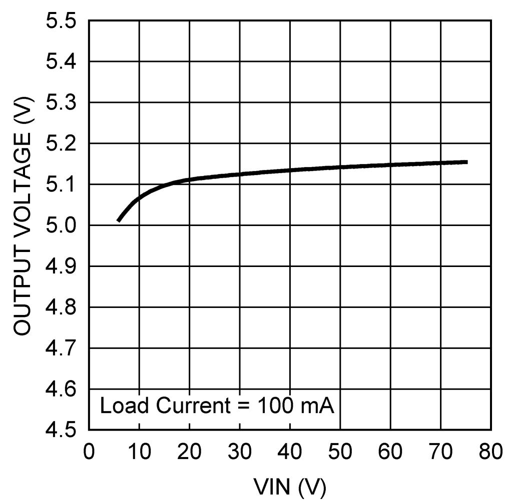

Figure 10. Line Regulation

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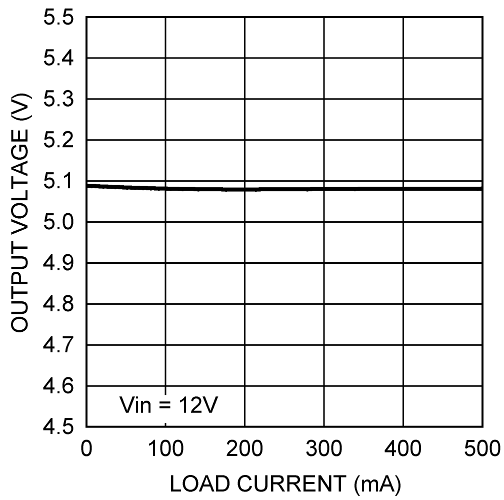
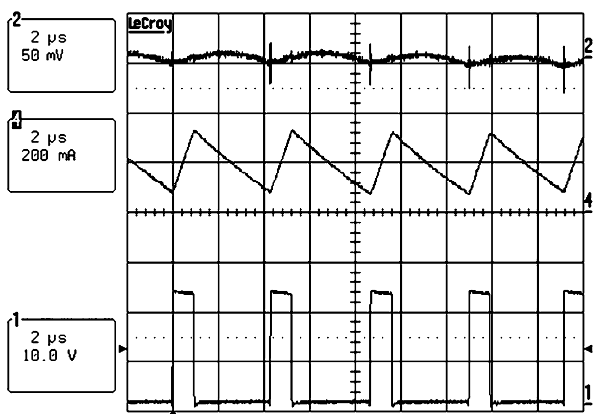


Figure 11. Load Regulation

10 Typical Waveforms



Trace 1 = SW Pin
Trace 2 = V_{OUT}
Trace 4 = Inductor Current
Vin = 12V, Iout = 200 mA

Figure 12. Typical Waveforms

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11 PC Board Layout

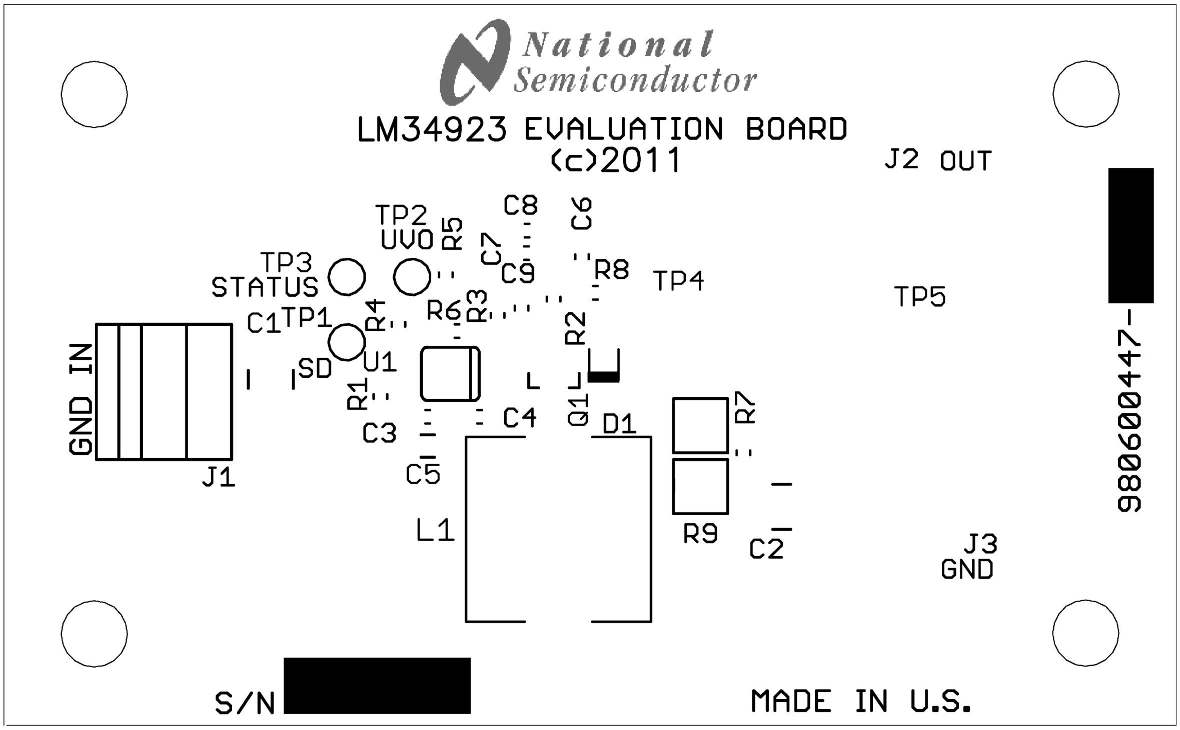

Figure 13. Board Silkscreen

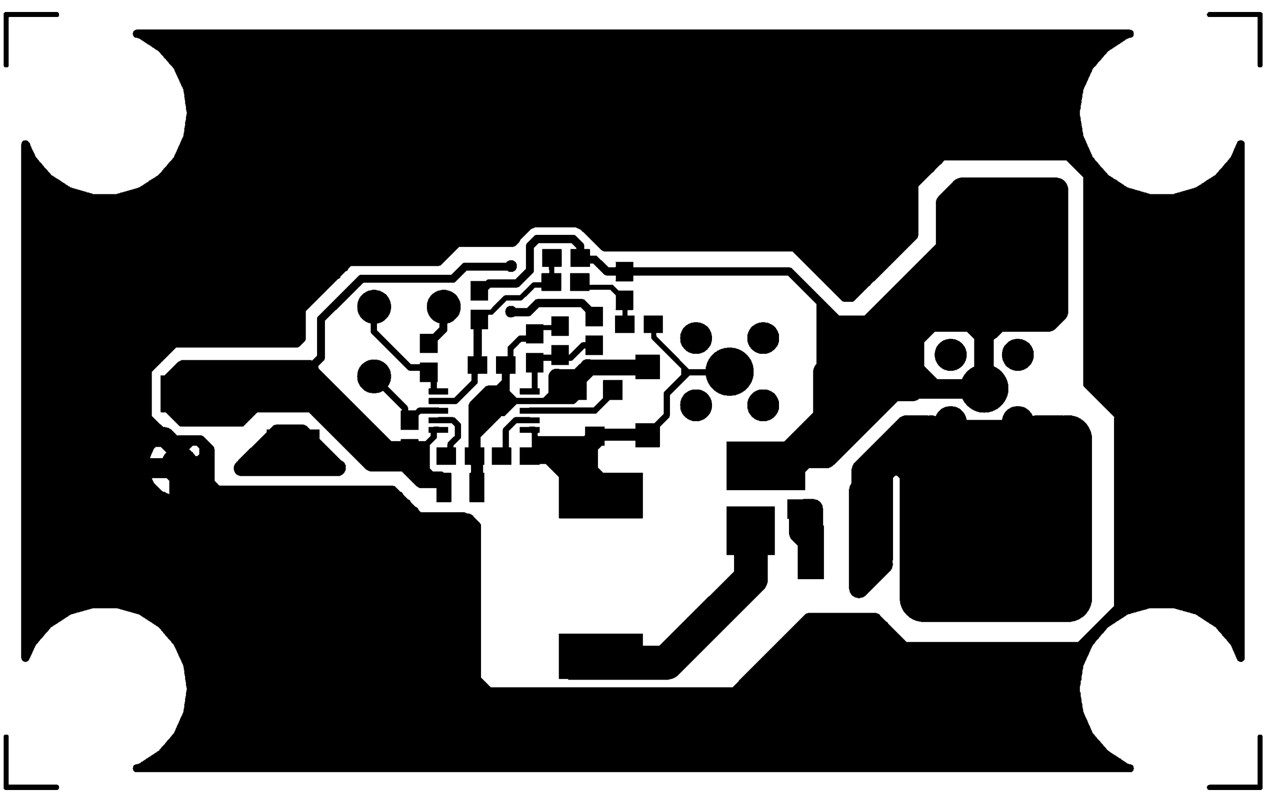

Figure 14. Board Top Layer

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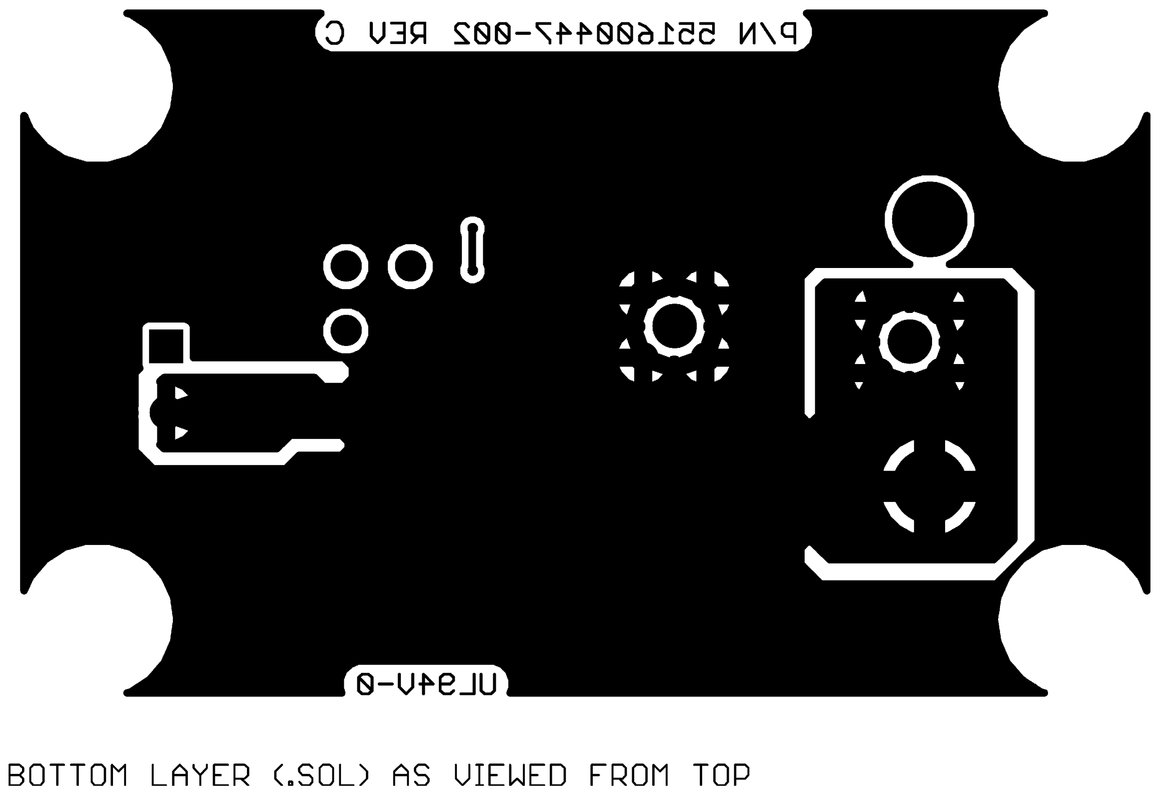

Figure 15. Board Bottom Layer (Viewed from Top)

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