

Implementation of an FSK Modem Using the TMS320C17

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Abstract

This report presents a complete hardware design for a splitband modem, and the software to implement a V.21/Bell 103 300-bps modem, using a TMS320C17 DSP.

- ❑ The first section reviews basic modem concepts and definitions and introduces frequency shift keying (FSK) data modulation.
- ❑ The second section describes the major functional blocks of the FSK modem system.
 - Host Interface
 - Modem Controller
 - Digital Signal Processor
 - Analog Front End
- ❑ The third section discusses DSP software implementation of the V.21/Bell 103 300-bps modem, using a TMS320C17 DSP.
- ❑ The fourth section reviews some issues involved with incorporating additional code into DSP software provided in Appendix B.
- ❑ The fifth section summarizes conclusions.
- ❑ Appendix A is a derivation of the filter coefficient value required for the sample fraction time delay.
- ❑ Appendix B is the source code listing for the TMS320C17 modem implementation.

The report also includes flow chart and tabular frequency and phase step data.



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Introduction

This application report presents an implementation of a 300-bit-per-second (BPS) modem conforming to the V.21 and Bell 103 standards, using a TMS320C17 Digital Signal Processor (DSP).

The purpose of this application report is, with references [1], [2], [3], to provide a complete hardware design for a splitband modem and the software to implement a V.21/Bell 103 300-bps modem. The designer can then concentrate on developing value-added functions, such as V.22bis or V.22 standard modems, encryption algorithms, etc. These value-added functions are implemented in software and can be easily incorporated into the TMS320C17 software provided in Appendix B.

The structure of this report is as follows:

- The first section reviews basic modem concepts and definitions and introduces the reader to frequency shift keying (FSK) data modulation.
- The second section describes the major functional blocks of the FSK modem system presented in this report:
 - Host interface,
 - Modem controller,
 - Digital signal processor, and
 - Analog front end.
- References to documents describing the actual hardware implementation are provided.
- The third section discusses the DSP software implementation of the V.21/Bell 103 modulator/demodulator using the TMS320C17 DSP.
- The fourth section reviews some of the issues involved with incorporating additional code into DSP software provided in Appendix B.
- The fifth section concludes this report.
- Appendix A is a derivation of the filter coefficient value required for the sample fraction time delay.
- Appendix B is the source code listing for the TMS320C17 modulator and demodulator implementation.

Background

Over the past decade there has been a proliferation in the number and the use of computer systems. Accompanying this growth, there has been an increased demand for data communications between the various computer systems and terminals.

One of the most convenient and frequently used methods of data communications between geographically separated computer equipment is via the Public Switched Telephone Network (PTSN). The essential element for this method of data communication is the modem.

The modem converts the digital data it receives from the computer system or terminal into a modulated analog signal that is transmitted via the telephone network to the destination computer system or terminal. At the destination, the receive modem demodulates the received signal and transfers the digital data to the receiving terminal or computer system.

Table 1 shows a number of popular modem standards as specified by either the International Telegraph and Telephone Consultive Committee (CCITT) or the Bell System.

Table 1. Bell and CCITT Modem Standards

Modem	Standard	Type*	Modulation	Data Rate (BPS)	Duplex
Bell	103	S/B	FSK	300	Full
	202	S/B	FSK	1200	Half
	212A	S/B	DPSK	1200	Full
	201	S/B	DPSK	2400	Half
CCITT	V.21	S/B	FSK	300	Full
	V.22	S/B	DPSK	1200	Full
	V.22bis	S/B	QAM	2400	Full
	V.32	E/C	QAM	9600	Full

* S/B = Split band E/C = Echo Cancelling

Modems can be either half-duplex or full-duplex. In a half-duplex system, the transmission can be in either direction; however, only one direction is possible at a time. A half-duplex modem cannot simultaneously transmit and receive information. At the end of its transmission sequence, the modem must advise the receiving modem that the sequence is complete. The receiving modem may then begin transmitting data.

In a full-duplex system, the data transmission is bidirectional. Both modems may simultaneously transmit and receive data. Bidirectional (simultaneous data transmission) is achieved by either splitband or echo cancellation techniques.

Figure 1 shows the spectral response of a typical telephone channel. A splitband modem uses a filtering scheme to separate the telephone channel into two distinct frequency bands. One band is dedicated to the transmissions of the originate modem, the other band is dedicated to transmissions of the answer modem. To separate the received signal from the received and transmitted signal that is detected on the two-wire telephone line, the modem removes the transmitted signal frequency band using a splitband filter [1], [4], or by other means (such as software implemented on the DSP). Dividing the telephone channel into two separate non-overlapping frequency bands limits the maximum baud rate.

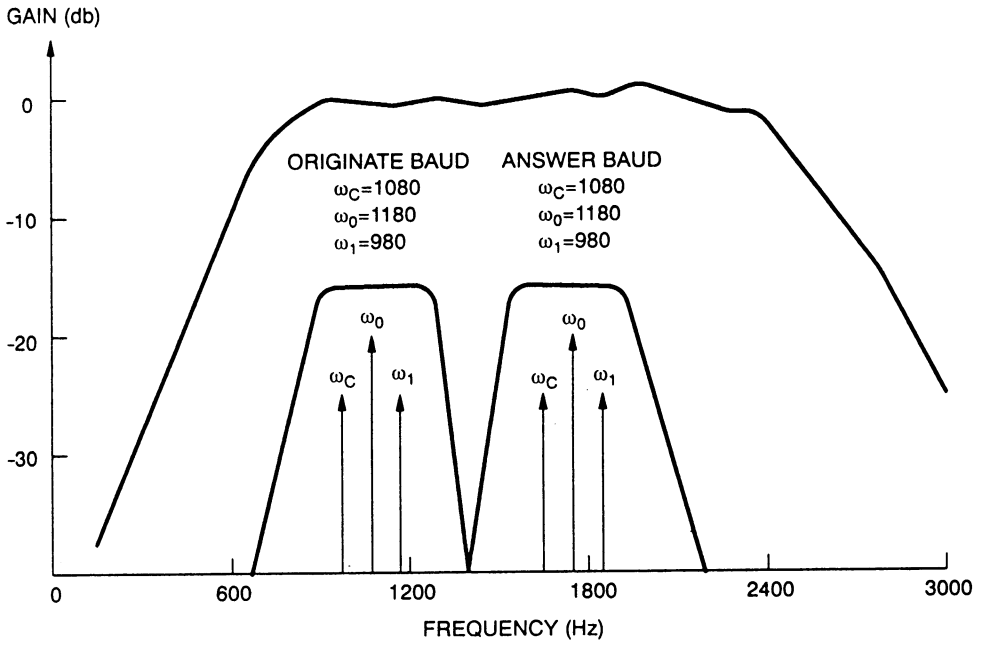


Figure 1. Spectral Response of a Typical Telephone and a V.21 Splitband Modem

The actual bit rate of the channel is determined by the baud rate and the data modulation scheme that is employed. Splitband type modems are typically used in low- to moderate-speed applications. As shown in Table 1, each modem standard uses a particular modulation scheme. For example, CCITT V.21, V.22, and V.22bis standards specify the frequency shift keyed (FSK), phase shift keyed (PSK) and quadrature amplitude modulation (QAM) schemes respectively.

Echo cancellation type modems, such as V.32, transmit both the originate and answer signals on the same channel. This allows both the originate and answer modems to utilize the complete bandwidth of the channel and to maximize the data baud rate. It is still necessary to separate the receive signal from the receive and transmit signal detected on the two-wire telephone line. However, the originate and answer signals are superimposed on the same channel band, and separating techniques that are more sophisticated than those found in splitband-type modems are required. The fact that transmit signal is typically 20 dB stronger than the receive signal, as measured on the transmit Tip and Ring, further complicates the extraction of the receive signal.

Echo cancellation type modems use algorithms that subtract an estimate of the transmit signal from the signal sampled from the two-wire telephone line, to determine the receive signal. Refer to [5] and [6] for further information on Echo cancellation type modems.

Table 2 shows the transmission frequencies for answer and originate modes for both the binary FSK modulated 300-bps V.21 and Bell 103 standards. It also shows details of the V.23 and Bell 202 1200-bps half-duplex standards.

Table 2. Binary FSK Transmission Frequencies

Modem Standard		Carrier (Hz)	1(Mark) (Hz)	0(Space) (Hz)
V.21	Originate	1080	980	1180
	Answer	1750	1650	1850
BELL 103	Originate	1170	1270	1070
	Answer	2125	2225	2025
V.23		1700	1300	2100
BELL 202		1700	1200	2200

Since this report is primarily concerned with the 300-bps V.21 and Bell 103 standard modems, it is worthwhile to review FSK data communication.

These are the primary advantages of an FSK system:

1. There is no requirement for carrier phase recovery; this reducing system complexity.
2. Increased immunity to amplitude nonlinearities. FSK is a constant envelope signal, with the information transmitted in the zero crossings. It is less affected by amplitude nonlinearities than amplitude modulated schemes, and
3. The modulator and demodulator architectures are easily implemented in software.

The primary disadvantage of FSK modulation is its low spectral efficiency. Because the telephone network is bandlimited to 4KHz, only moderate data transmission rates over the telephone network are supported by an FSK modulation scheme. As a consequence, FSK is often the favored modulation scheme for very low cost, low-to-moderate speed data communication systems.

Subsequent sections of this report discuss FSK modulation and demodulation in some detail. It is important that you understand the mathematical representations of FSK signals. FSK modulation is represented in the following manner:

$$S(t) = \cos((\omega_c \pm \delta\omega) * t + \phi) \quad (1)$$

where $S(t)$ = Transmitted signal

ω_c = Carrier frequency

$\delta\omega$ = Frequency shift

t = Time

ϕ = Phase shift

For a given baud period T , $S(t)$ is at a frequency $f_1 = (f_c + \delta f)$ or $f_0 = (f_c - \delta f)$, corresponding to the transmission of a 1 or 0, respectively, for the duration of the baud period. In some cases, it is convenient to represent

$$\omega_0 = \omega_c - \delta\omega \quad (2)$$

$$\omega_1 = \omega_c + \delta\omega$$

Thus the following identities are true:

$$\omega_c = (\omega_1 + \omega_0)/2 \quad (3)$$

$$\delta\omega = (\omega_1 - \omega_0)/2$$

Some binary FSK modulation schemes, such as V.21, have ω_0 greater than ω_1 ; so by (3), $\delta\omega$ would be negative. Figure 2 shows an FSK signal transmission.

Note that the telephone channel provides limited spectral bandwidth. To achieve progressively higher data rates, more spectrally efficient modulation schemes, such as PSK and QAM, must be used. As spectral efficiency increases, typically, the complexity of the signal modulation and demodulation schemes increase. Additional information on modulation schemes can be found in references [4], [5], [6] and [7].

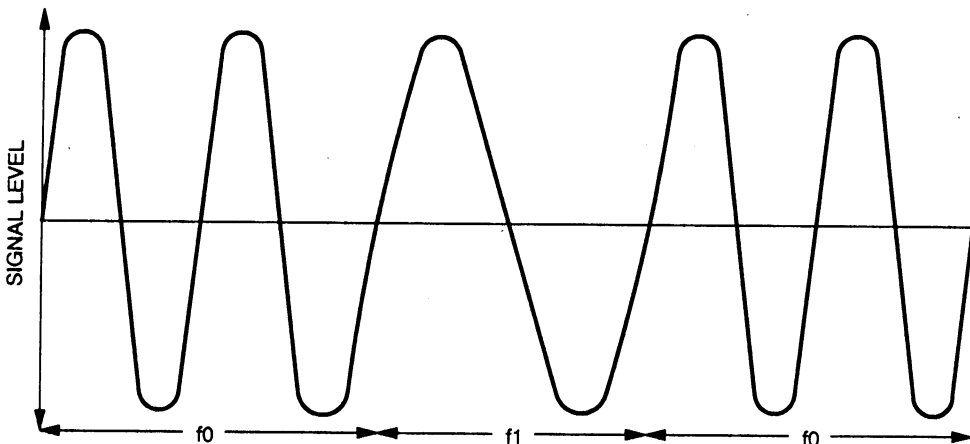


Figure 2. FSK Signal Transmission

System Description

As discussed in the introduction, this application report presents the implementation of a V.21/Bell 103 300-bps FSK modem using a TMS320C17 Digital Signal Processor. The system hardware is identical to that of the Texas Instruments DSP2400 modem [1].

There are significant functional differences between the modem design provided here and the DSP2400 modem. These result from the differences between the TMS320 code provided in Appendix B and the DSP2400 code. The software found in Appendix B implements a V.21/Bell 103 FSK modem. The DSP2400 also implements V.22, Bell 212A, and V.22bis standard modems that implement PSK and QAM modulation/demodulation and the associated carrier recovery, clock recovery, and adaptive equalization functions.

The software in Appendix B provides all the necessary hooks so that the designer can easily incorporate his own custom value-added features (such as V.22 and V.22bis standard modems). Nevertheless, the reader should be aware of the difference between the DSP2400 software implementation and the software in Appendix B, particularly when referring to any DSP2400 related literature [1], [2], [3].

Figure 3 is a block diagram showing the components of the modem system. The modem consists of the following subsystems:

1. Host interface
2. Modem controller
3. Digital signal processor
4. Analog front end

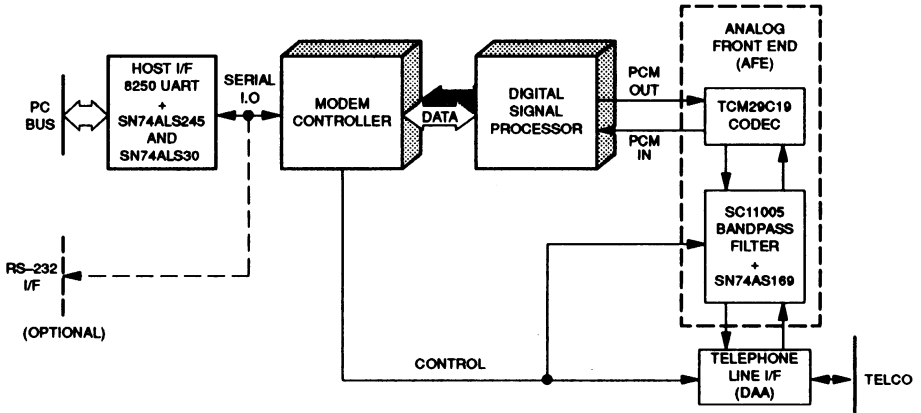


Figure 3. Block Diagram of Modem System Components

The designer must provide an interface between the host data terminal equipment and the modem controller. The DSP2400 uses an 8250 UART (plus a 74LS245 buffer and a 74ALS30 NAND Gate) to interface between a standard PC-AT and the modem controller. A standard RS-232C interface is used between the UART and the modem controller. The circuit diagram and additional information on the host interface used for the DSP2400 Modem can be found in [1].

The modem controller (80C51, TMS70C42, etc.) handles the overall modem control [3], directs the handshaking sequences, etc. It specifically performs the following functions:

1. AT command set interpretation
2. Scrambling/descrambling
3. Pulse dialing
4. Synchronous/asynchronous conversion
5. Modem configuration control
6. Protocol initialization

The modem controller sends a command to the DSP once per baud. Table 3 is a complete list of the commands, showing the structure and functions that are implemented.

Table 3. Modem Controller Commands for the DSP

Command	Code	Description
Protocol Select	Fxh	Select protocol Bits 1, 0 – Speed select 0 0 = 300 BPS 0 1 = Reserved 1 0 = Reserved 1 1 = Reserved Bit 2 – CCITT/Bell 0 = CCITT 1 = Bell Bit 3 – Answer/originate 0 = Answer 1 = Originate
Reserved	Exh	Reserved command
Operation Select	Dxh	Select operating mode (bits 3, 2 reserved) 0 0 = Line mode 0 1 = Analog loopback 1 0 = Reserved 1 1 = Reserved
Reserved	Cxh	Reserved command
Reserved	Bxh	Reserved command
Reserved	Axh	Reserved command
Transmit DTMF Tones	9xh	Dial DTMF and return to configuration mode xxxx = D3-D0; numbers 0-9, A, B, C, D, *, and #

Table 3. Modem Controller Commands for the DSP (Concluded)

Command	Code	Description
Transmit Mode Select	8xh	Enable answer tone/data select Bits 1, 0 = Transmit select 0 0 = Transmit idle 0 1 = Transmit answer tone 1 0 = Transmit data mode enable 1 1 = Reserved Bits 3, 2 = Select answer tone frequency 0 0 = 2100 Hz answer tone (V.21) 0 1 = 2225 Hz answer mark (Bell 103) 1 0 = 2025 Hz answer space (Bell 103) 1 1 = Reserved
Receive Mode Select	7xh	Select receive configuration (bits 3,2 reserved) 0 0 = Receive idle mode 0 1 = Reserved 1 0 = Receive data mode 1 1 = Reserved
Reserved	6xh	Reserved command
FSK Mode	5xh	Select 300 BPS mode (bits 3,2,1 reserved) 0 = 300 BPS mode deselect 1 = 300 BPS mode select
Reserved	4xh	Reserved command
Reserved	3xh	Reserved command
Reserved	2xh	Reserved command
Reserved	1xh	Reserved command
Reserved	0xh	Reserved command

As an example, the DSP2400 uses a masked ROM version of the TMS70C42 microcontroller (denoted as a TMS70C2400A) as the modem controller. The TMS70C2400A source code is available from Texas Instruments and includes provisions for the V.22bis and V.22 standard modems.

One noteworthy advantage of the TMS70C42/TMS320C17 interface is that it requires no external glue logic [7]. For complete information on the TMS70C2400 Modem Controller, including the call originate and answer sequences, refer to [2].

The TMS320 Digital Signal Processor performs the computationally intensive tasks such as modulation, demodulation, and tone generation and detection. It does not perform any control functions. Specifically, the TMS320 DSP performs the following functions:

1. Modulation/demodulation (V.21/Bell 103)
2. Data encoding/decoding
3. Filtering
4. Automatic gain control
5. Tone dialing
6. Call progress monitoring

The DSP is discussed in further detail in the next section of this application report. The DSP source code in Appendix B was originally part of the code developed for the TMS320A2400 Modem Digital Signal Processor (a ROM coded TMS320C17 DSP). The TMS320A2400 source code also includes V.22bis, V.22, and Bell 212A standard modems, with the software implementing the QAM and PSK modulation and demodulation schemes, carrier recovery, clock recovery, automatic gain control, and adaptive equalization functions. The TMS320A2400 and the source code is available from Texas Instruments.

Despite the differences between the code provided in Appendix B and the TMS320A2400 code, [1] and [3] are useful references, providing technical information about TMS320C17 modem applications.

The analog front end is composed of a TCM29C19 combo codec [9], a SC11005 bandpass filter [10] and a data access arrangement (DAA) telephone line interface composed of discrete components. The codec converts an 8-bit μ -law companded bit stream to an analog waveform and vice versa, at a 9.6-KHz sampling frequency. The SC11005 is a splitband filter that separates the transmit and receive carriers and performs the required signal shaping to the analog waveform. The DAA section is composed of a number of discrete components and is required to interface the modem to the public telephone network as dictated by FCC Rules Part 68. The analog front end circuit diagram is found in [1]. Further technical details are found in [2].

The DSP Software Implementation

The code provided in Appendix B is written specifically for a Texas Instruments TMS320C17 Digital Signal Processor. The key architectural features of the TMS320C17 are these:

1. 4 Kwords (8 Kbytes) of on-chip maskable ROM
2. 256 words of on-chip data RAM
3. Two full-duplex serial ports
4. On-chip companding hardware (μ - or A-Law)
5. On-chip sign magnitude/two's complement conversion hardware
6. A coprocessor port
7. 6.25-MIPS maximum execution speed

TMS320E17, with 4 Kwords of on-chip EPROM substituted for the 4 Kwords of maskable ROM, is also available for development and prototyping purposes. Refer to [8] and [11] for additional information on the TMS320C17 and TMS320E17.

The TMS320C17 source code listing file is found in Appendix B. The code requires approximately 50 words of data RAM and occupies 1100 words of program ROM. Of the 1100 words of program memory, 390 are coefficients, and the remaining 710 words are the program instructions. The software consists of a main program that references various subroutines. These are the main subroutines found in the program:

1. Command control interpreter (CCI)
2. FSK transmitter (FSKTX)
3. Dual-tone multifrequency transmitter (Part of FSKTX)
4. Automatic gain control (AGC)
5. FSK receiver (RSTSK)

The next section of text describes the main program. The subroutines are discussed in subsequent sections.

Figure 4 is a block diagram of the main program (code starting at beginning of main program label and ending at start of subroutines label) in Appendix B. Once the initialization of the data RAM and control registers (code beginning at start of additional tables label and ending at start of main program sequencer label) is complete, the main program loop is executed. The device remains in the WAIT loop (first four lines of code of main program sequencer routine) until the FR flag in the control register is raised. Control register bits 27-24 and 23-16 are set so the main program and data samples are transmitted/received to/from the TCM2919 codec at a rate of 9.6 KHz.

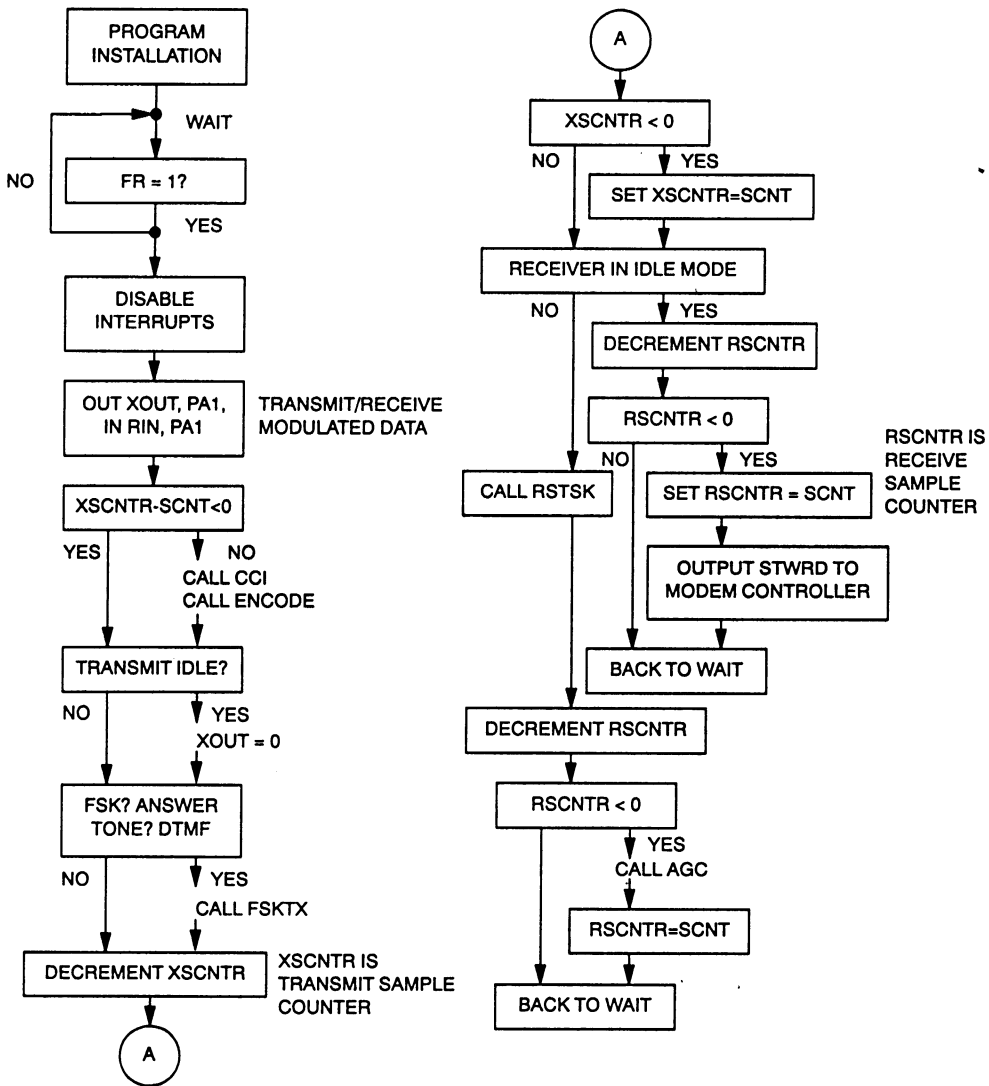


Figure 4. Flowchart of Main Program (Appendix B)

As the V.21/Bell 103 standard modems transmit data at 300 bps, a 9.6-KHz sampling rate results in 32 samples/ baud. The 9.6-KHz sampling rate is very practical for several reasons:

- It is higher than the Nyquist sampling frequency of approximately 8 KHz for a telephone channel, and
- It is a convenient multiple of the popular modem transmission frequencies (300, 1200, and 2400 bps).

The TMS320C17 is clocked by a 18.432-MHz oscillator. To satisfy the 9.6-KHz sampling frequency, the number of instructions executed per sample must be less than 480. To implement the various functions required by the FSK modulator/demodulator, it is necessary to distribute the tasks among the various samples within the baud. The command control interpreter (CCI) is executed during the first sample of the baud, and the AGC routine is implemented during the final sample baud.

When the raised FR flag is detected, the processor exits the WAIT loop and executes the main program. Refer to [8], Sections 3.8 and 3.9 for additional details on the FR flag, interrupts, and serial port. Table 4 describes the variables that are referenced in the main program.

Table 4. Variables Referenced in Main Program Variable

Variable Name	Description
XSCNTR	The transmit counter; equals the number of samples that have been transmitted in the current baud.
SCNT	Number of samples in a baud, i.e., 9.6 KHZ/300 HZ = 32 samples/baud.
XOUT	Output sample sent via the TX serial port to the combo codec.
RIN	Input sample sent via RX serial port from the combo codec.
STATUS	An 8-bit number used internally by the DSP. Indicates present operating mode of the modem.
STWRD	8-bit status word sent to the modem controller by the DSP. See Table 5.
OAFLAG	Indicates if modem is in originate or answer mode. OAFLAG = 0 → originate mode.
DTFLAG	Indicates if the modem is transmitting DTMF tones. DTFLAG = 1 → transmitting DTMF data.

Table 5 shows the organization of STWRD (the DSP status word that is written to the microcontroller).

Table 5 STWRD - DSP Status Word Written to the Modem Controller

Bit No.	Description
7	Enable/disable automatic gain control. 0 = Enable 1 = Disable
6	EDT (in band energy) 0 = Not detected 1 = Detected
5	Reserved
4	Reserved
3	Received data bit (0,1)
2	Reserved, set to 1
1	Reserved, set to 1
0	Reserved, set to 1

When the program exits the wait loop, it disables all interrupts and reads a data sample RIN from the receive buffer or writes a data sample XOUT to the transmit buffer of serial port #1.

At the first sample of a baud, when $XSCNTR = SCNT (=31)$, the program implements the command control interpreter (CCI) subroutine as shown in the following code. Note that $SCNT = 31$, and $XSCNTR$ is initially set at 31 and decremented by 1 every sample. When $XSCNTR$ equals 0, it is reset to 31, for a total of 32 samples.

```

LAC    XSCNTR
SUB    SCNT      ; ACCUM = XSCNTR-SCNT
BLZ    SEQU     ; BRANCH TO SEQU IF ACCUM < 0
CALL   CCI
SEQU:  LACK    030h

```

The CCI subroutine reads the next 8-bit command from the modem controller (TMS70C42400A or equivalent), performs the required program control functions, and returns to the main program.

If the DSP is in transmit idle mode, the data sample XOUT is set to 0 and sent to serial port #1 transmit buffer.

If the DSP is not in transmit idle, the FSK transmit subroutine FSKTX is called. Depending on the present value of STATUS as determined by the modem controller and the CCI subroutine, the FSKTX subroutine will transmit FSK encoded data, DTMF tones, or an answer tone. Upon completing the FSKTX subroutine, the program decrements the transmit sample counter XSCNTR by 1 and checks to see if it is less than 0. If so, XSCNTR is reset to 31. Otherwise, the program proceeds without any further modifications to XSCNTR.

At this point, the main program checks to see if the receiver is in idle mode. If the receiver is in idle mode, the receive sample counter RSCNTR is decremented. If RSCNTR is not less than 0, the program returns to the WAIT loop. If RSCNTR is now less than 0, it is reset to 31, and the program then returns to the WAIT loop.

If the receiver is not in idle mode, the receiver decode/demodulation subroutine RSTSK (receiver per sample task) is called. This subroutine demodulates the receiver signal and estimates the value of the received data. When the subroutine is complete, the main program decrements RSCNTR and resets it to 31, if required.

After the RSTSK subroutine is complete, the program decrements RSCNTR. If RSCNTR is greater or equal to 0, the program returns to the wait loop. For the sample, when RSCNTR is less than 0, the automatic gain control subroutine (AGC) is called once per baud. The AGC subroutine monitors and compensates for any significant variation of the received signal level caused by telephone line fluctuations and other dynamic effects. RSCNTR is then RESET to 31, and the program returns to the WAIT loop.

The main program calls the following subroutines:

- CCI—Command control interpreter
- DTMF—DTMF setup
- FSKSET—Set up FSK transmit frequency
- FSKTX—Transmitter mode select
- OPER—Set operating mode
- PROTO—Protocol select
- RESET—Reset and equalizer enable
- RMODE—Receiver mode select
- RSTSK—FSK demodulation
- XMODE—Transmitter mode select

Figure 5 shows a block diagram of the CCI subroutine. The CCI reads the setup command from the modem controller (through the co-processor port PA5) and stores it in data RAM location XDATA (The structure of XDATA is shown in Table 3). The CCI then calls the appropriate subroutine to modify the system control bits (OAFFLAG and DTFLAG) and status register (STATUS). The CCI, depending whether the modem configuring the DSP is in answer, originate, or transmit DTMF, loads the required nominal frequency values into TXFRQ and RXFRQ. Table 6 shows the organization of the STATUS register.

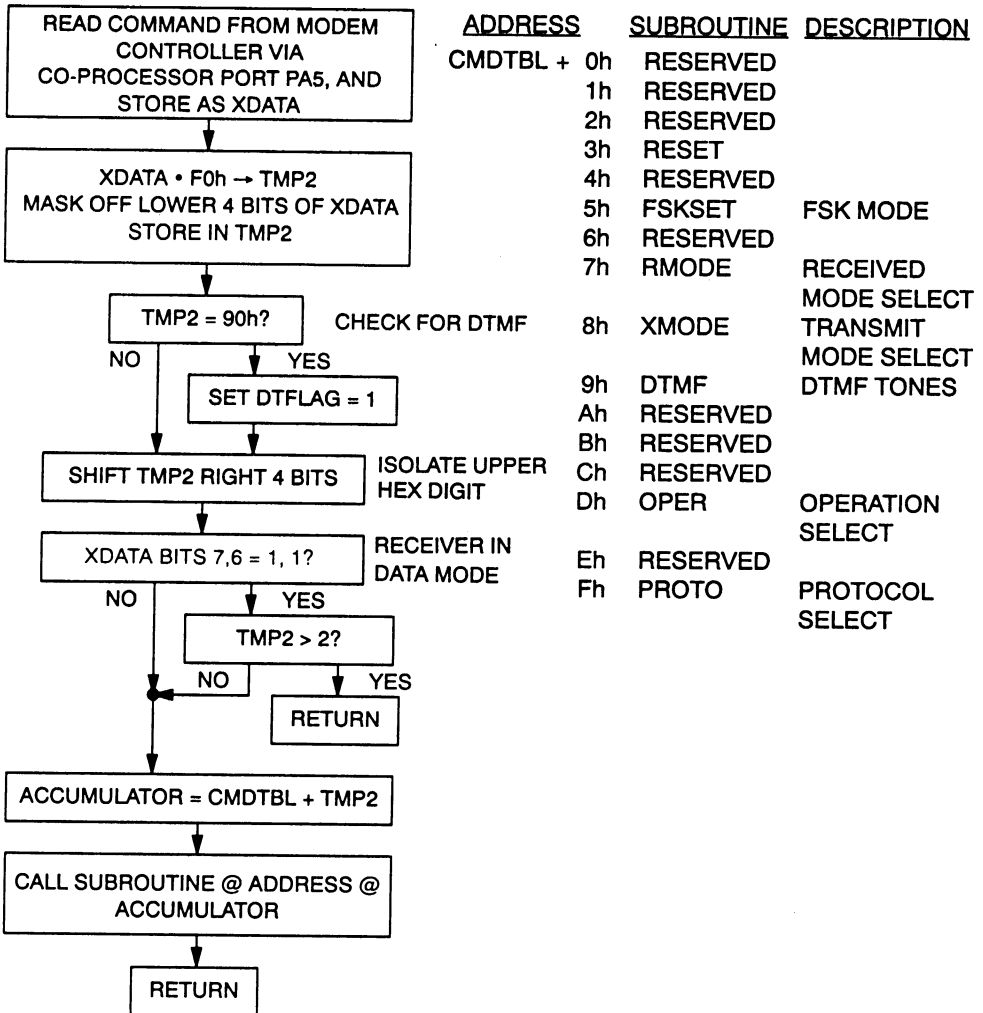


Figure 5. Flowchart of the CCI Subroutine

Table 6. The Status Register Organization

Bits	Description
7,6	Indicate Receiver Mode: 00 = Receiver in Idle Mode 01 = Call Progress Monitoring Mode 10 = Data Mode 11 = Reserved
5,4	Indicate Transmitter Mode: 00 = Transmitter in Idle Mode 01 = Transmit Answer Tone 10 = Data Mode 11 = Reserved
3	Answer/Originate Mode: 0 = Originate Mode 1 = Answer mode
2	CCITT/Bell Mode: 0 = CCITT (V.21) 1 = Bell (103)
1,0	Speed status: 00 = 300 BPS 01 = Reserved 10 = Reserved 11 = Reserved

The setup commands from the modem controller and subroutines called by the CCI subroutine are shown in Table 3.

The RESET subroutine loads 81h into the STWRD word that is sent to the modem controller via the co-processor port PA5. This advises the modem controller that the DSP has been reset. The DSP program then branches to START, and the DSP is reinitialized.

The FSKSET subroutine reads the XDATA word to determine if the next bit to be transmitted is 0 or 1 and then loads the appropriate 0 or 1 frequency FOADD or F1ADD into the TXFRQ register.

When setup in answer mode, XDATA bits 3 and 2 are loaded into the STATUS register bits 7 and 6, respectively, by the RMODE subroutine. These bits determine what tasks the FSK receiver subroutine RSTSK will perform, as shown in Table 3 and Figure 5.

The XMODE subroutine reads XDATA bits 0 and 1. These bits determine what tasks the FSK transmitter subroutine FSKTX will perform as shown in Figure 4. If the transmit answer tone function is selected, bits 2 and 3 of XDATA indicate what the answer tone frequency will be:

XDATA Bits 3,2 = 0,0	2100 Hz
0,1	2225 Hz
1,0	Reserved
1,1	Reserved

The program loads the appropriate answer tone value into register TXFRQ. XMODE then loads XDATA bits 1 and 0 into STATUS bits 5 and 4, respectively. STATUS bits 5 and 4 determine what tasks the transmitter subroutine FSKTX will perform.

The DTMF subroutine determines what number or symbol needs to be transmitted by reading XDATA bits 3 through 0. DTMF then loads the appropriate high-frequency phase step, low-frequency phase step, high-frequency gain, and low-frequency gain into the RXFRQ, TXFRQ, DTMFH, and DTMFL registers, respectively, from the Table TONTBL.

The OPER subroutine checks bits 1 and 0 of XDATA. If bits 1 and 0 equal 0 and 1 bit 3 of STATUS is set to 1, indicating that the modem is in analog loopback mode. If bits 1 and 0 are not equal to 0 and 1, OPER returns without performing any operations.

The PROTO subroutine selects the mode and protocol of the DSP based on XDATA bits 3 through 0. PROTO first sets bits 1 and 0 of STATUS (indicating the modem data rate), based on the value of bits 1 and 0 of XDATA (see Figure 7).

While the software provided in Appendix B supports only a 300-bps data rate, it does provide the necessary hooks so that different standard modems (ie V.22, V.22bis) can easily be incorporated into the code.

Next, PROTO checks XDATA bits 3 and 2 to determine if the modem should be in originate/answer mode and Bell/CCITT mode.

Bit 3:	0 = Originate
	1 = Answer
Bit 2:	0 = Bell
	1 = CCITT

As shown in Table 2, the transmission frequencies of the Bell 103 and V.21 originate and answer modes are unique. PROTO loads registers used by the FSK transmitter

subroutine (FSKTX) and the FSK receiver subroutine (RSTSK) with values stored in table TONTBL in data ROM and corresponding to transmit and receive frequencies.

PROTO then uses the XDATA bits 3 and 2 to determine which constants are transferred from table FSKTBL into addresses F1ADD (transmit 1 phase step), F0ADD (transmit 0 phase step), B1FSK (FSK delay filter coefficient), and GAIN (FSK mode gain). PROTO also loads addresses SCNT (baud counter=32), TRANS (FSK data transmission N=15), A1FSK (A1 demodulator filter coefficient), A2FSK (A2 demodulator filter coefficient), and DZONE (dead zone of window comparator) with the appropriate values.

If bit 3 of the STATUS word equals 1, the modem is set to analog loopback mode, and the modem should receive the information that it transmits. PROTO checks to see if bit 3 of STATUS equals 1; if so, the receiver parameters are modified to be the same band as the transmitter.

The FSK modulator is implemented in the FSKTX subroutine. Figure 6 is a block diagram of the FSKTX subroutine. The primary function of the FSK modulator is the following: Given a stream of binary data $a_0, a_1, a_2, \dots, a_{k-1}, a_k$ for each data element $a_k = \{0, 1\}$, generate a corresponding signal of frequency f_0 or f_1 for the duration of a_k 's baud period.

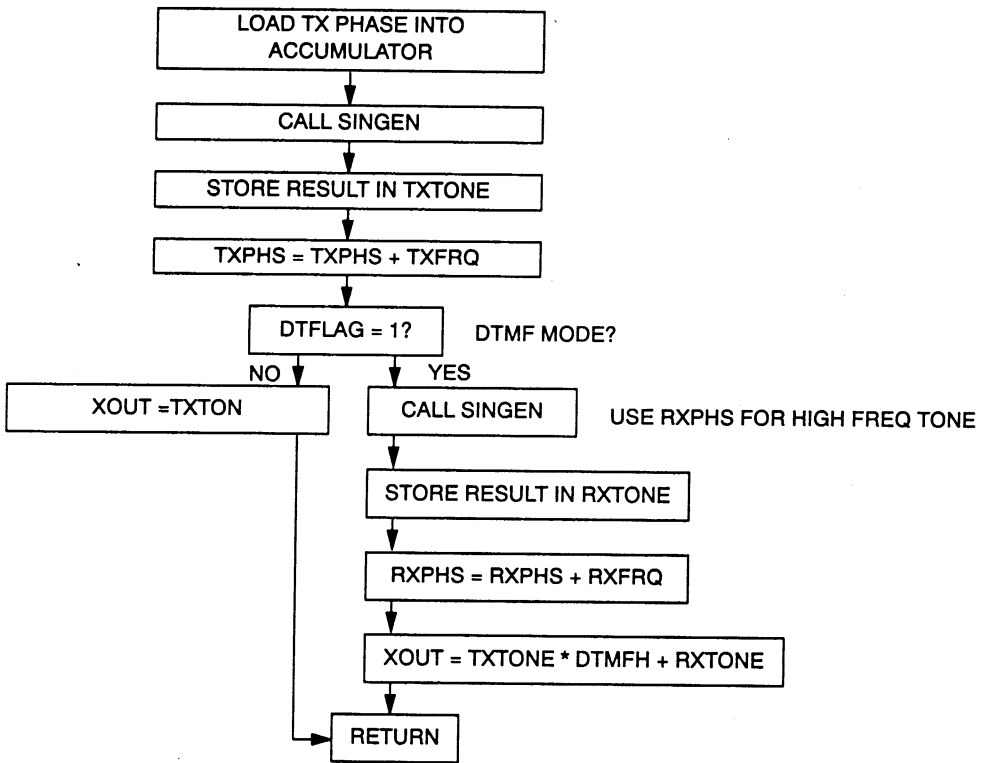


Figure 6. Flowchart of Subroutine FSKTX

Figure 7 shows a functional model of the FSK modulator. The TMS320 software implementation of the FSK modulator generates tones by stepping through a cosine table. The size of the phase step determines the output signal frequency. You should pay particular attention how phase angles, phase steps, cosines, and sines are represented as 16- and 32-bit integer numbers.

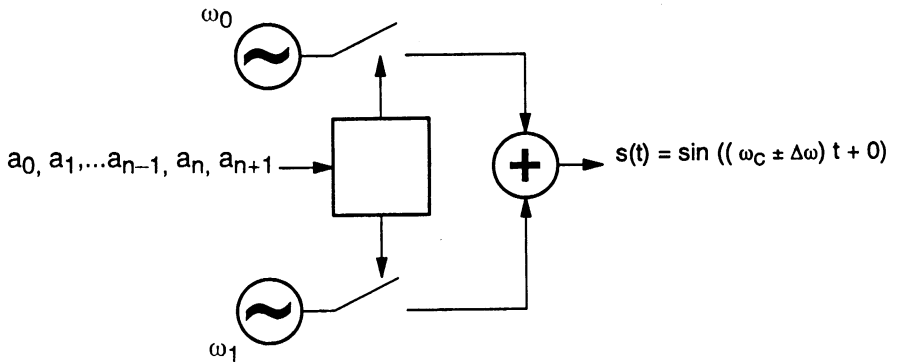


Figure 7. Functional Model of an FSK Modulator

Table 7 describes the significant variables used in the FSKTX subroutine.

Table 7. Variables Referenced in the FSK Transmitter Subroutine FSKTX

Variable Name	Description
TXPHS	Present value of the transmit signal phase. Also used as present phase of the low frequency DTMF tones.
TXFRQ	Phase step between consecutive TXPHS samples.
RXPHS	Normally used in the FSK demodulator subroutine RXTSK. Used as present phase for the high frequency DTMF tone.
RXFRQ	Normally used in RXTSK subroutine. Also used as phase step for high-frequency tone when transmitting DTMF tones.
DTMFL	Scaling factor for low-frequency DTMF tones.
DTMFH	Scaling factor for high-frequency DTMF tones.
SINGEN	A subroutine called by FSKTX. Given a 16-bit number representing an angle from 0 to Pi, the SINGEN routine determines the sine of the angle and stores the result at address TMP3.

The software FSK Modulation routine receives data at a rate of 300 bps and generates 12-bit, two's complement data samples at a rate of 9.6 KHz. The TMS320C17's on-chip hardware compander reduces the sample to 8 bits before it is sent to the Codec via the serial port.

The most recent phase of the output signal is stored in data memory location TXPHS, and the amplitude is read from the COSOFF table by the SINGEN subroutine. The frequency of the transmitted signal is determined by the size of the phase step TXFRQ between successive output samples:

$$\text{TXPHS}[(N+1)T] = \text{TXPHS}[NT] + \text{TXFRQ}[NT]$$

The value of TXFRQ is determined by the FSKSET subroutine referenced by the CCI subroutine. Recall that, depending on the instruction received from the modem controller at the beginning of the baud, the CCI subroutine loaded data memory location TXPHS with either F0ADD or F1ADD. Table 8 shows the FSK frequencies and phase steps (TXFRQ) for the V.21 and Bell 103 modem standards.

Table 8. Frequencies and Phase steps for V.21 and Bell 103 Modems

Modem Standard		Frequency (Hz)	Phase Step @9.6 KHz	Phase Step TXFRQ, Q15 hex
V.21	Originate 1	980	$0.2042 * \pi$	1A22h
	Originate 0	1180	$0.2458 * \pi$	1F77h
	Answer 1	1650	$0.3428 * \pi$	2C00h
	Answer 0	1850	$0.3854 * \pi$	3155h
Bell 103	Originate 1	1270	$0.2646 * \pi$	21DDh
	Originate 0	1070	$0.2229 * \pi$	1C89h
	Answer 1	2225	$0.4635 * \pi$	3B55h
	Answer 0	2025	$0.4219 * \pi$	3600h

The magnitude of the phase step is determined by

$$[(\text{Desired Frequency})/(\text{Sampling Frequency})] * 2\pi$$

In the case of the originate 1 of the V.21 modem, the phase step equals

$$(1270/9600) * 2\pi = .2646 \pi \text{ Radians}$$

Both TXPHS and TXFRQ data memory locations are 16-bit binary numbers in Q15 two's complement notation equal to

$$(\text{Output Signal Phase})/\pi.$$

Thus TXPHS hex values

$$2000h = \pi/4$$

$$4000h = \pi/2$$

$$6000h = 3\pi/4$$

$$8000h = -\pi$$

$$A000h = -3\pi/4$$

An advantage of this approach is that the phase of the output signal is continuous. This provides a higher spectral efficiency than that of a discontinuous phase FSK implementation.

The sine generation subroutine SINGEN subtracts $\pi/2$ (4000h) from TXPHS and uses this phase to read the amplitude from the COSOFF table. The symmetry of the cosine function has been used to reduce the table size from 513 to 257 elements, with data memory addresses COSOFF, COSOFF+128, and COSOFF+256 corresponding to 0, $\pi/2$, and π radians, respectively. To determine the cosine of an angle outside the 0-to- π range, the program utilizes the two's complement format of the data and the absolute value function ABS. As an example, assume that the present phase TXPHS is

$$\text{TXPHS}(N) = (-170/256) * \pi = -.6640625 * \pi = \text{A600h}$$

If we are transmitting a 1 in V.21 Originate mode, the phase step is

$$\text{TXFRQ} = .26448 * \pi = 21\text{DDh}$$

The next value of:

$$\begin{aligned}\text{TXPHS}(N+1) &= \text{TXPHS}(N) + \text{TXFRQ} \\ &= -.6640625 \pi + .26448 \pi \\ &= -.3995825 \pi \\ &= \text{A600h} + 21\text{DDh} = \text{C7DDh}\end{aligned}$$

The subroutine then subtracts $\pi/2$ (4000h) from TXPHS, so the sine of angle TXPHS can be determined from the Cosine table:

$$\begin{aligned}\text{ANGLE} &= \text{TXPHS}(N+1) - \pi/2 \\ &= -.3995825 \pi - .5 \pi \\ &= -.8995825 \pi \\ &= \text{C7DDh} - 4000h = 87\text{DDh}\end{aligned}$$

Note that TXRFQ is added to TXPHS(N), and $\pi/2$ is subtracted from TXPHS(N+1) with the sign extension suppressed, so TXPHS(N+1) = 87DDh. This represents 1.06143π as an unsigned number or $-.93857 \pi$ as a signed number. If we now consider TXPHS(N+1) a signed and take the absolute value:

$$\text{ABS}[\text{TXPHS}] = \text{ABS}[\text{87DDh}] = 7823h \text{ representing } .93857 \pi$$

Note that:

$$\text{Cos}(1.06143\pi) = \text{Cos}(.93857\pi) = -.98144$$

The cosine table address is generated:

$$\text{COSSOFF} + (7823\text{h}/80\text{h}) = \text{COSSOFF} + \text{F0h}$$

The value at Data Memory address $\text{COSSOFF} + \text{F0h}$ is

$$\text{Cos}((240/256)\pi) = -.980786 = 8276\text{h}, \text{Q15 } 2\text{'s complement notation}$$

Within the limits of the cosine table precision, the calculated output value equals the value read from the table.

The structure of the FSK Demodulator is shown in Figure 8.

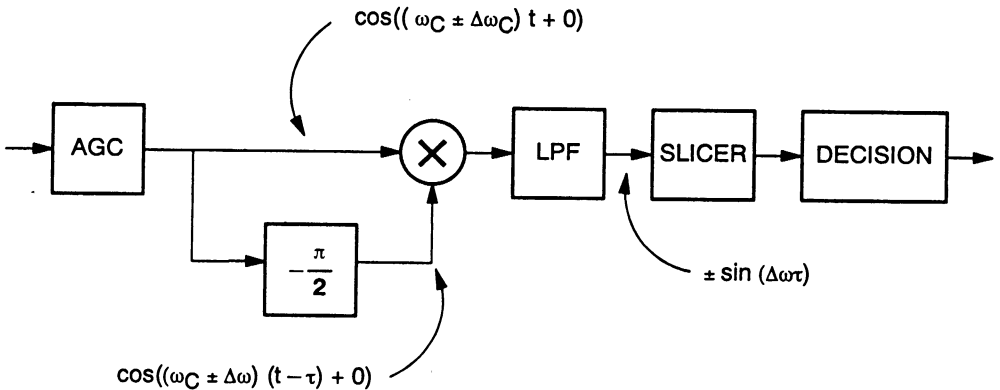


Figure 8. FSK Demodulator

The received FSK signal is sent to the DSP from the Codec via the serial port. The on-chip companding hardware expands the signal from an 8- to 13-bit value. The automatic gain control routine compensates for transient signal level variations and sends the amplitude adjusted received signal $R(t)$ to the software demodulator.

$$R(t) = \cos[(\omega_c \pm \delta\omega) * t + \phi] \quad (4)$$

As this is a binary FSK system, the frequency of this signal is either $\omega_c - \delta\omega$ or $\omega_c + \delta\omega$, depending on whether a 0 or 1 was sent. (Recall from the V.21 signal that $\delta\omega$ is less than 0.)

The received signal $R(t)$ is multiplied by a delayed version of itself:

$$R(t - \tau) = \cos[(\omega_c \pm \delta\omega) * (t - \tau) + \phi] \quad (5)$$

Where τ is the signal delay.

The product of the received signal (4) and delayed received signal (5) is

$$2 * \cos[(\omega_c \pm \delta\omega) * t + \phi] * \cos[(\omega_c \pm \delta\omega) * (t - \tau)] \quad (6)$$

$$= \cos[2(\omega_c \pm \delta\omega) * t - (\omega_c \pm \delta\omega) * \tau + 2 * \phi] + \cos[(\omega_c \pm \delta\omega) * \tau] \quad (7)$$

If $\omega_c \tau$ is set to equal $\pi/2$, and (7) is lowpass filtered to remove the double frequency component, the resulting signal is

$$\cos(\pi/2 \pm \delta\omega * \tau) = \sin(\pm \delta\omega\tau) = \pm \sin(\delta\omega) \quad (8)$$

If $\delta\omega$ is greater than 0, then the sign of the lowpass filter output will be positive or negative, depending on whether $\omega_c + \delta\omega$ or $\omega_c - \delta\omega$ is originally transmitted. If $\delta\omega$ is less than 0, obviously the opposite relationship is true. The sign of the lowpass filter output indicates the value of the received data.

The TMS320 software implementation of the 300-bps FSK Demodulator is found in Subroutine RSTSK, Subroutine CCITT, and Subroutine FDEM20 in Appendix B.

The AGC subroutine provides the RSTSK subroutine with a Q11 two's complement format received signal sample at a rate of 9.6 K samples per second.

As previously discussed, the data is extracted from the received signal by multiplying the received signal by a $\pi/2$ delayed version of itself, $\cos[(\omega_c \pm \delta\omega) * t + \phi - \pi/2 \pm \delta\omega * \tau]$. The product is then passed through a lowpass filter to remove the high frequency components.

If the desired phase delay is

$$\omega_c * \tau = \pi/2, \quad (9)$$

then

$$\tau = 1/(4 * f_c) \quad (10)$$

The sample rate is 9.6 KHz, or a period $T = 104.167 \mu s$. Table 9 shows the carrier frequencies, for both the V.21 and Bell 103 standards, the time delays corresponding to a $\pi/2$ phase delay and the equivalent number of 9.6-Khz samples. Note that none of the delays are exact multiples of the 9.6-KHz sampling period; each delay has an integer and fractional part.

Table 9. Carrier Frequency and Time Delays

Modem Standard		Frequency (Hz)	$\tau(\mu s)$	# of 9.6-KHz Samples
V.21	Originate	1080	231.481	2.2222
	Answer	1750	142.857	1.3714
Bell 103	Originate	1170	213.675	2.0513
	Answer	2125	117.647	1.1294

To minimize the probability of error, it is necessary that the phase delay be as close to $\pi/2$ as possible. An accurate estimate of the fractional part of the delay must be total phase delay. This is achieved by using a single zero FIR filter.

$$R((n - \alpha)T) = GAIN * [R(nT) + B1FSK * R((n-1)T)] \quad (11)$$

where $R(nT)$ is the nth sample of the received signal $R(t)$
 $R((n - \alpha)T)$ is the estimate of the fractionally delayed signal
 n is an integer
 α is the desired fractional delay , $0 < \alpha < 1$

The filter coefficient B1FSK and GAIN for the fractional delay filter of each V.21 and Bell 103 carrier are shown in Table 10. The derivation of the gain and filter coefficients are shown in Appendix A.

Table 10. Time Delay and FIR Filter Coefficients

Modem Standard		Frequency	Fractional Delay 9.6-KHz Sample()	Gain	B1FSK
V.21	Originate	1080	.2222	.69753	.32796
	Answer	1750	.3714	1.00000	.68889
Bell 103	Originate	1170	.0518	.57731	.07175
	Answer	2125	.1294	1.00000	.31678

B1 and GAIN are stored in data memory locations B1FSK and GAIN, respectively. The actual implementation is

$$PDEL1 = AGCOUT + B1FSK * PDEL0$$

where AGCOUT is the received signal after the signal level has been compensated by the automatic gain control routine.

$$\begin{aligned}
\text{AGCOUT} &= \cos[(\omega_c \pm \delta\omega) * nT + \phi] \\
\text{PDELO} &= \cos[(\omega_c \pm \delta\omega) * (n-1)T + \phi] \\
\text{PDEL1} &= \cos[(\omega_c \pm \delta\omega) * (n-1-\alpha)T + \phi], \quad 0 < \alpha < 1 \\
\text{PDEL2} &= \cos[(\omega_c \pm \delta\omega) * (n-2-\alpha)T + \phi]
\end{aligned}$$

Since AGCOUT, PDELO, PDEL1, and PDEL2 are consecutive data memory locations, the integer multiples of the 9.6-KHz sample delays are easily achieved by using the data move (DMOV) instruction. PDEL1 is calculated after the demodulator product operation and is not used until the next sample period, a delay of one sample period.

For the low-frequency carriers of the V.21 and Bell 103 standards, a second delay is required and is implemented as DMOV PDEL1, moving the contents of PDEL1 into data memory PDEL2.

When the sample delayed signal (PDEL1 or PDEL2 for the high- or low-frequency carriers, respectively) is generated, it is multiplied by the most recent sample AGCOUT. The product of the multiply is stored in data memory location PROD. PROD is multiplied by GAIN and then filtered by a second-order direct-form, lowpass IIR filter, and the result is stored in location LPFOUT. Further information on digital filters can be found in [12], [13].

Given the lowpass filter output LPFOUT, the FSK demodulator must now estimate the value of the received signal.

In the Data Estimation routine, the following memory location addresses are called:

- BDATA** — The data estimation for the previous baud.
- FSKDAT** — Data estimation of the current sample.
- BAUDCK** — A record of the number of samples presently taken in the current baud. Recall that the sample rate is 9.6 KHz and the baud rate is 300 Hz; so there are 32 samples/baud.
- COUNTR** — The data estimations of each sample in the current baud are compared to the decision of the previous baud. If these are different, then COUNTR is incremented. If COUNTR reaches 32 before BAUDCK reaches 32, it is assumed that a data transition has occurred, and BDATA is set to the opposite value:

$$\text{BDATA}(N+1) = \text{ABS}[\text{BDATA}(N) - 1]$$

Figure 9 is a flowchart of the data decision source code implementation.

AGCOUT - RECEIVED SAMPLE $t = nT$
 PDEL0 - AGCOUT @ $t = (n-1)T$
 PDEL1 - AGCOUT + BI + PDEL0
 PDEL2 - PDEL1 @ $f = (n-1)T$

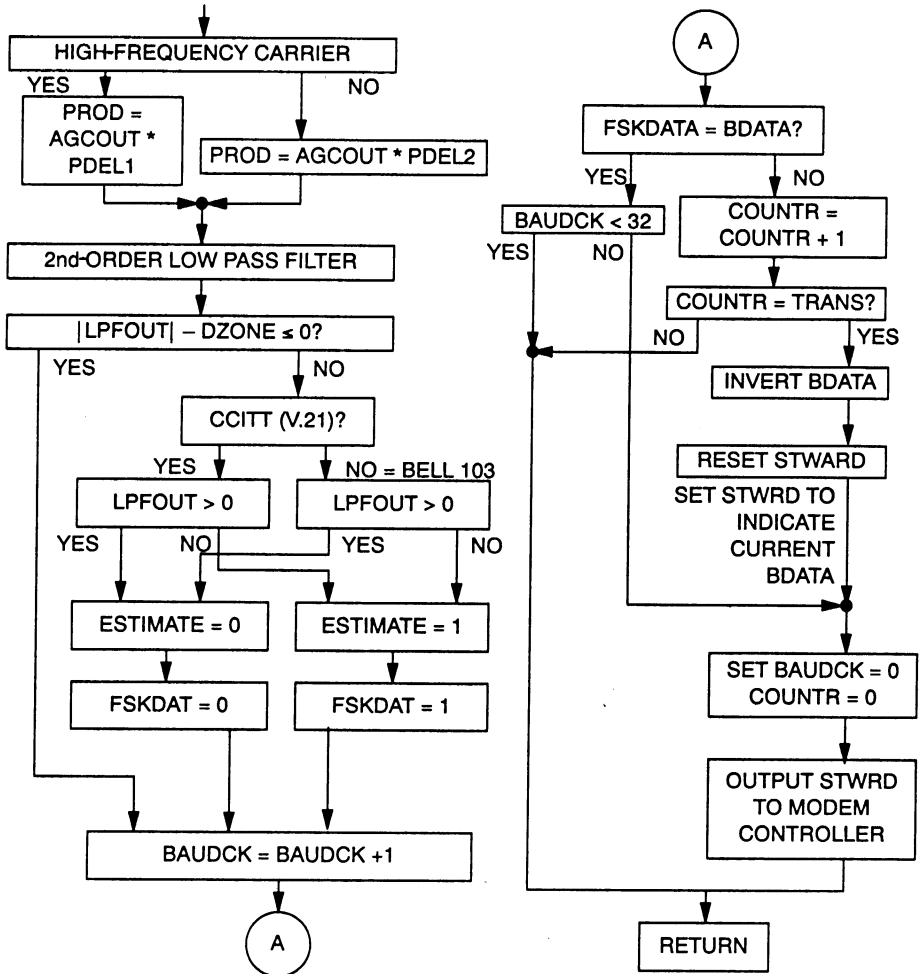


Figure 9. Data Decision Algorithm Flowchart

The function of the automatic gain control subroutine AGC is to compensate for amplitude distortions introduced by the telephone system, etc. References [5], [14] provide additional information on AGC.

Incorporating Additional Functions into the DSP

One of the important tasks the designer faces is incorporating value-added software functions into the DSP source code found in Appendix B.

The software presented here uses only 1.1 Kwords of the 4 Kwords of maskable ROM available on the TMS320C17. This provides you with a significant amount of code space to implement value-added functions.

This software offers a number of hooks that facilitate the easy inclusion of additional software. Note in Table 3 (Modem Controller Commands for the DSP), that the following commands are presently reserved : E, C, B, A, 6, 4, 2, 1, and 0. Each of these commands have bits 0 through 3 undefined. All of these commands can be used by the designer to call additional functions.

You must ensure that the correct modifications are made to the modem controller and modem DSP software. The DSP control command interpreter (CCI) must be modified to recognize and respond to the new commands. The additional functions should be implemented in either a new or the appropriate existing subroutine. The option indicating to the main program that the new subroutine should be called, needs to be provided. This can be done using the STATUS register, or you can define a new register.

You must also ensure that the XDATA word will indicate the present status of the DSP to the modem controller. There are presently a number of unused bits in the XDATA word, so incorporating the modifications in the DSP is straightforward.

Finally, you must ensure that the additional software functions do not exceed the timing requirements imposed by the 9600-KHz sampling frequency.

Conclusions

This application report presented you with the information required to implement a 300-bps V.21/Bell 103 FSK modem based on a TMS320C17 Digital Signal Processor. Both hardware and software issues were discussed. A summary of the FSK modulation and demodulation algorithms and a basic review of modems were also provided. A discussion about incorporation of additional functions and software into the code provided concluded this report.

Appendix A is a derivation of the FSK demodulator fractional delay filter coefficients. Appendix B is the TMS320C17 source code listing.

Acknowledgements

The author wishes to acknowledge the contribution of Dr. Amin Haoni of Technekron, Inc., and George Troullinos, and Raj Chirayil of Texas Instruments. This report is based on their work.

Glossary of Symbols and Abbreviations

- bps — Bits per second
FSK — Frequency shift keying
 ω_c — Carrier signal angular velocity
 $\delta\omega$ — Modulation shift of angular velocity
t — Time
 ϕ — Phase shift
 ω_0 — Angular velocity transmitted to indicate a 0
 ω_1 — Angular velocity transmitted to indicate a 1
 τ — The amount of time the received signal is delayed in the FSK demodulator
 f_0 — Frequency transmitted to indicate a 0
 f_1 — Frequency transmitted to indicate a 1
 f_c — Carrier frequency
 α — Sample fractional delay created by the single FIR filter

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Appendix A

Calculation of Phase Delay Filter Coefficients

A key element of the FSK demodulator implementation is the $\pi/2$ phase delay of the carrier signal. The effectiveness of the demodulator is highly dependent on the accuracy of the $\pi/2$ phase delay.

In a digital system, it is highly unlikely that the time delay required for the $\pi/2$ phase delay is an exact multiple of the signal sampling period. It will be necessary to introduce phase delays that are a fraction of the sampling period.

To accurately generate the fractional delay, the digital signal processor uses a single zero FIR filter. This appendix derives the coefficients for the single zero FIR.

Given the one zero FIR filter shown in Figure A-1:

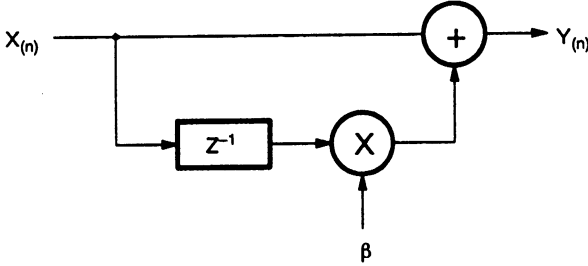


Figure A-1. One Zero FIR Filter.

$$Y(n) = X(n) + \beta X(n-1) \quad (\text{A1})$$

therefore

$$\begin{aligned} Y(z) &= X(z) + \beta * z^{-1} X(z) \\ &= X(z) * (1 + \beta z^{-1}) \end{aligned} \quad (\text{A2})$$

The transform of the filter is $F(z)$

$$F(z) = Y(z)/X(z) = (1 + \beta z^{-1}) \quad (\text{A3})$$

The purpose of this filter is to introduce a precise group delay τ (delay of the signal envelope) to the received signal. τ is defined as

$$\tau = \frac{-d\theta(\omega)}{d\omega} \Delta = \text{group delay} \quad (\text{A4})$$

Evaluate $F(z)$ at $z = e^{j\omega}$ to obtain the frequency response.

$$F'(\omega) = F(e^{j\omega}) = 1 + \beta e^{-j\omega} \quad (\text{A5})$$

$$F'(\omega) = R(\omega) + jI(\omega) = A(\omega)e^{j\phi(\omega)} \quad (\text{A6})$$

Where $R(\omega)$, $I(\omega)$, $A(\omega)$, and $\phi(\omega)$ are real functions of ω .

$$A(\omega) = |F'(\omega)| = [R(\omega)^2 + I(\omega)^2]^{1/2} \quad (\text{A7})$$

and

$$\phi(\omega) = \arctan (I(\omega)/R(\omega)) \quad (\text{A8})$$

Given

$$e^{-j\omega} = \cos\omega - j\sin\omega \quad (\text{A9})$$

Substituting (A9) into (A5)

$$F'(\omega) = 1 + \beta \cos\omega - j\beta\sin\omega \quad (\text{A10})$$

From (A6), (A8), and (A10)

$$\phi(\omega) = \left(\arctan \frac{-\beta\sin\omega}{1 + \beta \cos\omega} \right) \quad (\text{A11})$$

Substituting (A11) into (A5)

$$-d\phi(\omega) = \frac{d}{d\omega} \left(\arctan \left(\frac{-\beta\sin\omega}{1 + \beta\cos\omega} \right) \right) \quad (\text{A12})$$

now

$$\frac{d}{dx} (\arctan (u)) = \frac{1}{1 + u^2} * \frac{du}{dx} \quad (\text{A13})$$

therefore

$$\tau = \frac{-1}{1 + \left(\frac{-\beta\sin\omega}{1 + \beta\cos\omega} \right)^2} * \frac{d}{d\omega} \left(\frac{-\beta\sin\omega}{1 + \beta\cos\omega} \right) \quad (\text{A14})$$

$$\begin{aligned} &= \left(\frac{-(1 + \beta\cos\omega)^2}{1 + \beta^2 + 2\beta\cos\omega} \right) * \left(\frac{-\beta\cos\omega - \beta}{(1 + \beta\cos\omega)^2} \right) \\ &= \frac{+\beta(\beta + \cos\omega)}{1 + \beta^2 + 2\beta\cos\omega} \end{aligned} \quad (\text{A15})$$

Assuming τ is expressed in terms of sample delays D

$$D = \frac{+ \beta (\beta + \cos\omega)}{(1 + \beta^2 + 2 \beta \cos\omega)} \quad (\text{A17})$$

Rearranging (A17) and using the quadratic equation to solve for

$$\beta = - \frac{(1-2D)\cos\omega \pm ((1-2D)^2\cos^2\omega + 4D(1-D))^{1/2}}{2(1-D)} \quad (\text{A18})$$

Given the desired group delay D , and the frequency $f = \omega/2\pi$ (where $\omega = (1080/9600)2\pi$), the filter coefficient β can be determined using equation (A18).


```

*****
* DTMF TONE TABLE:
*
* FIRST ENTRY REPRESENTS LOW FREQUENCY
* SECOND ENTRY REPRESENTS HIGH FREQUENCY
*
* DELTA = (F / F ) * N
*           S
*
* WITH N = 256 TABLE SIZE
* F = 9600 HZ
* S
* F = FREQUENCY OF INTEREST
*
*****
* DATA FORMAT IS S7.8 TO BE AS STEP SIZE. THE TABLE ENTRIES ARE HOWEVER,
* TREATED AS 16 BIT UNSIGNED INTEGERS. A MULTIPLICATION OF DELTA BY 256
* DOES THE NECESSARY CONVERSION IN FORMATS.
*
*****
* TONTBL: .word 01918h ; 0 LOW FREQ
*          .word 02360h ; LOW FREQ GAIN
*          .word 0290h ; HI FREQ GAIN
*
*          .word 0360h ; 1
*          .word 01296h ; LOW FREQ GAIN
*          .word 0800h ; HI FREQ GAIN
*          .word 0492h ; 2
*
*          .word 01296h ; LOW FREQ GAIN
*          .word 02762h ; HI FREQ GAIN
*          .word 0800h ; 3
*          .word 0492h ; LOW FREQ GAIN
*          .word 0800h ; HI FREQ GAIN
*          .word 0492h ; 4
*
*          .word 01488h ; LOW FREQ GAIN
*          .word 0203Eh ; HI FREQ GAIN
*          .word 0360h ; 5
*          .word 01488h ; LOW FREQ GAIN
*          .word 02360h ; HI FREQ GAIN
*          .word 0420h ; 6
*          .word 01488h ; 6

```

```

.word 02762h ; LOW FREQ GAIN
.word 0360h ; HI FREQ GAIN
*
.word 01688h ; 7
.word 0203Eh ; LOW FREQ GAIN
.word 0260h ; HI FREQ GAIN
*
.word 01688h ; 8
.word 02360h ; LOW FREQ GAIN
.word 0290h ; HI FREQ GAIN
*
.word 01688h ; 9
.word 02762h ; LOW FREQ GAIN
.word 0290h ; HI FREQ GAIN
*
.word 01296h ; A
.word 028C0h ; LOW FREQ GAIN
.word 0492h ; HI FREQ GAIN
*
.word 01488h ; B
.word 028C0h ; LOW FREQ GAIN
.word 0492h ; HI FREQ GAIN
*
.word 01688h ; C
.word 028C0h ; LOW FREQ GAIN
.word 0492h ; HI FREQ GAIN
*
.word 01918h ; D
.word 028C0h ; LOW FREQ GAIN
.word 0492h ; HI FREQ GAIN
*
.word 01918h ; E (*)
.word 0203Eh ; LOW FREQ GAIN
.word 0360h ; HI FREQ GAIN
*
.word 01918h ; F (*)
.word 02762h ; LOW FREQ GAIN
.word 0360h ; HI FREQ GAIN
*

```

```

*****
* ADDITIONAL TABLES
*****
*.copy "COSINL.A00" ; COSINE FUNCTION TABLE
*****
*
* COSINE LOOKUP TABLE:
*
* 207 ENTRIES OVER THE RANGE [0,PI], THE RESOLUTION OF THE TABLE IS
* THEREFORE:
*
* (180 / 256 ) = 0.703125 DEGREES
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 05C4Fh : word : ANGLE = 218.6719 COSINE = -0.950426
 05C8Fh : word : ANGLE = 219.3750 COSINE = -0.945895
 05CCFh : word : ANGLE = 220.0781 COSINE = -0.941234
 05D0Fh : word : ANGLE = 220.7813 COSINE = -0.936453
 05D4Fh : word : ANGLE = 221.4844 COSINE = -0.931562
 05D8Fh : word : ANGLE = 222.1875 COSINE = -0.926561
 05DCFh : word : ANGLE = 222.8906 COSINE = -0.921460
 05E0Fh : word : ANGLE = 223.5938 COSINE = -0.916259
 05E4Fh : word : ANGLE = 224.2969 COSINE = -0.910958
 05E8Fh : word : ANGLE = 225.0000 COSINE = -0.905457
 05ECFh : word : ANGLE = 225.7031 COSINE = -0.899856
 05F0Fh : word : ANGLE = 226.4063 COSINE = -0.894155
 05F4Fh : word : ANGLE = 227.1094 COSINE = -0.888354
 05F8Fh : word : ANGLE = 227.8125 COSINE = -0.882453
 05FCFh : word : ANGLE = 228.5156 COSINE = -0.876452
 0600Fh : word : ANGLE = 229.2188 COSINE = -0.870351
 0604Fh : word : ANGLE = 229.9219 COSINE = -0.864150
 0608Fh : word : ANGLE = 230.6250 COSINE = -0.857849
 060CFh : word : ANGLE = 231.3281 COSINE = -0.851448
 0610Fh : word : ANGLE = 232.0313 COSINE = -0.844947
 0614Fh : word : ANGLE = 232.7344 COSINE = -0.838346
 0618Fh : word : ANGLE = 233.4375 COSINE = -0.831645
 061CFh : word : ANGLE = 234.1406 COSINE = -0.824844
 0620Fh : word : ANGLE = 234.8438 COSINE = -0.817943
 0624Fh : word : ANGLE = 235.5469 COSINE = -0.810942
 0628Fh : word : ANGLE = 236.2500 COSINE = -0.803841
 062CFh : word : ANGLE = 236.9531 COSINE = -0.796640
 0630Fh : word : ANGLE = 237.6563 COSINE = -0.789339
 0634Fh : word : ANGLE = 238.3594 COSINE = -0.781938
 0638Fh : word : ANGLE = 239.0625 COSINE = -0.774437
 063CFh : word : ANGLE = 239.7656 COSINE = -0.766836
 0640Fh : word : ANGLE = 240.4688 COSINE = -0.759135
 0644Fh : word : ANGLE = 241.1719 COSINE = -0.751334
 0648Fh : word : ANGLE = 241.8750 COSINE = -0.743433
 064CFh : word : ANGLE = 242.5781 COSINE = -0.735432
 0650Fh : word : ANGLE = 243.2813 COSINE = -0.727331
 0654Fh : word : ANGLE = 243.9844 COSINE = -0.719130
 0658Fh : word : ANGLE = 244.6875 COSINE = -0.710829
 065CFh : word : ANGLE = 245.3906 COSINE = -0.702428
 0660Fh : word : ANGLE = 246.0938 COSINE = -0.693927
 0664Fh : word : ANGLE = 246.7969 COSINE = -0.685326
 0668Fh : word : ANGLE = 247.5000 COSINE = -0.676625
 066CFh : word : ANGLE = 248.2031 COSINE = -0.667824
 0670Fh : word : ANGLE = 248.9063 COSINE = -0.658923
 0674Fh : word : ANGLE = 249.6094 COSINE = -0.650022
 0678Fh : word : ANGLE = 250.3125 COSINE = -0.641021
 067CFh : word : ANGLE = 251.0156 COSINE = -0.631920
 0680Fh : word : ANGLE = 251.7188 COSINE = -0.622719
 0684Fh : word : ANGLE = 252.4220 COSINE = -0.613418
 0688Fh : word : ANGLE = 253.1250 COSINE = -0.604017
 068CFh : word : ANGLE = 253.8281 COSINE = -0.594516
 0690Fh : word : ANGLE = 254.5313 COSINE = -0.584915
 0694Fh : word : ANGLE = 255.2344 COSINE = -0.575214
 0698Fh : word : ANGLE = 255.9375 COSINE = -0.565413
 069CFh : word : ANGLE = 256.6406 COSINE = -0.555512
 06A0Fh : word : ANGLE = 257.3438 COSINE = -0.545511
 06A4Fh : word : ANGLE = 258.0469 COSINE = -0.535410
 06A8Fh : word : ANGLE = 258.7500 COSINE = -0.525209
 06ACFh : word : ANGLE = 259.4531 COSINE = -0.514908
 06B0Fh : word : ANGLE = 260.1563 COSINE = -0.504407
 06B4Fh : word : ANGLE = 260.8594 COSINE = -0.493706
 06B8Fh : word : ANGLE = 261.5625 COSINE = -0.482805
 06BCFh : word : ANGLE = 262.2656 COSINE = -0.471704
 06C0Fh : word : ANGLE = 262.9688 COSINE = -0.460403
 06C4Fh : word : ANGLE = 263.6719 COSINE = -0.448902
 06C8Fh : word : ANGLE = 264.3750 COSINE = -0.437201
 06CCFh : word : ANGLE = 265.0781 COSINE = -0.425300
 06D0Fh : word : ANGLE = 265.7813 COSINE = -0.413299
 06D4Fh : word : ANGLE = 266.4844 COSINE = -0.401198
 06D8Fh : word : ANGLE = 267.1875 COSINE = -0.388997
 06DCFh : word : ANGLE = 267.8906 COSINE = -0.376696
 06E0Fh : word : ANGLE = 268.5938 COSINE = -0.364295
 06E4Fh : word : ANGLE = 269.2969 COSINE = -0.351794
 06E8Fh : word : ANGLE = 270.0000 COSINE = -0.339193
 06ECFh : word : ANGLE = 270.7031 COSINE = -0.326492
 06F0Fh : word : ANGLE = 271.4063 COSINE = -0.313691
 06F4Fh : word : ANGLE = 272.1094 COSINE = -0.300790
 06F8Fh : word : ANGLE = 272.8125 COSINE = -0.287789
 06FCFh : word : ANGLE = 273.5156 COSINE = -0.274688
 0700Fh : word : ANGLE = 274.2188 COSINE = -0.261487
 0704Fh : word : ANGLE = 274.9219 COSINE = -0.248186
 0708Fh : word : ANGLE = 275.6250 COSINE = -0.234785
 070CFh : word : ANGLE = 276.3281 COSINE = -0.221284
 0710Fh : word : ANGLE = 277.0313 COSINE = -0.207683
 0714Fh : word : ANGLE = 277.7344 COSINE = -0.193982
 0718Fh : word : ANGLE = 278.4375 COSINE = -0.180181
 071CFh : word : ANGLE = 279.1406 COSINE = -0.166280
 0720Fh : word : ANGLE = 279.8438 COSINE = -0.152279
 0724Fh : word : ANGLE = 280.5469 COSINE = -0.138178
 0728Fh : word : ANGLE = 281.2500 COSINE = -0.123977
 072CFh : word : ANGLE = 281.9531 COSINE = -0.109676
 0730Fh : word : ANGLE = 282.6563 COSINE = -0.095275
 0734Fh : word : ANGLE = 283.3594 COSINE = -0.080774
 0738Fh : word : ANGLE = 284.0625 COSINE = -0.066173
 073CFh : word : ANGLE = 284.7656 COSINE = -0.051472
 0740Fh : word : ANGLE = 285.4688 COSINE = -0.036671
 0744Fh : word : ANGLE = 286.1719 COSINE = -0.021770
 0748Fh : word : ANGLE = 286.8750 COSINE = -0.006769
 074CFh : word : ANGLE = 287.5781 COSINE = 0.008231
 0750Fh : word : ANGLE = 288.2813 COSINE = 0.023032
 0754Fh : word : ANGLE = 288.9844 COSINE = 0.037633
 0758Fh : word : ANGLE = 289.6875 COSINE = 0.051934
 075CFh : word : ANGLE = 290.3906 COSINE = 0.065935
 0760Fh : word : ANGLE = 291.0938 COSINE = 0.079636
 0764Fh : word : ANGLE = 291.7969 COSINE = 0.092937
 0768Fh : word : ANGLE = 292.5000 COSINE = 0.1


```

*
LAC DTFLAG
BNZ ISDTWF
LAC TRP3,13
SACH XOUT
LT XOUT
HPYK 0700h
PAC
SACH XOUT,4
B XOUTWF
*
ISDTWF: .set $
LAC TRP3,15
SACH TRP5
ZALS
CALL SINGEN
ZALS RIFPHS
ANDS RIFRFO
SACH RIFPHS
*
LAC TRP3,15
SACH TRP3
LT TRP5
HPY DTDFL
PAC
LT TRP3
HPY DTDFH
APAC
SACH XOUT,4
*
MOUTWF: .set $
ZALS TRP5
ANDS TRFRQ
SACH TRP5
*
NONE RET
*
.copy "CC10TM.A00" ; INCLUDES CODE FOR DTWF
*****
*
CONTROLLER COMMAND INTERPRETER (CC1)
*
THE FOLLOWING CODE READS A COMMAND FROM THE TMS7062000 ON PORT 5 AND
INTERPRETS IT ACCORDING TO THE RULES SPECIFIED IN THE CONTROLLER-ISP
INTERFACE DOCUMENT. THE 320 READS ONE COMMAND EVERY BRAD PERIOD. THE BRAD
RATE IS INITIALLY SET TO 600, AND THE BRAD CLOCK IS DERIVED FROM THE
SERIAL PORT FR SIGNAL.
*****
*
CC1 IN XDATA,PMS ; READ COMMAND
OCON
LACK AND IDATA
SACH TRP2 ; MASK OFF 4 LSBS OF COMMAND
LACK 090h ; CHECK FOR DTWF
SUB TRP2
BZ DTCONT
*
ZAC ; IF NOT,
DTFLAG ; CLEAR DTWF DIAL FLAG
LAC TRP2,12 ; COMMAND BITS TO ACDH LSBS
SACH TRP2
*****
*
NOW THE ACCUMULATOR VALUE CORRESPONDS TO THE FOLLOWING COMMANDS AND
CORRESPONDING SERVICE SUBROUTINES
*****
*
ACC COMMAND SUBROUTINE
*
Fh PROTOCOL SELECT PROTO
Dh SET OPERATING MODE OPER
*
9h DIAL DTWF DTWF
8h INIT MODE IMODE
7h RCV MODE RMODE
*
5h FSK DATA MODE FSKSET
4h RESET
*****
*
CHECK FIRST IF RECEIVER IS IN DATA MODE. IN WHICH CASE IGNORE ALL
COMMANDS EXCEPT ZIN, IIN, AND 00h.
*****
*
LACK RMASK ; REC. MODE MASK
AND STATUS
SUB ONE,7 ; CHECK IF BITS 7 AND 6 ARE ONES
SUB ONE,6
BZ CC11
*****
*
REC. IN DATA MODE => IGNORE COMMANDS >2
*****
*
LAC TRP2

```

```

*****
*
*   SUB   ONE,2      ; IF COMMAND LARGER THAN X2 EXIT COMMAND
*   BLEZ  CCI1      ; INTERPRETER.
*   RET
*
* *****
*
*   CALL THE APPROPRIATE SERVICE SUBROUTINE (REFER TO CONTROL TABLE).
*
* *****
*
*   CCI1  LACK  CNTRL      ; BASE OF COMMAND TABLE
*         ADD   TRF2      ; ADD COMMAND OP CODE
*         TBLR  TRF2      ; READ ADDRESS FROM TABLE
*         LAC   TRF2      ; LOAD SUB. ADDR. INTO ACC.
*         CALA          ; CALL SERVICE SUBROUTINE
*
*   RET      ; EXIT COMMAND INTERPRETER.
*
* *****
*
*   COMMAND INTERPRETER SUBROUTINES
*
* *****
*
*   PROTOCOL SELECT COMMAND
*
* *****
*
*   PROTO: .set  $
*
* *****
*
*   EXTRACT TWO LSB'S OF COMMAND
*
* *****
*
*   LACK  O3h      ; MASK OFF BITS 2 AND 3 OF COMMAND
*   AND   XDATA
*
* *****
*
*   SET SPEED BITS STATUS REGISTER:
*
*   BITS 1 AND 0 = 00 FOR 300 BPS (FSK)
*               = 01 RESERVED
*               = 10 RESERVED
*               = 11 RESERVED
*
* *****
*
*   LACK  TRF1
*   AND   STATUS   ; ZERO BITS 0 AND 1
*   SACL  STATUS

```

```

*****
*
*   DETERMINE FSK FREQUENCIES AND SET BAUD COUNTER, ALSO SET OTHER FSK
*   SIGNAL PROCESSING PARAMETERS
*
* *****
*
*   PROTO2 LACK  31      ; BAUD COUNTER IS 32
*         SACL  SINT
*
*   LAC   ONE,2
*   AND   XDATA
*   SACL  CCITT
*
*   LAC   ONE,3
*   SACL  FSKFLG
*
* *****
*
*   ACCUMULATOR NOW CONTAINS THE NUMERAL 8 LOGICAL AND HENCE IDENTIFIES
*   ORIGINATE./ANSWER MODES
*
* *****
*
*   AND   XDATA
*   OPLAG ; ISOLATE ORIGINATE./ANSWER BIT
*         ; SET OPLAG 0 IN ANSWER MODE = 0 IN
*         ; ORIGINATE MODE
*         ; MASK TWO LSB'S OF COMMAND
*
*   LACK  O3h
*   AND   XDATA
*   SACL  TRF1
*   LACK  FSKTBL
*   ADD   TRF1
*   SACL  FIADD
*   ADD   ONE
*   SACL  FOADD
*   ADD   ONE
*   TBLR  BIFSK
*   AND   ONE
*   TBLR  GAIN
*   SUB   ONE
*   SACL  TRF1
*
* *****
*
*   SET FSK TIMING RECOVERY PARAMETERS.
*
* *****
*
*   LACK  O3h      ; ACC = 12
*   SACL  TRANS    ; TRANS = 12
*
* *****
*
*   SET FSK RECEIVE FILTER COEFFICIENTS AND SLICER DEAD ZONE

```

```

*****
*                               ; LOAD ADDRESS OF A1 COEFFICIENT
*                               ;
* LACK FSKA1
* TLBR AF5K
* AOD ONE
* TLR AZ5K
* TLR AZ5K
* LACK ZONE
* TLBR DZONE
* TLBR DZONE
*                               ; DECISION
*                               ;
*****
*                               ; NOW CHECK FOR ANALOG LOOPBACK. IF IT IS IN ANALOG LOOPBACK MODE, THEN WE
*                               ; NEED TO MODIFY THE RECEIVER PARAMETERS TO CONFIGURE RECEIVER IN THE SAME
*                               ; BAND AS THE TRANSMITTER.
*                               ;
*                               ;
*                               ;
* LACK ANSK
* AND STATUS
* BZ PROTUS
*                               ; STATUS BIT IS 1 FOR ANALOG
*                               ; AND ZERO OTHERWISE
*                               ;
*****
*                               ; CHECK IF ANSWER OR ORIGINATE. IF IN ORIGINATE MODE THE THE RECEIVER MUST
*                               ; ALSO BE CONFIGURED FOR LOW BAND. IN WHICH CASE THE PARAMETERS REQUIRED
*                               ; ARE AT ADDRESS TMP1+8. IF IN ANSWER MODE, THE RECEIVER MUST BE PUT IN HIGH
*                               ; BAND AND THE PARAMETERS ARE AT ADDRESS TMP1-8. (PLEASE REFER TO THE
*                               ; FSKTBL)
*                               ;
*****
*                               ;
*                               ; CHECK ORIG/ANS BIT 3 OF XDATA
*                               ;
* LACK G8N
* AND XDATA
* BZ PROTUS
*                               ;
* LACK 0
* SACL OAF8G
* LAC TMP1
* SUB ONE,3
* B PROT07
*                               ;
*                               ; IN ANSWER MODE SUBTRACT 8 FROM TMP1
*                               ;
*****
*                               ; WE'RE IN ORIGIN MODE.
*                               ; SET OAF8G 0 FOR LOWBAND
*                               ; IN ORIGINATE MODE ADD 8
*                               ; TO TMP1 (THIS ONLY HAPPENS IN ANALOGP)
*                               ; READ B1 COEFF
*                               ; READ GAIN
*                               ;
* PROT06 LACK 8
* SACL OAF8G
* LAC TMP1
* AND AND
* AND AND
* TLBR B1FSK
* TLBR ONE
* TLBR GAIN
* PROT07
*                               ;
* PROT06 LACK 0
* SACL TMP0
* LACK TONR0
* AOD ADD
* TLBR TIFR0
* AND ONE
* TLBR RUFRO
* AND ONE
* TLBR DTFFL
* AND ONE
* TLBR DTFFH
*                               ;
*****

```

```

* SELECT GUARD TONE
* GUARD RET
*                               ;
*                               ; SET OPERATING MODE
*                               ;
* OPER LWR5K ; ZERO ANALOG LOOPBACK
* AND STATUS ; LOC. DIG. LOOPBACK BITS
*                               ;
*****
*                               ; CHECK OPERATING MODE
*                               ;
* LACK G8N ; MASK OFF BITS 2 AND 3 OF COMMAND
* AND XDATA ; IF ZERO => LINE MODE (RET)
* BZ OPER1 ;
* SUB ONE
* BZ ANLB ; IF ONE => ANALOG LOOPBACK
* RET
*                               ;
* LACK ANSK ; SET ANALOG LOOPBACK
* OR STATUS ; STATUS BIT
* SACL STATUS
* RET
*                               ;
*****
*                               ; DIAL DTFH
*                               ;
* DTFH SET-UP ROUTINE ; LOOKUP THE LOW AND HIGH FREQUENCIES CORRESPONDING
* TO EVERY DIGIT AND PLACE IN TIFR0 AND RUFRO RESPECTIVELY.
*                               ;
*                               ;
* DTFH LACK 15 ; MASK FOR ISOLATING THE DIGIT
* AND XDATA
* SACL TMP0
* LACK TONR0 ; STORE AWAY TEMPORARILY
* AOD ADD ; BRING IN BASE ADDRESS OF TONE TABLE
* TLBR TONR0,2 ; LEFT SHIFT IS REQUIRED AS THERE ARE FOUR
* ; ENTRIES PER DIGIT
* TLBR TIFR0 ; READ LOW FREQ INTO TIFR0
* AND ONE ; INCREMENT POINTER TOWARDS HIGH FREQ
* TLBR RUFRO ; READ HIGH FREQ INTO RUFRO
* AND ONE ; READ IN LO FREQ GAIN
* TLBR DTFFL ; READ IN HI FREQ GAIN
* AND ONE ;
* TLBR DTFFH ;
*                               ;
*****

```

```

*****
LAC ONE ; SET DTRF DIAL MODE FLAG
SACL DTRFLAG
RET
*****
TRANSMITTER MODE SELECT
*****
MODE 03h ; MASK OFF BITS 2 AND 3
AND XDATA ; SAVE MODE BITS TO SET STATUS
SACL TWP1 ; CHECK IF TRANSMIT ANSWER TONE
SUB ONE
BNZ XMODE1
*****
FOR ANSWER TONE, LOAD TONE FREQ IN TIFR0 LOCATION AND 0001h IN XBITS
LOCATION IN RAM, AND CALL FSK SUBROUTINE WHICH WILL TRANSMIT TIFR0 (I.E.
(THE ANSWER TONE)).
*****
MODE 01h
SACL XBITS ; ADDRESS OF 2100 ANS. TONE
LACK FZ1
TLR TIFR0 ; DETERMINE ANS. TONE FREQ.
LACK 0ch ; IF 0 => 2100 IS RIGHT
AND XDATA ; OTHERWISE LOAD TIFR0 REG WITH 2225
BL XMODE2 ; ANSWER TONE PHASE INC.
*****
LACK FZ2
TLR TIFR0
B XMODE2
*****
CHECK FOR REMOTE DIGITAL LOOPBACK
*****
MODE1 SUB ONE 1 ; SUBTRACT 2 MORE FROM TWP1
BNZ XMODE2 ; IF ZERO => REM. DIG. LOOPBACK
*****
HANDLE ROL: (ASSUME THAT THE RECEIVER IS ENABLED)
PLACE RECEIVED QUABITS IN XBITS. CHECK FOR 1200 BPS OPERATION. IF SO
FORCE A 1 INTO LSB OF XBITS. SET BITS 5 & 4 IN STATUS = 10. PLACE
RECEIVED QUABITS IN XBITS
*****
LACK ONE ; MASK OFF QUABITS
AND STMRD
SACL XBITS ; STORE AWAY
*****
CHECK FOR 1200 BPS OPERATION
*****
MODE 00h ; MASK FOR SPEED BITS
AND STATUS ; SPEED BITS
SUB ONE 1 ; CHECK FOR 10
BNZ XMODE2 ; IF NON-ZERO, JUST CONTINUE
*****
LAC XBITS ; ADD A 1 TO LSB FOR 1200 BPS OPERATION
ADD ONE
*****
SET THE TRANSMITTER MODE BITS IN STATUS REGISTER.
*****
MODE2 LACK NTXMSK ; NEGATION OF TRANSMISSION BITS MASK
AND STATUS ; ZERO THE TX STATUS BITS
ADD TWP1 TUSH ; ADD TX STATUS BITS IN RIGHT POS.
SACL STATUS
RET
*****
RECEIVER MODE SELECT
*****
SET THE RECEIVER STATUS BITS (BITS 6 AND 7) OF STATUS REGISTER TO:
00 IF RECEIVER IS IDLE
01 FOR CALL PROGRESS MONITORING
10 FOR DATA MODE
*****
MODE 03h ; MASK OFF BITS 2 AND 3
AND XDATA
SACL TWP1
LACK NRCRMSK ; NEG. OF REC. BITS MASK
AND STATUS ; ZERO REC. STATUS BITS
ADD TWP1 RCRSH ; ADD REC STATUS IN RIGHT POS.
SACL STATUS
MODE1 RET
*****

```

```

*****
*   FSK DATA MODE
*
*   SET UP FSK TRANSMIT FREQ ACCORDING TO THE TX DATA
*
*****
*
*   FSKSET      8      ; CHECK THE TRANSMITTED BIT
*   AND
*   DATA0      ; IF ZERO, DATA MUST BE 0
*   BZ          ; POINT ACC TO 1 FREQ
*   LAC         ; SET TX FREQ TO APPROPRIATE 1 FREQ
*   F1AND      T1FR0
*   T1LR       RET
*
*   DATA0     LAC      F0AND      ; POINT ACC TO 0 FREQ
*   T1LR       T1FR0     ; SET TX FREQ TO APPROPRIATE 0 FREQ
*
*   MFSK
*
*****
*   RESET AND EQUALIZER ENABLE ROUTINES
*
*****
*   RESET      LAC      081h
*   S1AND     S1AND
*   OUT      S1AND.PHS
*
*   B          START
*
*****
*   END CONTROLLER COMMAND INTERPRETER SUBROUTINES
*
*****

```

```

*****
*   .COPY      "SINEM.A00"
*
*****
*   SUBROUTINE : SINEM
*
*   PURPOSE : SINE GENERATION
*
*   TASK : GIVEN A COSINE TABLE WITH 257 VALUES AND START ADDRESS COSOFF, AND
*   GIVEN AN ANGLE INDEX IN THE ACCUMULATOR, DETERMINE THE SINE OF THE ANGLE.
*
*   ENTRY CONDITION : THE ANGLE INDEX MUST BE IN THE LOWER ACCUMULATOR.
*
*   EXIT CONDITION : THE SINE OF THE ANGLE IS RETURNED IN TEMPORARY LOCATION
*   T1P3.
*
*   DESCRIPTION : THE COSINE LOOKUP TABLE CONTAINS 257 VALUES WITH:
*
*   COS(0) = 1.0 AND COS(256) = -1.0
*
*   HENCE ANGLE INDEX 0 HOPS TO ANGLE 0 AND ANGLE INDEX 256 HOPS TO PI. THE
*   SINE VALUE IS GENERATED BY SUBTRACTING FROM THE ANGLE INDEX THE INDEX
*   CORRESPONDING TO PI/2, TAKING THE ABSOLUTE VALUE, AND HENCE FORMING AN
*   ADDRESS INTO THE LOOKUP TABLE.
*
*   NO OF CYCLES: 17
*
*   NO OF STACK LEVELS USED: 1
*
*   THE ANGLE INDEX IS THE LOWER ACCUMULATOR
*
*   ANGLE INDEX HAS S15.0 FORMAT. MUST SUBTRACT PI/2 VALUE WHICH LAYS AT THE
*   MIDDLE OF THE TABLE AND HAS SS14.0 FORMAT AS VIEWED IN S15.0 FORMAT
*
*****
*   SINEM      SUB      ONE.14      ; SUBTRACT INDEX OF PI/2
*   SACL       T1P3      ; PUT AWAY TEMPORARILY
*   ZALH      T1P3      ; PREPARE FOR ABSOLUTE VALUE
*   ABS       T1P3      ; TAKE ABSOLUTE VALUE
*   SACH      T1P3      ; PUT AWAY BEFORE RIGHT SHIFT
*
*****
*   THE VALUE STORED IN T1P3 HAS S15.0 FORMAT -- ALBEIT A POSITIVE NUMBER
*
*   A LEFT SHIFT OF 9 BITS CORRESPONDS TO SS24.0 FORMAT AND SHIFTING THE HIGH
*   ACCUMULATOR HAS A SS8.0 FORMAT
*
*****
*   LAC      T1P3.9      ; ISOLATE 8 HSB'S IN HIGH ACC
*   SACH     T1P3        ; PUT AWAY THE 8 HSB'S TEMPORARILY
*
*****

```

```

*****
* THE NEXT THREE INSTRUCTIONS ELIMINATE ANY SIGN EXTENSION BITS THAT MIGHT
* HAVE PROPAGATED
*
*****
*
* LAC   TMP3
* ABS
* SACL  TMP3
*
*****
*
* FORM THE FINAL LOOK-UP ADDRESS
* BRING IN THE ADDRESS OFFSET.
* THE BASE ADDRESS IS IN 888.0 FORMAT, WHILE THE INDEX IS ALSO IN 888.0
* FORMAT.
*
*****
*
* LACK  COSOFF
* ADD   TMP3      ; FORM FINAL LOOK-UP ADDRESS
* TBLR  TMP3      ; READ SAME VALUE INTO TMP3
*
* RET
*
*****
*
* FSX DEMODULATION FILES
*
*****
*
* .copy "RSTSG-A00"
*
*****
*
* DATE: 5-29-86
* SUBROUTINE: RSTSK
* INCLUDES FSX RECEIVING/TXING RECOVERY
* PURPOSE: RECEIVER PER SAMPLE TASK
*
* TASK: THIS SUBROUTINE COMBINES SMALLER MODULES TO PERFORM THE SIGNAL
* PROCESSING FUNCTIONS THAT ARE REQUIRED ON A PER SAMPLE BASIS
* (9600 Hz).
*
* ENTRY CONDITION: THE RECEIVED S/M SAMPLE IS IN REG LOCATION R1N.
*
*****

```

```

*
* RSTSK: .set $
* LAC   R1N      ; INPUT 14-BIT S/M SAMPLE
* SACL  TMP1     ; ARL INTO TMP1
*
*****
*
* USE HIGH PASS FILTER, MAKE SURE INCOMING SAMPLE HAS NO SHIFT.
*
*****
*
* LAC   TMP1,0   ; ARL
*
*****
*
* HIGH PASS FILTER THE INPUT
*
*****
*
* MUP: .set $
* LRPK  1
* SACL  X1
* ZALS  STLSB
* ANDH  ST
* SUB   ST,TAU
* ANDH  X1,X1,TAU-1
* SUB   X1,TAU-1
* SUBH  X2,X2,TAU-1
* AND  X2,TAU-1
* SACL  STLSB
* SACH  ST
* DMOV  X1
* LRPK  0
* SACH  TMP1
*
*****
*
* MUP LEAVES THE SAMPLE IN TMP1. MULTIPLY IT BY ACC GAIN ALPHA. THE OUTPUT
* FORMAT IS S.111 REQUIRING SOME MANIPULATIONS
*
*****
*
* LT   TMP1      ; MULTIPLY BY ACC WORD
* RPY  ALPHA
* PRC
*
*****
*
* SHIFT ACCUMULATOR EIGHT 4 TIMES BEFORE STORING
*
*****
*
* SACL  TMP0
* SACH  TMP1
*
*****

```

```

LAC      TMP0,8
SACH     TMP0
LAC      ONE,8
SUB      ONE
AND      TMP0
SACL     TMP0
LAC      TMP1,8
ADD      TMP0
SACL     TMP1
*****
; IN BOTH TMP1 AND TMP2 UPDATE THE SIGNAL POWER ESTIMATE AWESOR
AWESOR = AWESOR + TMP1*2
AWESOR IS ZEROED BY THE AGC ROUTINE ONCE PER BAUD.
*****
LAC      TMP1,15
SACH     TMP0
LT       TMP0
MPY      TMP1
PAC      AWESOR
ADDH    AWESOR
SACH     AWESOR
*****
; INCREASE SIGNAL ENERGY BY A FACTOR OF 4 FOR COMPATIBILITY WITH THE REST
; OF THE RECEIVER
*****
LAC      TMP1,1
SACL     TMP1
SACL     TMP2
*****
; CHECK FOR FSK OPERATION
AND      3
LAC      STATUS
LT       TMP1
MPYK    013h ; ASSUME V,21
LAC      CCITT
BNZ     VZLONG ; MULTIPLY BY 2.5
MPYK    018h ; MULTIPLY BY 3.0
PAC
VZLONG
SACL     TMP0
SACH     TMP1
LAC      TMP0,13
SACH     TMP0
LAC      ONE,13
SUB      ONE
AND      TMP0
SACL     TMP0
SACL     TMP1,13
ADD      TMP0
SACL     AGCOUNT
CALL     RFSK
RET
      .copy      *FIDECO.A00*
*****
; DEMODULATOR SECTION
; THIS DESIGN IMPLEMENTS A DELAY OF 5(P1)/2
; AGC
; FSK DEMODULATOR
; MEMORY CONFIGURATION: (CONSECUTIVE ADDRESSES)
AGCOUNT
PIELO
PIEL1
PIEL2
LPIEL0
LPIEL1
LPIEL2
*****
RFSK     SAWN ; SET OVERFLOW MODE
*****
; TAKE PRODUCT FOR PRODUCT DEMOD SCHEME. ASSUME ANSWER MODE (2 SAMPLES)

```

```

*****
* GENERATE THE EXACT DELAY REQUIRED FOR RECEIVER.
*
*
*
*
*****

```

```

LAC   ACCOUT,15      ; PREPARE FOR FIR ACCUMULATION
LT    PLEVEL        ; STATE OF ONE ZERO FIR FILTER
MPY   B1FSK         ; MULTI BY COEFFICIENT
APAC  B1            ; OUTPUT OF ONE ZERO FIR FILTER
BV    RFLAG         ; RESET OVERFLOW FLAG

RFLAG .set $
SACH  PLEVEL,1     ; STORE AT NEXT STAGE OF DELAY FILTER
DMOV  ACCOUT       ; SHIFT SAMPLE IN FILTER

*****

```

```

* PREPARE TO LOW PASS FILTER THE PRODUCT.
*
*
*
*
*****

```

```

ZAC   PROD          ; 2ND ORDER DIRECT FORM LP FILTER
LT    GAIN          ; 500 HZ, 0.25 DB RIPPLE
ADD   LPEL1,15     ; COEFFICIENTS:
LTA   LPEL1        ; A1 = 1.392 = 1.0 * 0.392
MPY   A1FSK       ; A2 = -.562
LTA   LPEL2       ; B0 = 1
MPY   A2FSK       ; B1 = 2
APAC  B2          ; B2 = 1
SACH  GAIN,1      ; GAIN = 1 HIGH BAND
      GAIN,0.5    ; GAIN = 0.5 LOW BAND

*****

```

```

OVRFLW .set $
ZAC   LPEL0,14    ; CLEAR DELAY LINE
ADD   LPEL1,15   ; LPEL1 = 1 LPEL1
ADD   LPEL2,14   ; LPEL2 = 1 LPEL2
BV    OVRFLW
B     NOVRFL
      $
NOVRFL .set $
SACH  LPEL1      ; STORE FILTERED
OUT   LPEL0,1   ; LPEL0 = 1 LPEL0
DMOV  LPEL1
      LPEL0

*****

```

```

*****
* LOAD I WITH AGE STAGE OUTPUT
* TAKE PRODUCT WITH DELAY LINE OUTPUT
*
*
*
*
*****

```

```

LTA   ACCOUT,15   ; ORIGINAL/ANSWER FLAG = 0 WHEN TX ORIGINATES THE CALL HENCE RX RECEIVES
      IN THE HIGH BAND

LAC   OVRFLAG     ; CHECK FOR HIGH BAND/LOW BAND
BNZ   ANSWER     ; LOW BAND, DONE.
MPY   PLEVEL     ; HIGH BAND; USE ONE LESS SAMPLE DELAY
PAC   PROD,1     ; ACCUMULATE THE PRODUCT OUTPUT
SACH  PROD,1     ; STORE IN PROD (1,15)

*****

```

```

* PRODUCT DEMOD DELAY LINE -----> FOR HIGH BAND
* ACCOUT--->: 1 ZERO FIR FILTER ;--->: Z++-1 ;--->: Z++-1 ;--->: FOR LOW BAND

PRODUCT = ACCOUT + OUTPUT OF DELAY LINE
PRODUCT IS LOWPASS FILTERED AND IT'S SIGN INDICATES 0 OR 1 DATA...

*****

```

```

* ONE ZERO FILTER TO WOP-UP PHASE SHIFT OF FLAT DELAY LINE TO BE PI/2 IN
* PRODUCT FSX DEMODULATOR:
* COEFFICIENTS FOR ZERO: (B1)

```

```

      BELL 103:      GAIN 103:
1170 HZ 0.07175    0.57731
2125 HZ 0.31678    1.0
      V-21 :      GAIN V21:
1080 HZ 0.32796    0.69753
1750 HZ 0.46889    1.0

START UPDATING THE DELAY LINE

*****

```

```

* DMOV PLEVEL ; START SHIFTING DATA IN DELAY LINE
*
*
*
*
*****

```



```

RET
*****
ASC FILES
*****
      .copy "ASC.A00"
*****
ASC.ASM
      FRONT END ASC FUNCTION.
      THIS ASC WAS REDESIGNED TO INCORPORATE THE FREEZE OF EQUALIZATION 5/29/87
      THE AVERAGE SIGNAL SQUARED IS COMPUTED BY THE MAIN PROGRAM AND STORED IN
      ARESOR, WHICH IS CLEARED BY THIS ROUTINE AFTER ARESOR IS USED. THE
      ROUTINE USES A WINDOW whose WIDTH DEPENDS ON THE MODULATION (1200, 2400)
      AND AN ERROR WEIGHTING WHICH ALSO DEPENDS ON THAT RATE. WE FIRST SET
      THOSE VALUES:
*****
ASC
      SOWN
      LAC      ON      ; CHECK FOR AFE SWITCHING
      BNZ      SWITCH
*****
      CHECK IF 2400 AND CHANGE THOSE VALUES
*****
      LACK      3
      AND      STATUS      ; IF STATUS BITS 0 AND 1 > 2 => 2400
      SUB      ONE,1
      BLEZ     ASCO
      ; IF <= 2 , DO NOT MODIFY TPO AND TFP1
*****
      FOR 2400 , 2 -> TPO AND 1320 -> TFP1
*****
      LACK      2
      SACL     TPO
      LT       ONE
      BPTK     1320
      PAC
      SACL     TFP1
      B
*****
      ; IT IS 1200
      ; WEIGHTING FACTOR -> TPO
      ; WINDOW -> TFP1
*****
      NOW SUBTRACT REFERENCE FROM BAUD ENERGY TO GET ERROR. THE BAUD ENERGY IS
      IN SIO.3 FORMAT. THE ASC MAINTAINS THAT LEVEL AT 2.86416 = 44.7 (H*586
      IN SIO.5), THE ACRF IS THEREFORE H*586
*****
      LAC      ARESOR
      BEEZ     CONT1
      LAC     ONE,15
      SUB     ONE
      LT      ONE
      BPTK    ACRF
      SPKC
*****
      ; FOR NEGATIVE ENERGY SET TO MAX POSITIVE
      ; ENERGY LEVEL - FORCED SLEN MODE
      ; ACRF = H*586
      ; ARESOR - ACRF -> ACC
*****
      COMPARE THE ERROR TO WINDOW (TFP1).
      IF ERROR > WINDOW => ERROR - WINDOW -> ERROR
      IF -WINDOW < ERROR < WINDOW => 0 -> ERROR
      IF ERROR < -WINDOW => TPO + (ERROR + WINDOW) -> ERROR
*****
      IF THE AVERAGE BAUD ENERGY IS A, THE PEAK BAUD ENERGY FOR QAM SIGNALS IS
      1.8 A AND THE MINIMUM IS 0.2 A. THE WINDOW IS THEREFORE CHOSEN TO BE 0.8
      A IN EITHER DIRECTION. WITH ACRF = H*586, THE WINDOW IS H*492. FOR DPSK
      SIGNALS, THE VARIATIONS IN BAUD ENERGY ARE ENTIRELY DUE TO ISI AND
      DISTORTION AND THEREFORE THE WINDOW IS MUCH SMALLER (H*41). FIRST CHECK IF
      ERROR < WINDOW
*****
      SUB     TFP1
      SACL     TFP3
      BEEZ     ASC2
      ; ERROR - WINDOW -> TFP3
*****

```

```

*****
* ERROR < WINDOW > CHECK IF ERROR > -WINDOW, IN WHICH CASE, ZERO THE
* ERROR, FIRST, ZERO THE ERROR (I.E. ASSUME ERROR > -WINDOW) AND MODIFY IF
* WRONG ASSUMPTION.
*****
*
* LACK ARI,0
* SAR ARI,TMP3 ; ASSUME ERROR > -WINDOW
*****
*
* CHECK ASSUMPTION
*****
*
* ADD TMP1,1 ; ERROR + WINDOW -> ACC
* BEEZ ACC2 ; ASSUMPTION IS RIGHT
*****
*
* ERROR < -WINDOW => TMP0+(ERROR+WINDOW) -> TMP3
*****
*
* SACL TMP3
* LT TMP3
* RPY TMP0
* PAC
* SACL TMP3
*****
*
* AT THIS POINT, THE WEIGHTED WINDOWED ERROR IS CONTAINED IN TMP3. WE
* CONSIDER IT AN S.15 NUMBER AND USE IT TO UPDATE THE ACC GAIN ALPHA.
* FIRST, WE DETERMINE WHETHER TO SLEW OR NOT. IF THE ERROR IS LARGER THAN
* LEAK OR SMALLER THAN FE27h, GO INTO SLEWING MODE BY SETTING ERROR TO
* 7FFAh OR 8000h RESPECTIVELY. OTHERWISE, LEAVE IT UNCHANGED.
*
* ALSO SET STATZ(7) APPROPRIATELY TO FREEZE THE UPDATE OF THE EQUALIZER
*
* STATZ(7)=1 UPDATE EQUALIZER
*
* STATZ(7)=0 FREEZE EQUALIZER
*****
*
* ACC2 LAC ONE,7
* OR STATZ ; ASSUME EQUALIZER UPDATE
* SACL STATZ
*****
*
* ACC2 LAC TMP3
* LOPK 1

```

```

SUB POSSM ; DO NOT SLEW
ACC3
BLEZ
LDPK 0 ; ENTER SLEW MODE
LAC ONE,15
SUB ONE
SACL TMP3 ; TMP3 <- 7FFF
*
* LACK 7Fh
* AND STATZ ; FREEZE EQUALIZER UPDATE
* SACL STATZ
* B
*****
*
* ACC3 ADD POSSM ; ACC <- TMP3
* ADD NEGRM
* LDPK 0
* BEEZ ACC4 ; DO NOT SLEW
* LAC ONE,15 ; ENTER SLEW MODE
* ADD ONE
* SACL TMP3 ; TMP3 <- 8000
*
* LACK 7Fh
* AND STATZ ; FREEZE EQUALIZER
* SACL STATZ
*****
*
* THE FOLLOWING LINES UPDATE THE GAIN ALPHA USING AN EXPONENTIAL INTEGRATOR
*
* ALPHA = ALPHA/(1+K*ERROR) (ERROR = TMP3)
*
* WHERE ALPHA IS OF FORMAT S7.8, ERROR IS S0.15, AND K = 0.5.
*
* ALPHA * ERROR: S7.8 * S.15 = S7.24.
*
* BY KEEPING ACC4 WITHOUT LEFT SHIFT THE MULTIPLICATION BY K IS
* ACCOMPLISHED.
*
* ALPHA IS UPPELROUNDED TO .5,73 IN S7.8
*****
*
* ACC4 LACK MAXALP
* TLRB TMP0
* ZALH ALPHA
* LT TMP3 ; ERROR -> T
* RPY ALPHA
* SPC ALPHA (1 - 0.5*ERROR) -> ACC
* SACL ALPHA
*****
*
* CHECK IF ALPHA > MAX ALPHA

```

```

*****
SUBH TPO0
BLZ ACOS
LAC TPO0
SACL ALPHA
*****
* ZERO BAUD ENERGY REGISTER
*****
ACCS: .set $
#HL OUT ALPHA_P42 ; ANL DIAGNOSTIC
ZAC
SACL AVESNR
*****
* ENERGY DETECT LOOP
*****
* START BY READING IN HYSTERESIS COUNTER INCREMENT CONSTANT
*****
LACK HYSINC
TBLR TMS0
*****
* CHECK IF AFE GAIN IS ON OR OFF
*****
EDIT LACK O80h
AND STMRD
BLZ EDIT1
*****
* AFE GAIN IS ON, CHECK IF ENERGY DETECT IS ON (STMRD(G) = 1)
*****

```

```

LAC ONE_6
AND STMRD
BLZ EDIT01
*****
LACK THRES1
TBLR TPO0
LAC TPO0
SUB ALPHA
BLZ EDIT2
*****
* CHECK IF AFE GAIN STAGE SHOULD BE BYPASSED
*****
LACK THRES3
TBLR TPO0
LAC TPO0
SUB ALPHA
BLZ EDIT3
*****
* IS AFE GAIN ON ?
*****
LACK O80h
AND STMRD
BLZ EDIT3 ; IF GAIN IS OFF, EXIT
*****
* BYPASS AFE GAIN
*****
LACK O7Fh
AND STMRD
SACL STMRD
LACK O4h
SACL O4h
RET
*****

```

```

; IF ZERO => ENERGY IS NOT DETECTED =>
; CHECK IF LEVEL IS LARGER THAN ~43.5 DBM
; IF STMRD(G) IS ONE, CHECK IF LEVEL LESS
; THAN ~48 DBM
; IF < 0 THEN NO ENERGY DETECT

```

```

*****
* DECREMENT HYSTERESIS COUNTER
*****
EDT2 BV EDT21 ; CLEAR OVERFLOW BIT
EDT21 ZALH HYST ; HYSTERESIS COUNTER
SUBH TIPS ; TIPS = 1927 = 32768/15
SACH HYST
*****
* IN CASE OF OVERFLOW, DECLARE LOSS OF ENERGY DETECT
*****
BV EDT02
RET ORFH
LACK STMRD AND STMRD
SACL STMRD
RET
*****
* FOLLOWING LINES ARE EXECUTED IF AFE GAIN IS HIGH, BUT NO ENERGY DETECT.
* CHECK IF ALPHA < 21.28 (I.E., RECEIVE LEVEL >= 43.5 DBM) AND INCREMENT
* HYSTERESIS COUNTER IF IT IS, OTHERWISE, EXIT.
*****
EDT01 LACK THRESH ; 21.28 IN 57.8
TBLR TPO TPO
LAC TPO
SUB ALPHA
BLZ EDT3
*****
* ALPHA < 21.28 => INCREMENT HYSTERESIS COUNTER
*****
BV EDT011 ; CLEAR OVERFLOW BIT
EDT011 ZALH HYST
AUBH TIPS ; TIPS CONTAINS INC. X'OF
SACH HYST
*****

```

```

*****
* DETECT BIT STMRD(6) = 1.
*****
BV EDT04 ; IN CASE OF OVERFLOW, SET ENERGY
RET ORFH ONE.6
LAC STMRD OR STMRD
SACL STMRD
RET
*****
* IF AFE GAIN STAGE IS BYPASSED, CHECK LEVEL OF ALPHA
*****
EDT1 LACK THRESH
TBLR TPO TPO
LAC TPO
SUB ALPHA
BLZ EDT3
*****
* IF ALPHA > THRESH (20.09 IN 57.8) THEN TURN AFE GAIN STATUS WORD BIT ON.
*****
LACK ORFH
OR STMRD
SACL STMRD
LACK O14h
SACL O14h
RET
*****
* ROUTINE FOR SWITCHING THE AFE ON/OFF
*****
EDT3 RET
*****

```

```

*****
* ZERO BAD ENERGY REGISTER
*
*****
* SWITCH ZAC SACL AWESNR
*
LACK 010h ; MASK OFF UNWANTED BITS
AND ON
BZ AFEOFF
*
*****
* CHECK IF THE GAIN SHOULD BE ON
*
*****
*
LACK 0Fh ; MASK OFF THE AFE ON BIT
AND ON
SUB 0Eh ; DECREMENT THE COUNTER
BZ SWITCH1
*
SACL ON ; SAVE ON VALUE
LACK 010h ; LOAD THE AFE ON BIT
OR ON
SACL ON ; RESTORE AFE ON BIT
RET
*
SWITCH1 SACL ON ; RESET THE ON VALUE TO ZERO
LACK THRES6 ; LOAD THE NEW ALPHA VALUE
TLR ALPHA ; RESET ALPHA TO 5.05
RET
*
AFEOFF LAC ON ; DECREMENT THE COUNTER
SUB ONE
BZ SWITCH2
*
SACL ON
RET
*
SWITCH2 SACL ON ; LOAD NEW ALPHA VALUE
LACK THRES4 ; RESET ALPHA TO 8.98 IN 57.8
TLR ALPHA
RET
*

```