

Migrating from TMS320VC5410 to TMS320VC5416

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ABSTRACT

This document describes issues of interest related to migration from the TMS320VC5410 to the TMS320VC5416. The objective of this document is to indicate differences between the two devices. Functions that are identical between the two devices are not included. For detailed information on the specific functions of either device, refer to the device data sheets, 5410 (SPRS075), 5416 (SPRS095), the TMS320C54x™ DSP CPU and Peripherals, Reference Set, Volume 1 (SPRS131) and the TMS320C54x DSP Enhanced Peripherals, Reference Set, Volume 5 (SPRU302).

Migration issues from the 5410 to 5416 are indicated with the following symbols:

- S** means software modification is required
- H** means hardware modification is required
- D** means the 5410 and 5416 are different (usually due to added features on the 5416) but no modification is necessary for migration (i.e. different but compatible).

These symbols are included at the beginning of each section.

Revision History:

| Revision | Date | Description |
|----------|----------|---|
| 1.0 | 09/16/99 | Original |
| 1.1 | 09/30/99 | New format |
| 1.2 | 09/20/00 | Add DMA Interrupt Generation in ABU section |
| 1.3 | 12/07/00 | Removal of OSC mode |

Unless otherwise noted, the information contained in this document should be considered **ADVANCE INFORMATION** on new products in the sampling or preproduction phase of development. Information and specifications in this document are subject to change without notice.

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1 Package and Pinout Compatibility [D]

The 5416 is available in two package types:

- 144-pin 'PGE' thin quad flat pack (TQFP)
- 144-pin 'GGU' microstar™ ball grid array (BGA)

While the 5410 is available in two package types:

- 144-pin 'PGE' thin quad flat pack (TQFP)
- 176-pin 'GGW' microstar™ ball grid array(BGA)

The 5416 is pin compatible (same footprint and pinout) with the PGE 5410. Note that there is a "no connect" (NC) pin on the 5410 (PGE pin no. 80). This pin is given a new name (HPI16 pin), and is used to configure the 5416 HPI to either an 8-bit HPI or a 16-bit HPI.

2 Power Supply [H]

The 5410 CVdd operates at 2.5V and DVdd operates at 3.3V, while the 5416 CVdd operates at 1.5V for 120 MHz and 1.6V for 160 MHz, and DVdd operates at 3.3V.

The power-up/power-down sequence on 5416 is different from that of 5410. It is desired to power both supplies simultaneously. If it is impossible to power-up/down the CVdd and DVdd simultaneously, CVdd must be powered up first, DVdd second. For power-down, DVdd must be powered down first, CVdd second.

3 Clock Mode Settings at Reset [D]

The PLL programming and operation of the 5416 PLL is similar to the 5410 but the clock mode settings at device reset is different. Refer to 5410 (SPRS075) and 5416 (SPRS095) data sheet for more details. Note that the 5416 does not support the clock mode of internal oscillator with external crystal.

4 Multichannel Buffered Serial Port (McBSP) [H/S]

The 5416 McBSP slightly differs from the 5410. The 5416 McBSP has been enhanced:

- To allow all 128 channels of a 128-channel bitstream so they can be enabled simultaneously
- To enable the receive clock pin (BCLKR) or the transmit clock pin (BCLKX) to be configured as the input clock to the sample rate generator

Three control bits and twelve registers have been added to enable the 128 channel selection. Refer to the 5416 data sheet (SPRS095) for more details.

5 Host Port Interface (HPI) [H/S]

The 5416 HPI slightly differs from the 5410. In addition to its capability to interface to an 8-bit host, the 5416 HPI has been enhanced so that it can be interfaced to a 16-bit host processor.

16-bit HPI (HPI16) [S/W]

The 5416 host port interface can be configured as an 8-bit HPI (HPI8) or a 16-bit HPI (HPI16) via a dedicated pin, namely pin HPI16, as mentioned above in the Package and Pinout Compatibility section. This pin has an internal pull down resistor. When it is left unconnected or tied to ground, the 5416 HPI is configured as an HPI8. By tying the pin to DVdd, the 5416 HPI is configured as an HPI16 in non-multiplex mode.

The external signals associated with the HPI16 are significantly different from those on the 5416 when HPI is configured as an 8-bit HPI. Refer to the 5416 data sheet (SPRS095) for more details.

Expanded memory map [S]

The 5416 HPI memory map is expanded to 128KW of internal memory. Refer to 5416 data sheet for more details.

6 DMA External and Extended Memory Transfer [S]

The 5416 DMA has external memory access that is implemented differently from the 5410. The 5416 DMA has been enhanced to provide the ability to access to extended external data and IO memory.

Two new bits have been added to the DMA transfer mode control register (DMMCRn) to specify the space (i.e., internal or external access) of the DMA transfer: one for the source and one for the destination. Also two new 7-bit registers are added to specify the extended data and IO pages (page 0 to page 127), one for the source and one for the destination. Refer to the 5416 data sheet (SPRS095) for more details.

7 DMA Expanded Memory Map [S]

In internal access mode, the 5416 DMA memory map is expanded to 128KW of internal program memory. In external access mode, for data, program and IO space, the 5416 DMA memory map is expanded to 8MW (128 64K pages). Refer to 5416 data sheet for more details.

8 DMA Interrupt Generation in ABU [S]

On the 5410, the half buffer interrupt is generated when the next address (in DMSRC for transmission or DMDST for reception) is greater than the halfway point of the transmit/receiving buffer if positive index is used, or when the next address is less than the halfway point when the negative index is used. For odd and even buffers, the interrupt point differs accordingly.

On the 5416, the half buffer interrupt is generated when the next address is equal to or greater than the halfway point if positive index is used, or when the address is less than the halfway point when the negative index is used. For odd and even buffers, the interrupt point differs accordingly. For more info, please refer to sections 3.2.3.8 and 3.2.3.9 in the *TMS320C54x DSP Enhanced Peripherals, Volume 5* (SPRU302).

9 Memory Map [D]

The memory map of the 5416 is similar to the 5410 with following exceptions:

- 64K of additional on-chip SARAM is mapped into addresses 028000h-02FFFFh, and 038000h-03FFFFh in program space in the 5416 is in the micro computer mode.
- The 5416 has a total of 64K (8 8K blocks) DARAM, while the 5410 has 8K (4 2K blocks) DARAM.

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