

How to Begin Development Today With the TMS320C6713 Floating-Point DSP

Dominic Suryabudi
C6000 Applications Team

ABSTRACT

Development can begin now for the Texas Instruments TMS320C6713 highest-performance, peripheral-rich floating-point digital signal processor (DSP) systems. Because of the compatibility between TMS320C6000™ DSP platform devices, existing C6000™ software tools and development platforms can be used to develop code for the C6713 and other future devices. This capability allows for systems to be up and running when silicon becomes available.

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1 Introduction to the TMS320C6713 DSP Device

The Texas Instruments TMS320C6000 DSP platform of high-performance digital signal processors (DSPs) now includes the TMS320C6713. The C6713 brings the highest level of performance in the C6000 DSP platform of floating-point DSPs. At the initial clock rate of 225 MHz, the C6713 can process information at a rate of 1.35 giga-floating-point operations per second (GFLOPS).

Introduced in February 1997, the C6000 DSP platform is based on TI's VelociTI™ architecture, an advanced very-long-instruction-word (VLIW) architecture for DSPs. Advanced features of the VelociTI architecture include instruction packing, conditional branching, and pre-fetched branching, all of which overcome problems that were associated with previous VLIW implementations. The architecture is highly deterministic, with few restrictions on how or when instructions are fetched, executed, or stored. This architectural flexibility is key to the breakthrough efficiency levels of the C6000 compiler.

The roadmap for the floating-point C6000 DSP platform shown in Figure 1 demonstrates TI's commitment to present highest-performance DSPs.

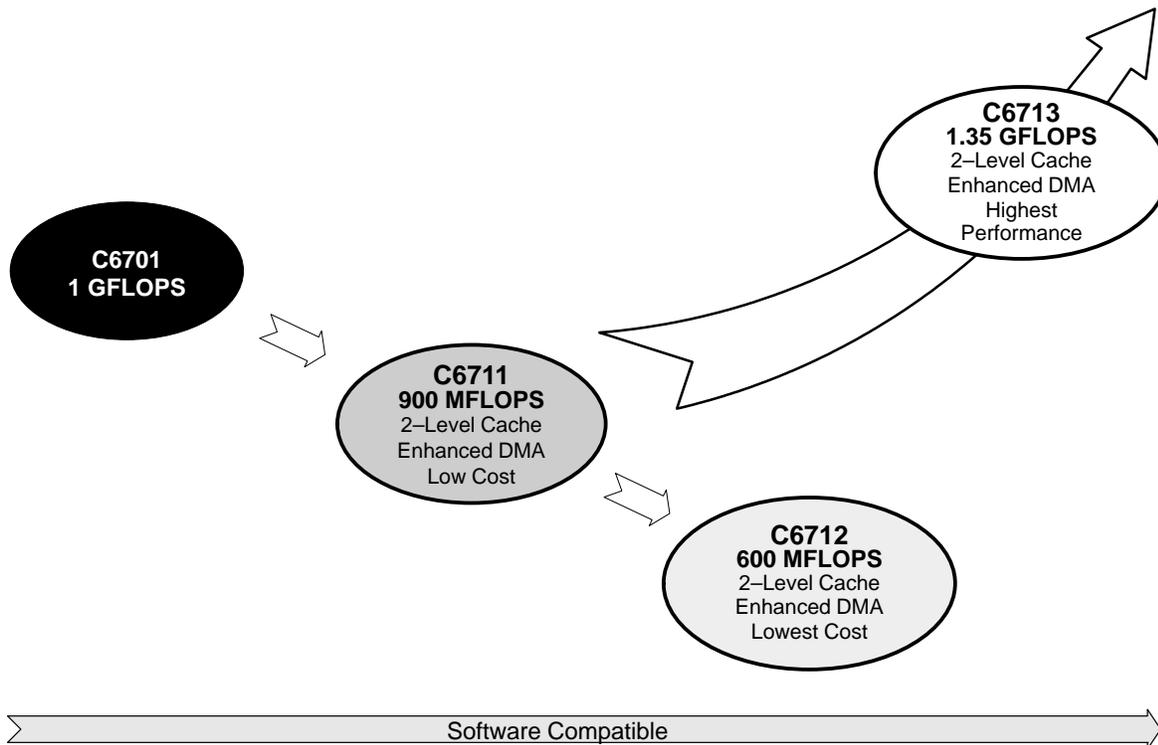


Figure 1. TMS320C6000 Highest-Performance Floating-Point DSP Roadmap

2 TMS320C6000 Compatibility

All C6000 DSP platform devices are code-compatible with one another, with the exception that there are some floating-point instructions that are only valid on the floating-point (TMS320C67x™) members. The C67x™ DSP core employs the VelociTI architecture that is designed to achieve high performance through increased instruction-level parallelism. VelociTI provides eight execution units, including two multipliers and six arithmetic logic units (ALUs). Out of eight functional units, six (L1, L2, S1, S2, M1, and M2) can perform six floating-point operations every cycle. These functional units operate in parallel and can perform up to eight instructions, including six floating-point operations during a single clock cycle—up to 1800 million instructions per second (MIPS), or 1.35 GFLOPS at 225 MHz initial device clock speed.

The common architecture allows designers to begin development with existing C6000 software tools for those devices currently in development. This also allows for migration from one C6000 processor to another, as design specifications require.

In addition to the DSP core, many of the on-chip peripherals are common between C6000 devices. Figure 2 shows a block diagram of the C6713 device. The blocks in white are common among members of C6700 generation of floating-point DSPs. The blocks in gray are new peripheral/improved features available on the C6713 device.

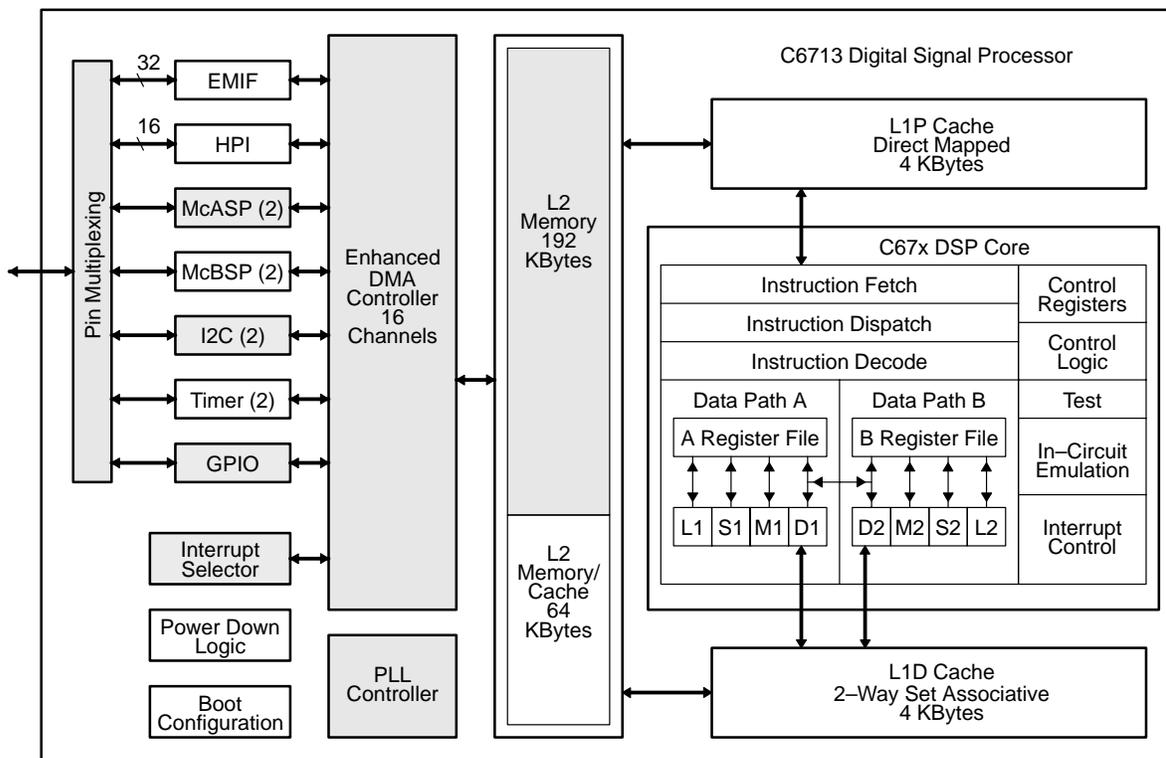


Figure 2. TMS320C6713 DSP Block Diagram

2.1 Similarities Between the C6713 and C6711(B) DSPs

The following device components are identical between the C6713 and C6711(B) devices:

- C67x floating-point DSP core
- L1P and L1D cache architecture
- 32-bit external memory interface (EMIF)
- 16-bit host port interface (HPI)
- Two multichannel buffered serial ports (McBSPs)
- Two 32-bit timers
- Boot configuration
- Power-down logic

2.2 Differences Between the C6713 and C6711(B) DSPs

Significant enhancements have been made to the C6713 over the C6711(B) to allow the C6713 to be the highest-performance floating-point DSP. These include:

- **Process Technology:** The C6711(B) is based on 0.18 μm /5-level metal CMOS process technology, while the C6713 employs 0.13 μm /6-level metal CMOS process technology.
- **Core Supply Voltage:** The C6711(B) requires 1.9V/1.8V of core supply voltage. The C6713 requires only 1.26V of core supply voltage, allowing high performance while still maintaining low-power consumption.
- **Clock Rate:** The C6711(B) runs at 150 and 100 MHz, while initial samples of C6713 run at 225 and 150 MHz.
- **Package:** The C6711(B) offers a 256-pin ball grid array (BGA), while the C6713 offers both BGA and a 208-pin PowerPAD™ plastic quad flatpack (QFP) package.
- **PLL Controller:** The Phase-Lock Loop (PLL) circuitry on the C6711(B) supports clock multiplier factors of x1 (bypass) and x4. On the C6713, the PLL resides within the PLL Controller module that does not require the external loop filter. The C6713 PLL controller also features a software-configurable PLL logic that supports three levels of clock divider/multipliers to provide different clock frequencies for the DSP core, the EMIF, CLKOUT3, and the other peripherals:
 - The first level is a clock divider (prescaler) that supports: /1, /2, ... /32 mode
 - The second level is a clock multiplier that supports: x4, x5, ..., x25 mode
 - The third level is a clock divider (postscaler) that supports: /1, /2, ... /32 mode

See *TMS320C6713 Floating-Point Digital Signal Processor* (SPRS186) and *TMS320C6000 PLL Controller Reference Guide* (SPRU233) for details on the PLL and the PLL controller.

- **Internal Memory:** The L1/L2 caches in C6713 have the same size and structure as C6711(B). In addition, the C6713 has an extra 192 KB of SRAM in L2 that can only function as mapped internal memory, but cannot function as L2 cache. This addition increases the size of L2 to a total of 256 KB.
- **Enhanced Direct Memory Access (EDMA):** The C6711(B) has 16 independent EDMA channels with fixed event mapping. The C6713 also has 16 independent EDMA channels, plus programmable event mapping, allowing flexible allocation of EDMA events for various peripherals.

- **Multichannel Audio Serial Port (McASP):** The C6711(B) does not have a McASP. The C6713 has two McASPs. Each of the McASPs features two independent clock zones (for transmit and receive) and 8 data pins. The McASP is capable of data interface in time-division multiplexed (TDM) synchronous serial format, burst mode format, or in digital audio interface transmitter (DIT) format; where the bit stream is encoded for S/PDIF, AES-3, IEC-60958 transmission. See section 4, *New Peripherals*, for more details.
- **Inter-Integrated Circuit (I2C) Port:** The C6711(B) does not have an I2C port. The C6713 has two I2C ports that are capable of transmit and receive in both master and slave interfaces. See section 4, *New Peripherals*, for more details.
- **General-Purpose Input/Output (GPIO):** On the C6711(B), GPIO pins are shared with timers and McBSP pins. The C6713 extends this capability by adding a dedicated GPIO module with 16 GPIO pins. The GPIO peripheral can also be programmed to generate different CPU interrupts and EDMA events.
- **Interrupt Selector:** New peripheral interrupts, i.e., interrupts from McASP_x, I2C_x, and GPIO, are added to the interrupt selection module.
- **Pin Multiplexing/Device Configuration:** Some of the pins on the C6713 are shared/multiplexed by two different peripherals. These pins are mutually exclusive; only one peripheral has exclusive use of each of these pins at anytime. The functions of these multiplexed pins are determined by:
 - External pullup/down resistors at device reset
 - HPI vs. McASP1/I2C0/GPIO, selected by HPI_EN (HD14) pin status at device reset:
 - HPI_EN = 0: HPI is disabled, McASP1/I2C0/GPIO are enabled.
 - HPI_EN = 1: HPI is enabled, McASP1/I2C0/GPIO are disabled.
 - Device Configuration Register (DEVCFG)
 - This register can be programmed to configure/enable certain peripheral combinations. Peripherals affected by this register include: McASP0, McBSP0, McBSP1, I2C1, TIMER0, and TIMER1.

The C6713 features convenience and flexibility in selecting peripherals to use. Various combinations of peripheral selections are possible by configuring the HPI_EN pin and the DEVCFG register. A few examples below are the peripheral combinations that the user can get:

- EMIF, GPIO, McASP0 (8 data pins), McASP1 (8 data pins), I2C0, I2C1, 2 timers
- EMIF, GPIO, McASP0 (5 data pins), McASP1 (8 data pins), I2C0, McBSP1, 2 timers
- EMIF, GPIO, McASP0 (DIT mode, 6 data pins), McASP1 (8 data pins), I2C0, I2C1, McBSP0, 2 timers
- EMIF, GPIO, McASP0 (DIT mode, 3 pins), McASP1 (8 pins), McBSP0, McBSP1, I2C0, 2 timers
- EMIF, HPI, McASP0 (8 data pins), I2C1, 2 timers
- EMIF, HPI, McASP0 (5 data pins), McBSP1, 2 timers

For more information about device configurations, see *TMS320C6713 Floating-Point Digital Signal Processor* (SPRS186).

3 Highest-Performance Floating-Point DSP

The TMS320C6713 DSP packs a powerful floating-point C67x DSP core along with feature-rich peripherals and achieves performance improvements over the industry's previous DSP performance leader, the TMS320C6701 DSP. Chips in development couple this processing performance with new memory and peripheral systems designed to accelerate real-time throughput for higher system performance.

The large internal memory and efficient on-chip cache architecture of the C6713 allows system designers to use slower, cheaper external-memory devices for data and program storage, while keeping the high-performance capabilities of the device. In addition, a cache helps programmers to achieve their performance goals faster, shortening code development and accelerating time to market.

The enhanced direct memory access (EDMA) controller allows designers to optimize data organization in their systems. Capable of accessing any location in the C6713 memory map, the EDMA controller transfers data in the background of DSP core operation. The EDMA controller can handle multiple transfers simultaneously and can interleave bursts. The EDMA controller offers 16 independent channels, with a separate RAM space to hold additional transfer configurations. Each EDMA controller channel is synchronized by an event to allow minimal intervention by the DSP core.

The on-chip memory is organized to allow design flexibility and ensure efficient memory usage. The C6713 has 264K bytes (KB) of on-chip memory, with 8 KB serving as a level-one (L1) cache that the DSP core can directly access. The L1 cache is divided into 4 KB of program (L1P) and 4 KB of data (L1D) cache memory. The remaining 256 KB of on-chip memory is a unified program and data memory space (L2). The 64 KB of L2 memory can serve as a level-two (L2) cache, be directly mapped as internal memory, or serve as a combination of these functions. The rest of L2 (192 KB) functions as mapped internal memory.

The L1P cache is direct-mapped, so that each instruction byte occupies a unique location in the cache. It has a 256-bit-wide data path to the DSP core, so that the DSP core may fetch eight instructions (one fetch packet) every cycle.

The L1D cache is two-way set associative, so that it can hold two different sets of information with independent address ranges. The L1D cache is a dual-ported memory that allows simultaneous accesses from both DSP core data ports, so that the DSP core can load or store two 64-bit values in a single L1D data cycle. The cache uses a least-recently-used (LRU) replacement scheme to select between the two possible cache locations on a cache miss.

The 64 KB of L2 memory is divided into four 16-KB blocks, each of which can be programmed as a cache or RAM space. Each block selected as cache adds one way of associativity, allowing the L2 cache to be 0- (no cache), 1-, 2-, 3-, or 4-way associative. Blocks of L2 that are selected as cache are not included in the C6713 memory map. The remaining 192 KB of L2 functions as mapped internal memory. The mappability of L2 blocks as addressable locations allows critical code and data to be locked into internal memory.

TI has run extensive tests on this L1/L2 architecture to determine how it performs with an enhanced full-rate global system module (GSM) vocoder, system-level applications in asymmetric digital subscriber line (ADSL), V.90 modems, and other commonly used algorithms. For both data and program, TI's tests indicate L1 cache hit rates greater than 98 percent. In other words, only one instruction or data word in fifty needs to be fetched from L2 or external memory.

The high L1 hit rate, combined with the large size and flexibility of L2 memory organization, means that this architecture can operate at competitive cycle performance of a more expensive device, with a traditional memory organization where all system memory is on the chip. This high degree of efficiency allows systems to rely on inexpensive external memory for program and data storage, while at the same time performing high speed, number-crunching routines in real time.

4 New Peripherals

New peripherals have been added to the C6713 DSP from the previous C6711. They are: clock generator, general-purpose input/output (GPIO) module, two multichannel audio serial ports (McASPs), and two inter-IC (I2C) ports. *TMS320C6713 Floating-Point Digital Signal Processor* (SPRS186) has the detailed description of the clock generator module. *TMS320C6000 Peripherals Reference Guide* (SPRU190) explains the GPIO module in detail. This section explains the new McASP and I2C peripherals.

4.1 Multichannel Audio Serial Port (McASP)

The C6713 device includes two multichannel audio serial port (McASP) peripherals. The McASP is a serial port optimized for the needs of multichannel audio applications. With two McASP ports, the C6713 device is capable of supporting two completely independent audio zones simultaneously.

Each McASP consists of a transmit and a receive section. They may operate completely independently with separate master clocks, bit clocks, and frame syncs, and using different transmit modes with different bit stream formats. Alternatively, the transmit and receive sections may be synchronized. Each McASP module also includes 8 serializers that can be individually enabled to either transmit or receive. Figure 3 illustrates the major McASP blocks.

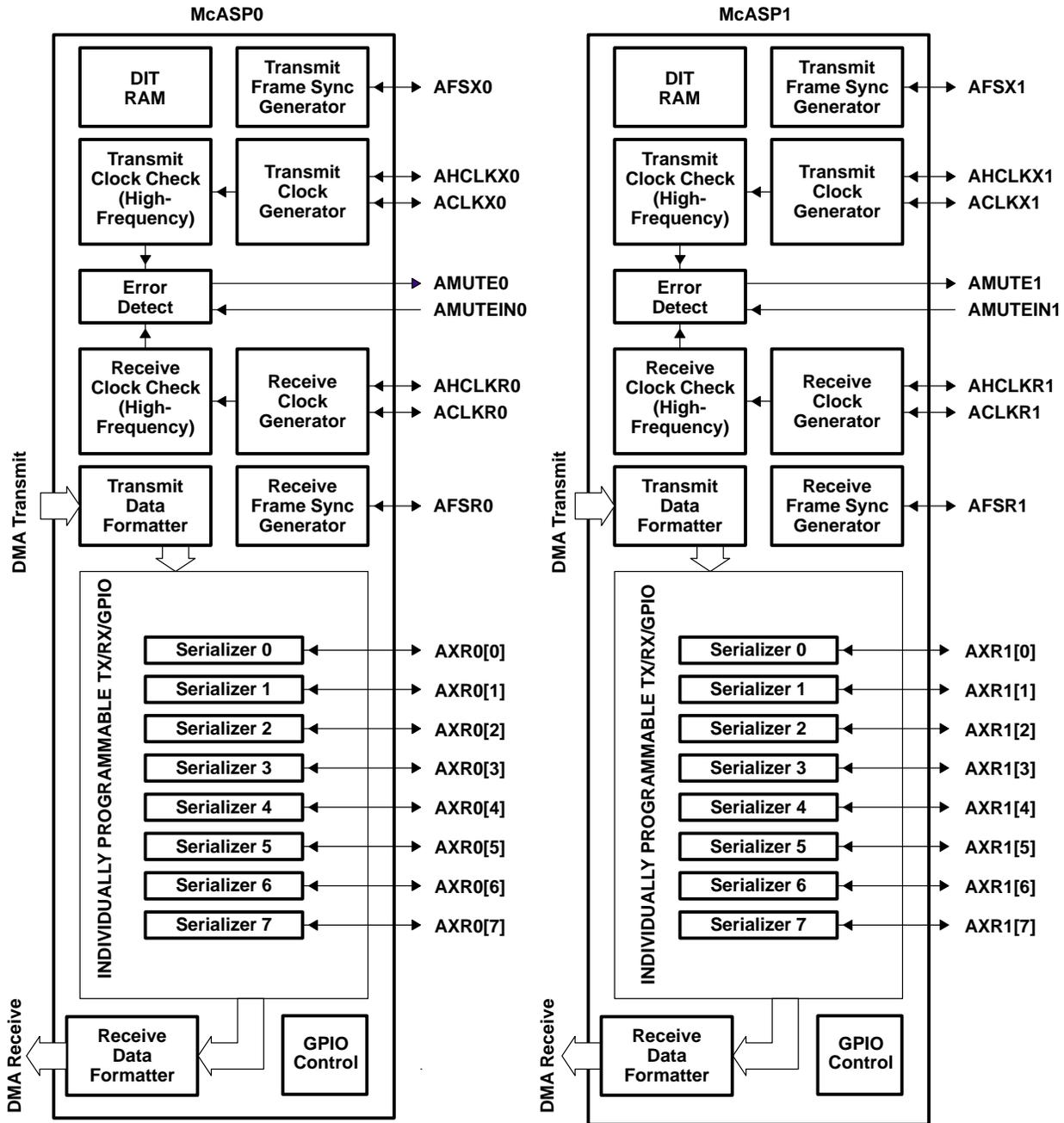


Figure 3. McASP Block Diagram

As shown in Figure 3, each of the two McASPs on the C6713 device is capable of controlling 8 serial data (AXR) pins, both transmit and receive. Each McASP includes full general-purpose input/output (GPIO) control, so any pins not needed for serial transfers can be used for general-purpose I/O pins.

When transmitting audio data, the transmit section of the McASP can transmit data in either a time division multiplexed (TDM) synchronous serial format, or in digital audio interface (DIT) format, where the bit stream is encoded for S/PDIF, AES-3, IEC-60958, CP-430 transmission. The receive section of the McASP supports the TDM synchronous serial format.

The McASP also supports a burst mode, which is useful for non-audio data (for example, passing control information between two DSPs). Burst mode uses a synchronous serial format similar to TDM, except a frame sync is generated for each data word transferred, and frame sync generation is not periodic or time-driven as in TDM mode, but rather, is data-driven.

4.1.1 Multichannel Time-Division Multiplexed (TDM) Synchronous Transfer Mode

The McASP supports a multichannel, synchronous, time-division multiplexed (TDM) transfer mode for both transmit and receive. Within this transfer mode, a wide variety of serial data formats are supported, including formats compatible with devices using the inter-IC Sound (I2S) protocol.

The TDM synchronous serial transfer mode is typically used when communicating between integrated circuit devices on the same printed circuit board or on another printed circuit board within the same piece of equipment. For example, TDM synchronous serial transfer mode would be used to transfer data between the DSP and one or more ADC, DAC, CODEC, or S/PDIF receiver devices.

To transmit data in the TDM synchronous serial transfer mode requires a minimum set of pins:

- ACLKX – transmit bit clock
- AFSX – transmit frame sync (commonly called left/right clock)
- One or more serial data pins, whose serializers have been configured to transmit.

The transmitter has the option to receive the ACLKX bit clock as an input from the system, or to generate the ACLKX bit clock by dividing down the AHCLKX high-frequency master clock. Furthermore, the transmitter can either generate AHCLKX internally, or accept it as an input from the system.

Similarly, to receive data in the TDM synchronous serial transfer mode requires a minimum set of pins:

- ACLKR – receive bit clock
- AFSR – receive frame sync (commonly called left/right clock)
- One or more serial data pins, whose serializers have been configured to receive.

The receiver has the option to receive the ACLKR bit clock as an input from the system, or to generate the ACLKR bit clock by dividing down the AHCLKR high-frequency master clock. Furthermore, the receiver can either generate AHCLKR internally, or to accept it as an input from the system. In addition, the receiver has the option to use the transmitter bit clock and frame sync.

All of the signals in the TDM synchronous serial protocol are synchronous to the respective bit clocks (ACLKX or ACLKR).

Data transfers in the TDM synchronous serial transfer mode are continuous and periodic, since this mode is most commonly used to communicate with data converters that operate at a fixed sample rate. The bit streams are organized into frames of data, and the beginning of a frame is marked by a frame sync edge on the AFSX (transmit) or AFSR (receive) frame sync pin.

In a typical system, one frame of data is transferred during each data converter sample period. To support multiple channels, the choices are to either include more timeslots per frame (and therefore operate with a higher bit clock), or to keep the bit clock period constant and use additional data pins to transfer the same number of channels.

For example, a particular six-channel DAC might require three serial data pins, transferring two channels data on each pin during each sample period. Another similar DAC may be designed to use only a single serial data pin, but clock three times faster and transfer six channels of data per time slot. The McASP is flexible enough to support either type of DAC.

TDM mode on the McASP is extensible to support multiprocessor applications, with up to 32 time slots per frame. For each of the time slots, the McASP may be configured to participate or be inactive, which allows multiple DSPs to communicate on the same TDM serial bus.

In addition, to support S/PDIF, AES-3, IEC-60958, CP-430 receiver ICs whose natural block (block corresponds to McASP frame) size is 384 samples, the McASP receiver supports a 384 time slot mode. The advantage to using the 384 time slot mode is that interrupts may be generated synchronous to the S/PDIF, AES-3, IEC-60958, CP-430, for example, the “last slot” interrupt.

4.1.2 Burst Transfer Mode

The McASP also supports a burst transfer mode, which is useful for non-audio data (for example, passing control information between two DSPs). Burst transfer mode uses a synchronous serial format identical to TDM, except the frame sync is generated for each data word transferred. In addition, frame sync generation is not periodic or time-driven as in TDM mode, but rather, data-driven.

4.1.3 Supported Bit Stream Formats for TDM and Burst Transfer Modes

The serial data pins support a wide variety of formats. In the TDM and burst synchronous modes, the data may be transmitted/received with the following options:

- Time slots per frame: 1 (burst/data-driven), or 2, 3 ... 32, or 384 (TDM/time-driven).
- Time slot size: 8, 12, 16, 20, 24, 28, 32 bits per time slot.
- Data size: 8, 12, 16, 20, 24, 28, 32 bits (must be less than or equal to time slot).
- Data alignment within time slot: Left- or right-justified.
- Bit order: MSB or LSB first.
- Unused bits in time slot: Padded with 0, 1, or extended with value of another bit.
- Time slot delay from frame sync: 0, 1, or 2 bit delay.

The data format can be programmed independently for transmit and receive, and for McASP0 vs. McASP1. In addition, the McASP can automatically realign the data as processed natively by the DSP (either integer or Q31 fractional formats), adjusting it in hardware to any of the supported serial bit stream formats outlined above. This reduces the amount of bit manipulation that the DSP must perform, and simplifies software architecture.

4.1.4 Digital Audio Interface Transmitter (DIT) Transfer Mode (Transmitter Only)

In addition to the TDM and burst transfer modes, which are suitable for transmitting audio data between ICs inside the same system, the McASP also supports transmission of audio data in the S/PDIF, AES-3, IEC-60958, or CP-430 format. These formats are designed to carry audio data between different systems through either an optical or coaxial cable.

From an internal DSP standpoint, the McASP operation is basically identical to the two time-slot TDM mode, but the data transmitted is output as a bi-phase, mark-encoded bit stream with preamble, channel status, user data, validity, and parity automatically stuffed into the bit stream by the McASP module. The McASP includes separate validity bits for even/odd subframes, and two 384-bit RAM modules to hold channel status and user data bits.

To transmit data in the DIT mode, the following pins are typically needed:

- AHCLKX – Transmit Master Clock
- One or more serial data pins, whose serializers have been configured to transmit.

Strictly speaking, AHCLKX is optional (the internal oscillator clock may be used) but if used as a reference, the DSP provides a clock check circuit that continually monitors the AHCLKX input for stability.

If a single McASP is configured to transmit in the DIT mode on more than one serial data pin, the bit streams on all pins will be synchronized. In addition, although they will carry unique audio data, they will carry the same channel status, user data, and validity information.

4.1.5 McASP Flexible Clock Generators

The McASP requires a minimum of a bit clock and a frame sync to operate, and provides the capability to reference these clocks from a high-frequency master clock. In TDM and burst transfer modes, the minimum set of clocks must be available to all devices; therefore, it is required that the ACLKX, ACLKR, AFSX, AFSR pins be used for serial port functions. In DIT mode, it is possible to use only internally generated clocks and frame syncs.

The transmit bit clock can either be input from the system on the ACLKX pin, or internally generated. If internally generated, it is divided down by a programmable divider ($/1$, $/2$, $/3$, ... $/4096$) from the transmit high-frequency master clock. In TDM and burst modes, an internally generated clock must be output on the AHCLKX pin; this is not required in DIT mode. When either internally generated or input from the system, polarity of this clock may be programmed to be either rising or falling edge.

The transmit high-frequency master clock may be either externally sourced from the AHCLKX pin or internally generated by a programmable divider ($/1$, $/2$, $/3$, ... $/4096$) from the internal oscillator clock on the C6713 device. If internally generated, this clock may be (but is not required to be) output on the AHCLKX pin, where it is available to other devices in the system. The AHCLKX polarity is also programmable.

The transmit frame sync pin is AFSX. A typical usage for this pin is to carry the LRCLK signal when transmitting and receiving stereo data. Options for the transmit frame sync signal include internal or external, bit or slot length, rising or falling edge polarity, and 0-, 1-, or 2-bit delay until the first data bit.

The receiver has an identical, but independent, clock generation circuit as the transmitter. The receiver bit clock pin is ACLKR. The receiver high-frequency master clock pin is AHCLKR, and the receiver frame sync pin is AFSR. The receiver also has the option to use the transmitter ACLKX, AFSX signals (but it may be configured with different polarity and frame sync, data delay options). In this case, the AFSR and ACLKR pins are available as general-purpose I/O (GIO).

Some examples of the things that a system designer can use the McASP clocking flexibility for are:

- Receiving data from a DVD at 48 KHz, but outputting up-sampled or decoded audio at 96 KHz or 192 KHz. This might be accomplished by inputting a high-frequency master clock (for example, $512 * \text{receive fs}$), receiving with an internally generated bit clock ratio of $/8$, while transmitting with an internally generated bit clock ratio of $/4$ or $/2$.

- Transmitting/receiving data based one sample rate (for example, 44.1 KHz) using McASP0, while transmitting and receiving at a different sample rate (for example, 48 KHz).
- Using the DSPs on-board oscillator to supply the “local oscillator” system clock, when the input source is an A/D converter.

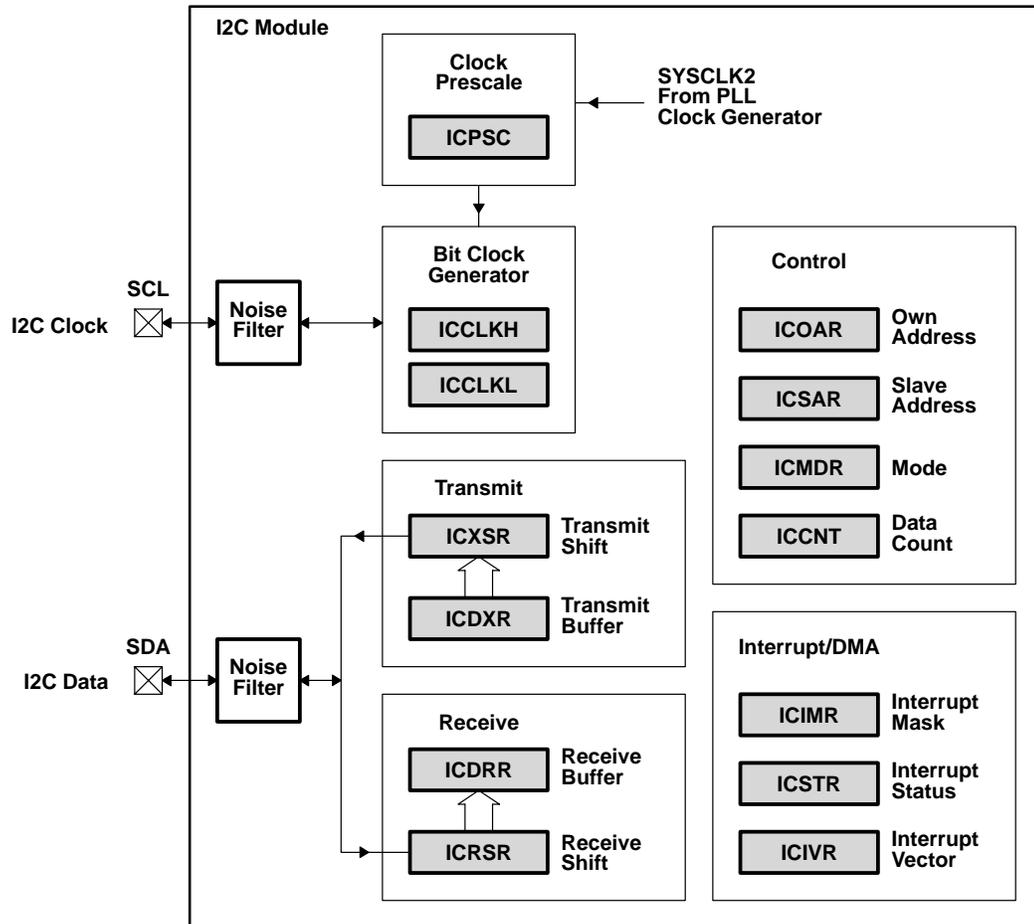
4.1.6 McASP Error Handling and Management

To support the design of a robust audio system, the McASP module includes error-checking capability for the serial protocol, data underrun, and data overrun. In addition, each McASP includes a timer that continually measures the high-frequency master clock every 32 clock cycles. The timer value can be read to get a measurement of the clock frequency, and has a min-max range setting that can raise an error flag if the master clock goes out of a specified range.

Upon the detection of any one or more of the above errors (software selectable), or the assertion of the AMUTEIN pin, the AMUTE output pin may be asserted to a high or low (selectable) level, to immediately mute the audio output. In addition, an interrupt may be generated, if desired, based on any one or more of the error sources.

4.2 Inter-Integrated Control Circuit (I2C)

Another new peripheral featured on the C6713 is the Inter-IC (I2C) Control Circuit. Having two I2C modules on the TMS320C6713 simplifies system architecture, since one module may be used by the DSP to control local peripherals' ICs (DACs, ADCs, etc.), while the other may be used to communicate with other controllers in a system, or to implement a user interface. The block diagram of the I2C peripheral is illustrated in Figure 4.



NOTE: Shading denotes control/status registers.

Figure 4. I2C Module Block Diagram

The C6713 also includes two I2C serial ports for control purposes. Each I2C port supports:

- Compatibility with Philips I2C specification, revision 2.1 (January 2000)
- Fast mode up to 400 Kbps (no fail-safe I/O buffers)
- Noise filter to remove noise, 50 ns or less
- Seven- and ten-bit device addressing modes
- Master (transmit/receive) and slave (transmit/receive) functionality
- Events: DMA, interrupt, or polling
- Slow-rate, limited open-drain output buffers

5 Begin Writing Code for the C6713 Today

Full object code compatibility with existing C6000 DSPs allows system developers to begin development of C6713 DSP systems today. The code-compatible, floating-point DSP cores in the C6711, C6712, and C6713 devices allow for code to be written for the C6713 using existing C6000 tools. By taking advantage of the C6000 software and hardware tools currently available, C6713 systems can have a running start for when silicon becomes available.

The C6000 simulator may be used to provide a cycle-accurate account of device performance, and to provide a good environment to learn the C6000 VLIW architecture. The C6713 configuration of the simulator is available to model the device. The C6713 simulator configuration also models the EDMA, EMIF, and cache performance of the device. Using this configuration, it is possible to optimize code structure and data organization to take advantage of the C6713 cache structure. L1 cache misses to L2 and L2 cache misses are supported with 100% cycle accuracy. C6713 designs may be worked out in detail on the simulator prior to purchasing actual silicon.

The C6000 compiler may be used for all members of the C6000 device platform. Floating-point devices are object code compatible, so the C6713 may use code written for the C6711 or C6712.

For a development start in hardware, the C6711 DSP Starter Kit (DSK) may be used to understand the C6000 functionality. In this environment, code can be debugged while running in real time. Applications running on the C6711 DSK will not be 100% cycle accurate to a C6713 system, due to the difference in the internal memory architecture, clock rates, and other peripherals. Many of the peripherals on the C6713, such as McBSP, EDMA, EMIF, HPI, and timers, are identical to those of C6711, so the C6711 DSK is a good tool for understanding how to incorporate the peripherals into a real-time system. The identical architectures of the C6711 and C6713 devices allow for many system-level issues to be resolved prior to obtaining C6713 silicon.

Using these development platforms, as well as the C6000 literature currently available, will enable C6713 systems to be completed soon after C6713 silicon is made available.

5.1 C6000 Tools Support

C6000 tools are available now for use in all C6000 designs. The C6000 development tools available today for the C6713 are:

- C6000 simulator software
- C6000 optimizing C compiler/assembler
- TMS320C6711 DSP Starter Kit (DSK)
- TMS320C6201 multichannel evaluation module (McEVM)
- XDS510 C6000 C Source debugger software
- XDS510 emulator hardware with JTAG emulation cable

5.2 C6000 Literature Available

A great deal of literature is available today for the C6000 devices.

- *TMS320C6713 Floating-Point Digital Signal Processor* (SPRS186).
- *TMS320C6000 CPU and Instruction Set Reference Guide* (SPRU189).
- *TMS320C6000 CPU and Instruction Set Reference Guide – Manual Update Sheet for SPRU189F* (SPRZ168).
- *TMS320C6000 Peripherals Reference Guide* (SPRU190).
- *TMS320C6000 Peripherals Reference Guide – Manual Update Sheet for SPRU190D* (SPRZ122).
- *TMS320C6000 PLL Controller Reference Guide* (SPRU233)
- *TMS320C6000 Technical Brief* (SPRU197).
- *Code Composer Studio User's Guide* (SPRU328).
- *TMS320C6000 Code Composer Studio Tutorial* (SPRU301).
- *TMS320C6000 Programmer's Guide* (SPRU198).
- *TMS320C6201/6701 Evaluation Module User's Guide* (SPRU269).
- *TMS320C6000 Chip Support Library API Reference Guide* (SPRU401).
- *TMS320C6x Peripheral Support Library Programmer's Reference* (SPRU273).
- *TMS320C6000 Assembly Language Tools User's Guide* (SPRU186).
- *TMS320C6000 Optimizing C Compiler User's Guide* (SPRU187).
- *TMS320C6x C Source Debugger User's Guide* (SPRU188).
- *TMS320C6x C Source Debugger For SPARC* (SPRU224).
- *TMS320C6000 DSP/BIOS User's Guide* (SPRU303).
- *TMS320C6000 DSP/BIOS Application Programming Interface (API) Reference Guide* (SPRU403).
- *TMS320 DSP Algorithm Integration Standard Rules and Guidelines* (SPRU352).
- *TMS320 DSP Product Family Glossary* (SPRU258).
- *TMS320 DSP Algorithm Standard Developer's Guide* (SPRU424).

Many application reports also exist for assistance with C6711/C6713 applications.

- *Migrating from TMS320C6211(B)/6711(B) to TMS320C6713* (SPRA851)
- *Bit-Reverse/Digit-Reverse: Linear-Time Small Lookup Table Implementation for the TMS320C6000* (SPRA440).
- *Guidelines For Software Development Efficiency On the TMS320C6000 VelociTI Architecture* (SPRA434).
- *Implementation Of G.726 ADPCM On TMS320C62xx DSP* (BPRA066).
- *Implementing V.32bis Viterbi Decoding on the TMS320C62xx DSP* (SPRA444).

- *Performance Analysis of Line Echo Cancellation Implementation Using TMS320C6201 (SPRA421).*
- *TMS320C6201 Power Supply (SPRA447).*
- *TMS320C6000 System Clock Circuit Example (SPRA430).*
- *TMS320C6000 EMIF to External SDRAM Interface (SPRA433).*
- *TMS320C6000 BGA Manufacturing Considerations (SPRA429).*
- *PowerPAD Thermally Enhanced Package Technical Brief (SLMA002).*
- *TMS320C6000 Board Design: Considerations for Debug (SPRA523).*
- *Reset Circuit for the TMS320C6000 DSP (SPRA431).*
- *TMS320C6x Thermal Design Considerations (SPRA432).*
- *Using the TMS320C6000 McBSP as a High Speed Communication Port (SPRA455).*

NOTE: For more information, go to the TI web site at <http://www.ti.com>

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265