

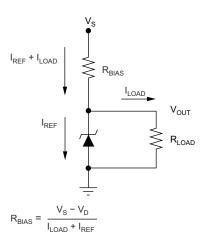
REF1112 10ppm/°C, 1µA, 1.25V Shunt Voltage Reference

1 Features

- Small package: SOT23-3
- Fixed reverse breakdown voltage of 1.25V
- Key specifications
 - Output voltage tolerance: ±0.2% (maximum)
 - Low output noise (0.1Hz to 10Hz): $25\mu V_{pp}$ (typical)
 - Temperature range: -40°C to +125°C
 - Operating current range: 1.2µA to 5mA
 - Low temperature coefficient from 0°C to +70°C: 30ppm/°C (maximum)
 - Low temperature coefficient from –40°C to +85°C: 50ppm/°C (maximum)

2 Applications

- Battery-powered instruments
- Building security sensors
- Medical equipment
- Field transmitters
- Calibrators



Shunt Reference Application Schematic

3 Description

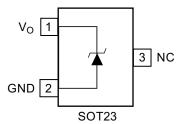
The REF1112 device is a two-terminal shunt reference designed for power and space sensitive applications. The REF1112 features an operating current of 1µA in a SOT23-3 package and is an improved, lower power voltage reference for designs currently using voltage references in larger packages, such as the REF1004 and LT1004. The REF1112 is specified from -40°C to +85°C with operation extending from -40°C to +125°C.

The REF1112 complements other 1µA components from Texas Instruments including the OPA349 and TLV240x low-power operational amplifiers, and the TLV349x micropower voltage comparator.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
REF1112	SOT-23 (3)	2.92mm × 1.3mm

- For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and includes pins, where applicable.



NC indicates the pin must be left unconnected or connected to **GND**

Pinout



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4 Pin Configuration and Functions

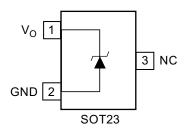


Figure 4-1. DBZ Package 3-Pin SOT-23 Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION		
NAME	NO.	1/0	DESCRIPTION		
Vo	1	I/O	Shunt Current/Voltage input		
GND	2	0	Ground connection		
NC	3	-	Must float or connect to GND		

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Reverse breakdown current		10	mA
Forward current		10	mA
Operating temperature	– 55	125	°C
Junction temperature		150	°C
Storage temperature, T _{stg}	-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
V	\	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
V _(ESD) Electrostatic discharge		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

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over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
I _{REF}	Reverse current	0.0012	5	mA
T _A	Operating temperature	-40	125	°C

Product Folder Links: REF1112



5.4 Thermal Information

		REF1112	
	THERMAL METRIC ⁽¹⁾	DBZ (SOT-23)	UNIT
		3 PINS	
R _{0JA}	Junction-to-ambient thermal resistance	219	°C/W
R ₀ JC(top)	Junction-to-case (top) thermal resistance	99	°C/W
R _{0JB}	Junction-to-board thermal resistance	79	°C/W
ΨЈТ	Junction-to-top characterization parameter	6.7	°C/W
ΨЈВ	Junction-to-board characterization parameter	79.6	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

 V_R = 1.25V, T_A = +25°C, I_{REF} = 1.2 μ A and C_{LOAD} = 10nF, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V	Davaraa braakdayya yaltaga	- 1 200	1.2475	1.25	1.2525	V
V _R	Reverse breakdown voltage	I _{REF} = 1.2μA	-0.2%		0.2%	
		$1.2\mu A \le I_{REF} \le 5mA$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$		10	30	
ΔV _R	Temperature coefficient	$1.5\mu A \le I_{REF} \le 5mA$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$		15	50	ppm/°C
		$1.5\mu A \le I_{REF} \le 5mA$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$		15		
I _{RMIN}	Minimum operating current			1	1.2	μA
$\Delta V_R/\Delta I_R$	Reverse breakdown voltage change with current	1.2μA ≤ I _{REF} ≤ 5mA		100	150	ppm/mA
Z _R	Reverse dynamic impedance	1.2µA ≤ I _{REF} ≤ 5mA		0.135	0.2	Ω
e _N	Low-frequency noise ⁽¹⁾	0.1Hz ≤ I _{REF} ≤ 10Hz		25		μV_{PP}
V _{HYST}	Thermal hysteresis ⁽²⁾			100		ppm
ΔV_R	Long-term stability	+25°C ± 0.1°C		60		ppm/kHr

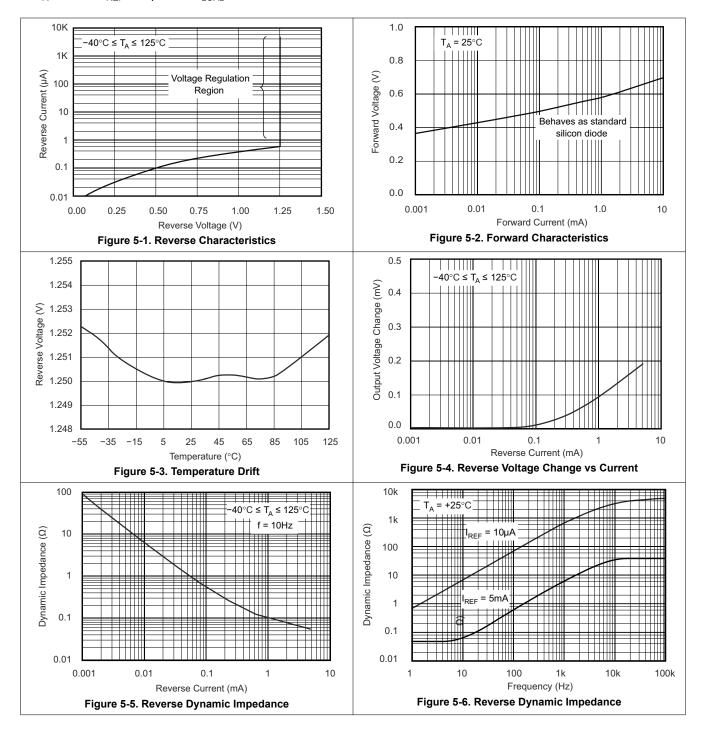
⁽¹⁾ Peak-to-peak noise is measured with a 2-pole high-pass filter at 0.1Hz and a 4-pole, low-pass Chebyshev filter at 10Hz.

Product Folder Links: REF1112

⁽²⁾ Thermal hysteresis is defined as the change in output voltage after operating the device at +25°C, cycling the device through the specified temperature range, and returning to +25°C.

5.6 Typical Characteristics

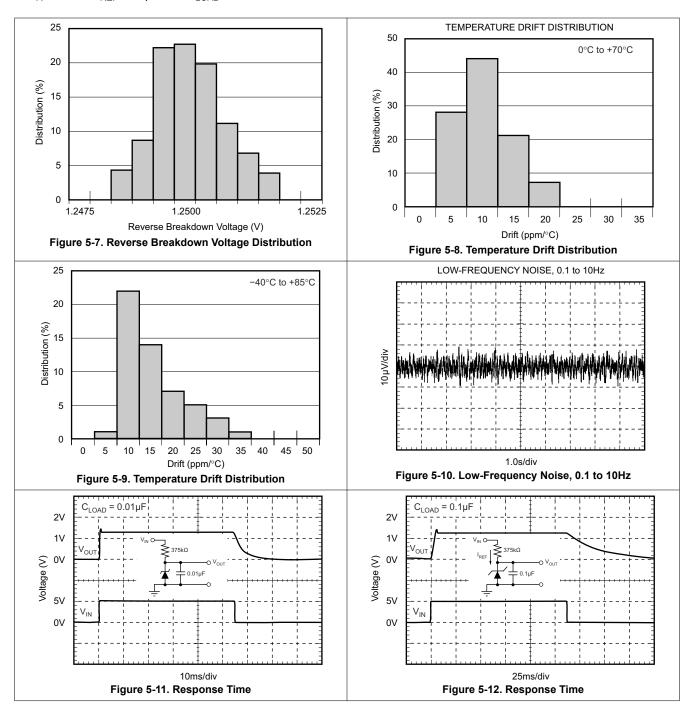
At T_A = +25°C, I_{REF} = 10 μ A and C_{LOAD} = 10nF, unless otherwise noted.





5.6 Typical Characteristics (continued)

At T_A = +25°C, I_{REF} = 10 μA and C_{LOAD} = 10nF, unless otherwise noted.

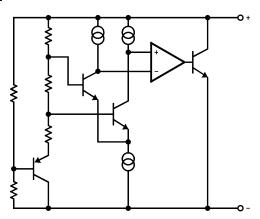


6 Detailed Description

6.1 Overview

The REF1112 is a 2-terminal bandgap reference diode designed for high accuracy with outstanding temperature characteristics at low operating currents. Precision thin-film resistors result in 0.2% initial voltage accuracy and 50ppm/°C maximum temperature drift. The REF1112 is specified from –40°C to +85°C, with operation from –40°C to +125°C, and is offered in a SOT23-3 package.

6.2 Functional Block Diagram



6.3 Feature Description

The REF1112 device is effectively a precision Zener diode. The part requires a small quiescent current for regulation, and regulates the output voltage by shunting more or less current to ground, depending on input voltage and load. The only external component requirement are an resistor between the cathode and the input voltage to set the input current and an external capacitor at the output to maintain stability under varying loads.

6.4 Device Functional Modes

The REF1112 device is a fixed output voltage part where the feedback is internal. Therefore, the part can only operate in a closed-loop mode and the output voltage cannot be adjusted. The output voltage remains in regulation as long as I_{REF} is between I_{REFMIN} (see *Electrical Characteristics*) and I_{REFMAX} is 5mA. A proper selection of the external resistor for input voltage range and load current range maintains that these conditions are met.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

Typical connections for the REF1112 are shown in Figure 7-1. A minimum 1 μ A bias current is required to maintain a stable output voltage and can be provided with a resistor connected to the supply voltage. I_{BIAS} depends on the values selected for R_{BIAS} and V_S , and varies as a sum of the minimum operating current and the load current. To maintain stable operation, the value of R_{BIAS} must be low enough to maintain the minimum operating current at the minimum and maximum load and supply voltage levels.

A 0.1µF load capacitor is recommended to maintain stability under varying load conditions. A minimum 0.01µF load capacitor is required for stable operation. Start-up time for the REF1112 is be affected, depending on the value of load capacitance and the bias currents being used. A 1µF power-supply bypass capacitor is recommended to minimize supply noise within the circuit. The REF1112 shunt voltage reference provides a versatile function for low power and space-conservative applications.

7.2 Typical Applications

7.2.1 Shunt Regulator

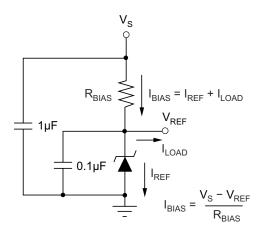


Figure 7-1. Typical Connections

7.2.1.1 Design Requirements

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage	3V
Cathode current (I _{REF})	1.2µA
Load Current (I _{LOAD})	50uA

Product Folder Links: REF1112

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7.2.1.2 Detailed Design Procedure

When using the REF1112 as a reference, determine the following:

- · Supply voltage range
- · Current source resistance
- · Reference voltage accuracy

To design using the REF1112, make sure that the V_S is larger than V_{REF} .

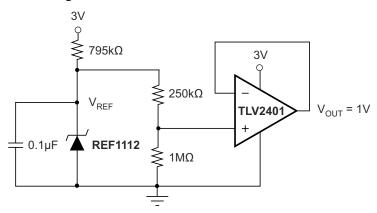
The resistor R_{BIAS} sets the cathode current of the REF1112, I_R . Make sure that this current remains in the operational region of the part for the entire V_S and load range.

Using this information, select a R_{BIAS} such that:

 $I_{REFMIN} < I_{REF} < I_{REFMAX}$ where $I_{REFMAX} = 5$ mA.

In this application the I_{REF} is the operating current of the REF1112 plus the maximum possible I_{LOAD} under no-load conditions.

7.2.2 MicroPOWER 3µA, 1V Voltage Reference



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Figure 7-2. MicroPOWER 3µA, 1V Voltage Reference

7.2.2.1 Design Requirements

The REF1112 can be scaled to provide extremely low power reference voltages. Figure 7-2 shows the REF1112 used as a 1V V_{OUT} , 3 μ A voltage reference.

7.2.2.2 Detailed Design Procedure

Set R_{BIAS} such that the current through the shunt reference, I_{REF}, is greater than I_{REFMIN} + I_{LOAD}.

Use a resistor divider to set the required voltage to the input of the amplifier. The TLV2401 requires an input bias current maximum of 350pA which allows the use of larger resistor values to save power.

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7.2.3 2.5V Reference on 1µA

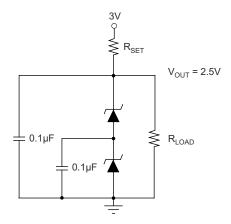


Figure 7-3. 2.5V Reference on 1µA

7.2.3.1 Design Requirements

Create a 2.5V reference that consumes 1µA of I_{RFF}.

7.2.3.2 Detailed Design Procedure

Figure 7-3 shows the REF1112 used as a 2.5V reference on 1μ A. This is done by stacking the REF1112 in series.

$$V_{OUT} = 2 \times V_{REF} \tag{1}$$

where

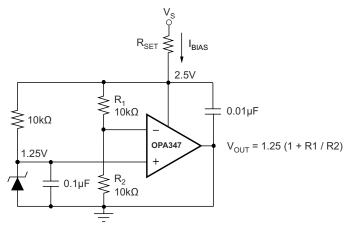
V_{RFF} is the reference voltage

In this case, $V_{OUT} = 2 \times 1.25V = 2.5V$

The I_{BIAS} is still 1µA because the stacked REF1112 are in series.

7.2.4 Adjustable Voltage Shunt Reference

For applications requiring a stable voltage reference capable of sinking higher than 5mA of current, a REF1112 combined with an OPA347 can sink up to 10mA of current. This configuration is shown in Figure 7-4, and through appropriate selection of R1 and R2, can be used to provide a wide range of stable reference voltages.



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Figure 7-4. Adjustable Voltage Shunt Reference

7.2.5 Level Shift to Achieve Full ADC Input Range

The REF1112 is also useful for level shifting, and as shown in Figure 7-5, can be used to achieve the full input range of an analog-to-digital converter (ADC).

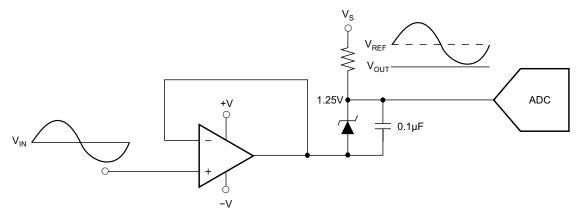


Figure 7-5. REF1112 Provides a Level Shift to Achieve Full ADC Input Range

7.2.6 Stable Current Source

The REF1112 can be configured with an additional diode and NPN transistor to provide a temperature compensated current reference as shown in Figure 7-6.

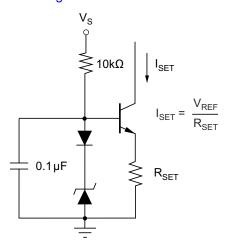


Figure 7-6. REF1112 as a Stable Current Source

7.3 Power Supply Recommendations

While a bypass capacitor is not required on the input voltage line, TI recommends reducing noise on the input which can affect the output. A $0.1\mu F$ ceramic capacitor or larger is recommended.

7.4 Layout

7.4.1 Layout Guidelines

Place decoupling capacitors as close to the device as possible. Use appropriate widths for traces when shunting high currents to avoid excessive voltage drops.

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7.4.2 Layout Example

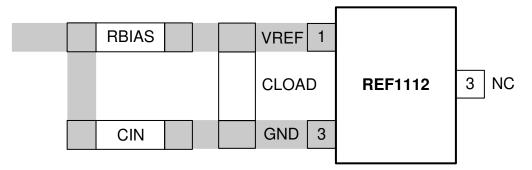


Figure 7-7. Layout Example

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E[™] is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

(Changes from Revision D (March 2018) to Revision E (December 2024)	Page
•	Updated the numbering format for tables, figures, and cross-references throughout the document	1
•	Updated Z _R and ΔV _R /ΔI _R	4
-		

Changes from Revision C (March 2008) to Revision D (March 2018)

Page

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking
	(1)	(2)			(3)	(4)	(5)		(6)
REF1112AIDBZR	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	R11A
REF1112AIDBZR.A	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	R11A
REF1112AIDBZRG4	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R11A
REF1112AIDBZRG4.A	Active	Production	SOT-23 (DBZ) 3	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R11A
REF1112AIDBZT	Active	Production	SOT-23 (DBZ) 3	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	R11A
REF1112AIDBZT.A	Active	Production	SOT-23 (DBZ) 3	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	R11A
REF1112AIDBZTG4	Active	Production	SOT-23 (DBZ) 3	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R11A
REF1112AIDBZTG4.A	Active	Production	SOT-23 (DBZ) 3	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R11A

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

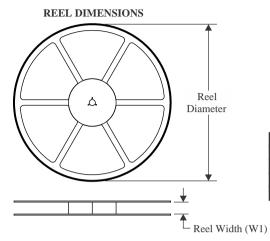
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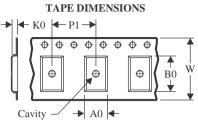
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

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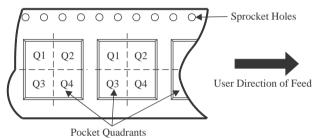
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF1112AIDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
REF1112AIDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3
REF1112AIDBZRG4	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
REF1112AIDBZT	SOT-23	DBZ	3	250	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3
REF1112AIDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
REF1112AIDBZTG4	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3



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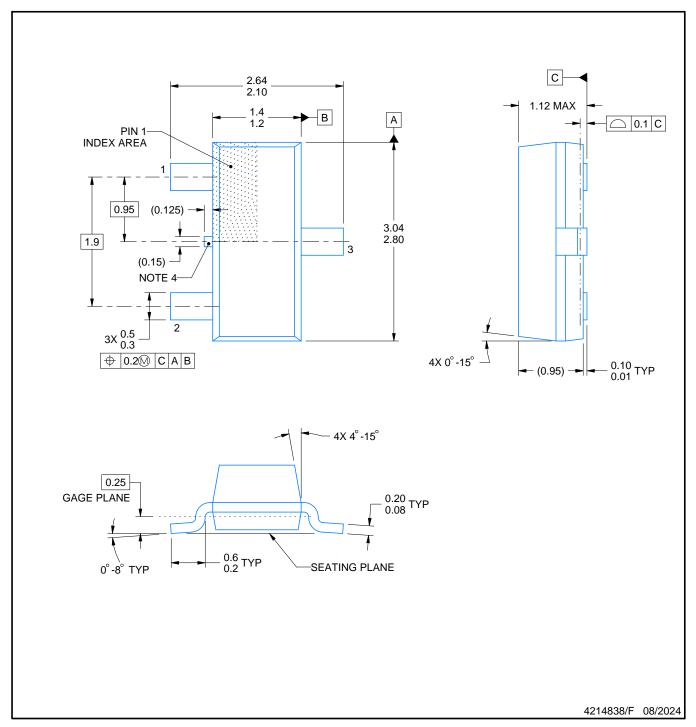


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF1112AIDBZR	SOT-23	DBZ	3	3000	200.0	183.0	25.0
REF1112AIDBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
REF1112AIDBZRG4	SOT-23	DBZ	3	3000	200.0	183.0	25.0
REF1112AIDBZT	SOT-23	DBZ	3	250	210.0	185.0	35.0
REF1112AIDBZT	SOT-23	DBZ	3	250	200.0	183.0	25.0
REF1112AIDBZTG4	SOT-23	DBZ	3	250	200.0	183.0	25.0



SMALL OUTLINE TRANSISTOR



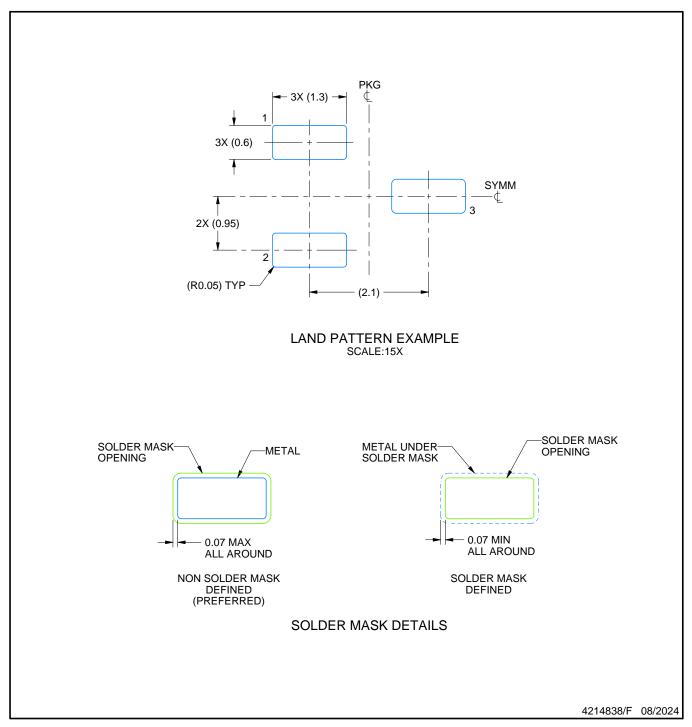
NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
 Reference JEDEC registration TO-236, except minimum foot length.

- 4. Support pin may differ or may not be present.
- 5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



SMALL OUTLINE TRANSISTOR

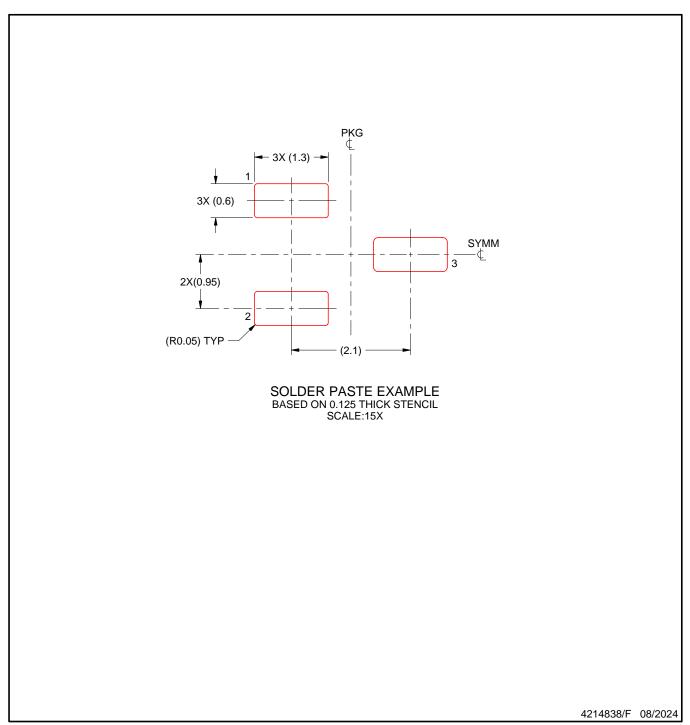


NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE TRANSISTOR



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



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