

N-Channel NexFET™ Power MOSFET

1 Features

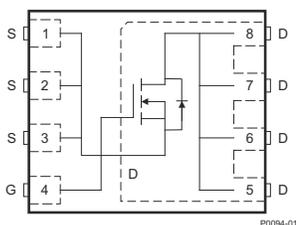
- Optimized for 5 V Gate Drive
- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

2 Applications

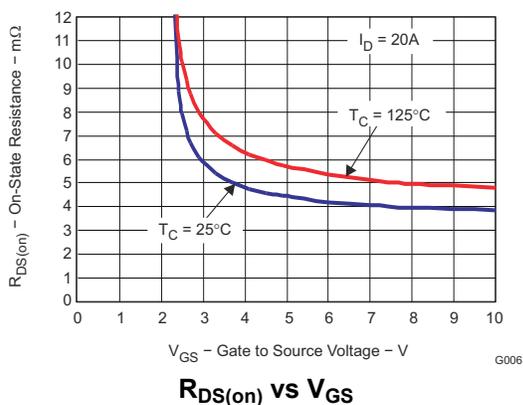
- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems
- Synchronous or Control FET Applications

3 Description

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications and optimized for 5 V gate drive applications.



Top View



$R_{DS(on)}$ vs V_{GS}

Product Summary

V_{DS}	Drain to Source Voltage	25	V
Q_g	Gate Charge Total (4.5 V)	6.8	nC
Q_{gd}	Gate Charge Gate to Drain	1.3	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V$	5.4 mΩ
		$V_{GS} = 4.5V$	4.6 mΩ
		$V_{GS} = 8V$	3.9 mΩ
$V_{GS(th)}$	Threshold Voltage	1.1	V

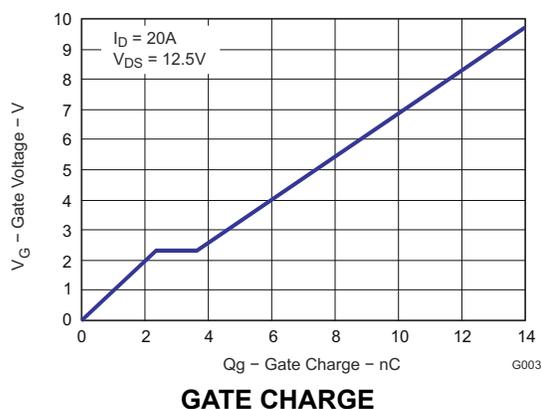
Ordering Information

Device	Package	Media	Qty	Ship
CSD16322Q5	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

Absolute Maximum Ratings

$T_A = 25^\circ C$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+10 / -8	V
I_D	Continuous Drain Current, $T_C = 25^\circ C$	97	A
	Continuous Drain Current ⁽¹⁾	21	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ C$ ⁽²⁾	136	A
P_D	Power Dissipation ⁽¹⁾	3.1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ C$
E_{AS}	Avalanche Energy, single pulse $I_D = 50 A, L = 0.1 mH, R_G = 25 \Omega$	125	mJ

- (1) Typical $R_{\theta JA} = 39^\circ C/W$ on 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.
- (2) Pulse duration $\leq 300 \mu s$, duty cycle $\leq 2\%$



GATE CHARGE



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2010) to Revision C (October 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	7
Changes from Revision A (April 2010) to Revision B (May 2010)	Page
• Changed $R_{DS(on)}$, $V_{GS} = 3\text{ V}$ in the Electrical Characteristics table From: 7 To: 7.2 in the max column.....	3
Changes from Revision * (August 2009) to Revision A (April 2010)	Page
• Changed Note1 of the ABSOLUTE MAXIMUM RATINGS From: $R_{\theta JA} = 39^{\circ}\text{C/W}$ To: Typical $R_{\theta JA} = 39^{\circ}\text{C/W}$..	1
• Changed Figure 7-1 text From: $R_{\theta JA} = 99^{\circ}\text{C/W}$ To: Typical $R_{\theta JA} = 98^{\circ}\text{C/W}$	4
• Changed Figure 7-10 text From: $R_{\theta JA} = 99^{\circ}\text{C/W}$ To: Typical $R_{\theta JA} = 98^{\circ}\text{C/W}$	4
• Changed Figure 7-11 X-axis values.....	4

5 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

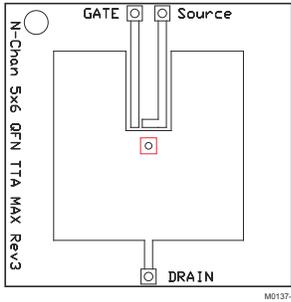
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
V_{DSS}	Drain to Source Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	25			V
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = +10/-8\text{ V}$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.9	1.1	1.4	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3\text{ V}, I_D = 20\text{ A}$		5.4	7.2	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		4.6	5.8	m Ω
		$V_{GS} = 8\text{ V}, I_D = 20\text{ A}$		3.9	5	m Ω
g_{fs}	Transconductance	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		106		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 12.5\text{ V},$ $f = 1\text{ MHz}$		1050	1365	pF
C_{oss}	Output Capacitance			740	950	pF
C_{riss}	Reverse Transfer Capacitance			55	70	pF
R_G	Series Gate Resistance		1.1	2.2		Ω
Q_g	Gate Charge Total (4.5 V)	$V_{DS} = 12.5\text{ V},$ $I_D = 20\text{ A}$		6.8	9.7	nC
Q_{gd}	Gate Charge Gate to Drain			1.3		nC
Q_{gs}	Gate Charge Gate to Source			2.4		nC
$Q_{g(th)}$	Gate Charge at V_{th}			1.3		nC
Q_{oss}	Output Charge	$V_{DS} = 13\text{ V}, V_{GS} = 0\text{ V}$		17		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 12.5\text{ V}, V_{GS} = 4.5\text{ V},$ $I_D = 20\text{ A}, R_G = 2\ \Omega$		6.1		ns
t_r	Rise Time			10.7		ns
$t_{d(off)}$	Turn Off Delay Time			12.3		ns
t_f	Fall Time			3.7		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{SD} = 20\text{ A}, V_{GS} = 0\text{ V}$		0.8	1	V
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 13\text{ V}, I_F = 20\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		19		nC
t_{rr}	Reverse Recovery Time	$V_{DD} = 13\text{ V}, I_F = 20\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		21		ns

6 Thermal Characteristics

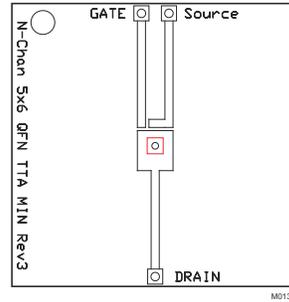
($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			2.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^{(1) (2)}			50	$^\circ\text{C}/\text{W}$

- $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



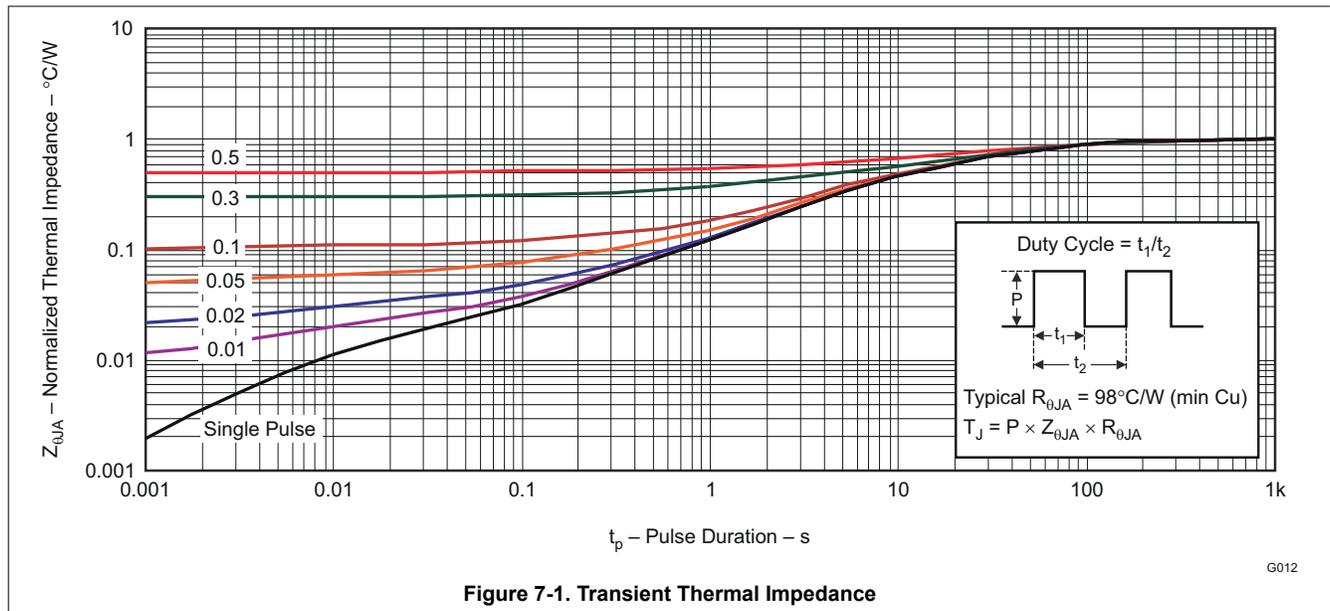
Max $R_{\theta JA}$ = 50°C/W
when mounted on 1 inch²
(6.45 cm²) of 2-oz. (0.071-
mm thick) Cu.



Max $R_{\theta JA}$ = 123°C/W when
mounted on minimum pad
area of 2-oz. (0.071-mm
thick) Cu.

7 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)



7 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

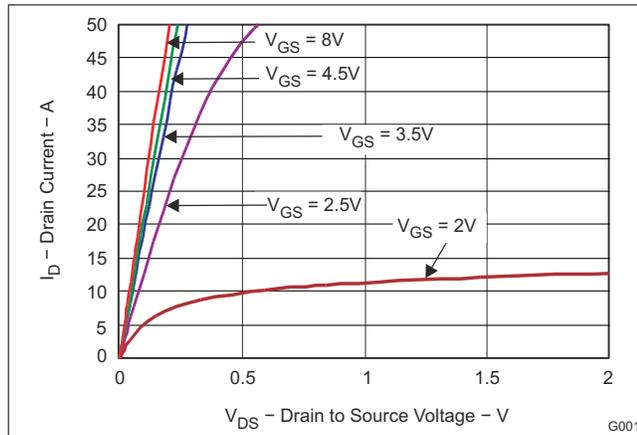


Figure 7-2. Saturation Characteristics

G001

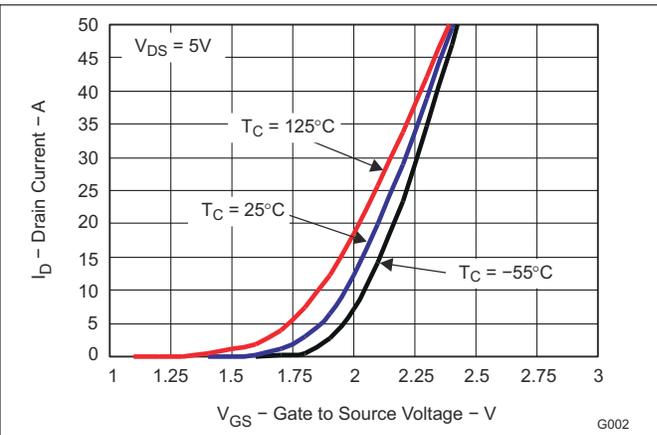


Figure 7-3. Transfer Characteristics

G002

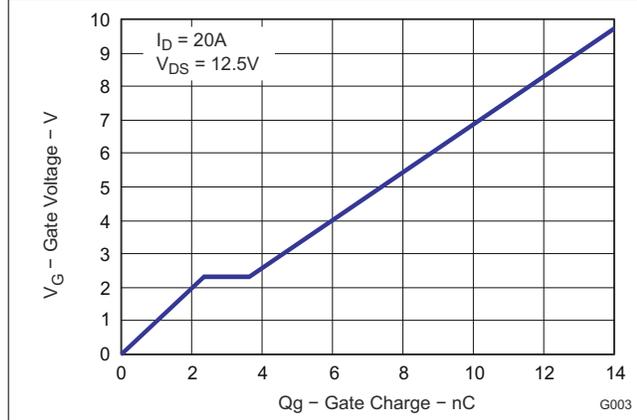


Figure 7-4. Gate Charge

G003

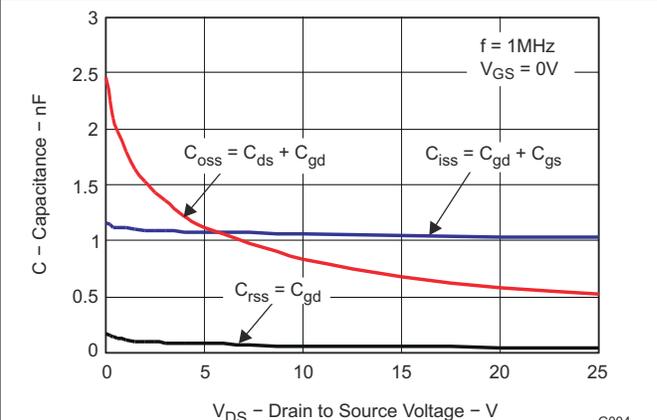


Figure 7-5. Capacitance

G004

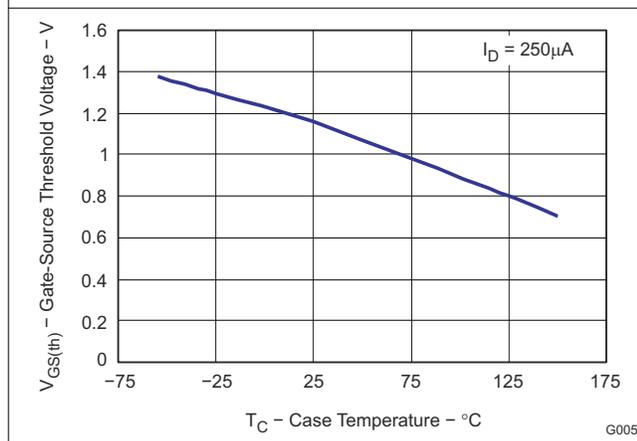


Figure 7-6. Threshold Voltage vs. Temperature

G005

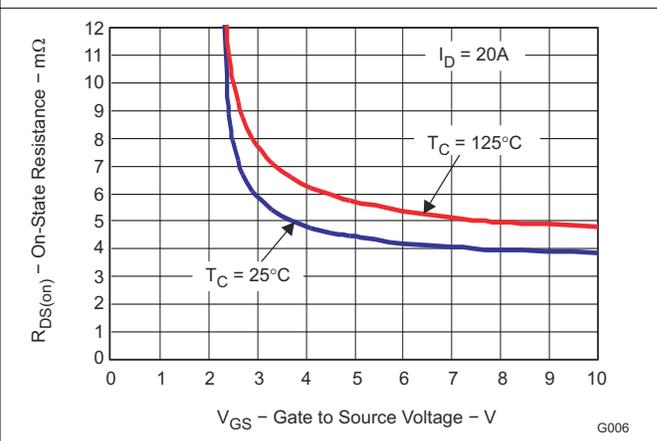


Figure 7-7. On-State Resistance vs. Gate to Source Voltage

G006

7 Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

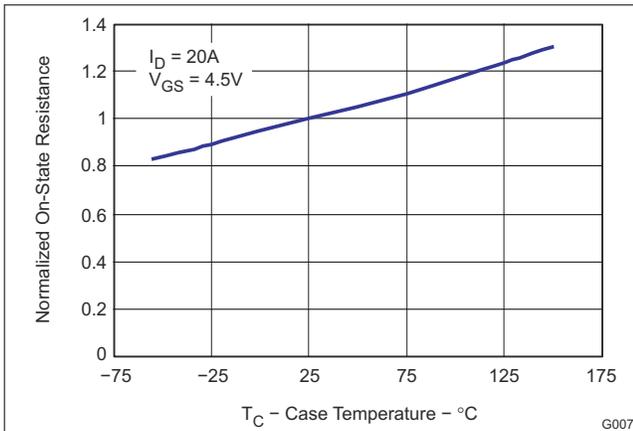


Figure 7-8. Normalized On-State Resistance vs. Temperature

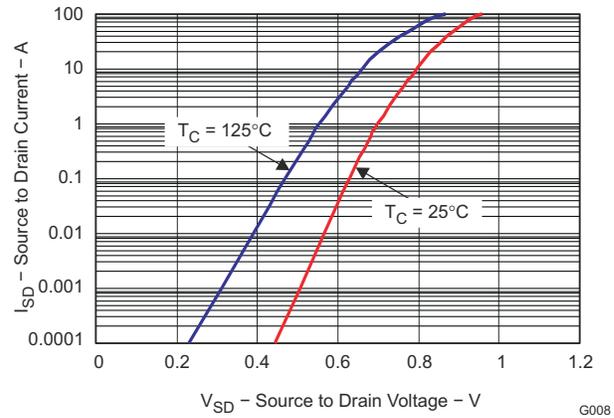


Figure 7-9. Typical Diode Forward Voltage

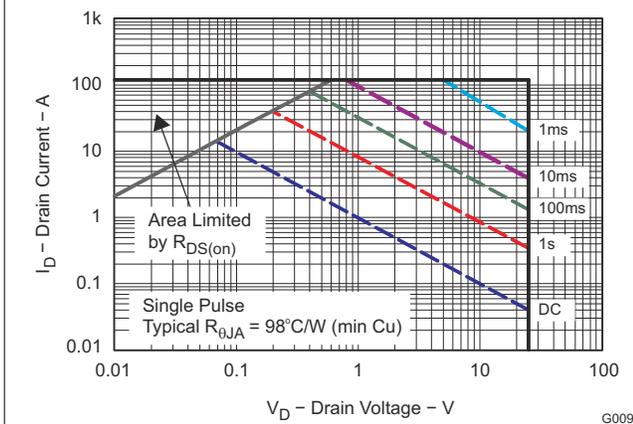


Figure 7-10. Maximum Safe Operating Area

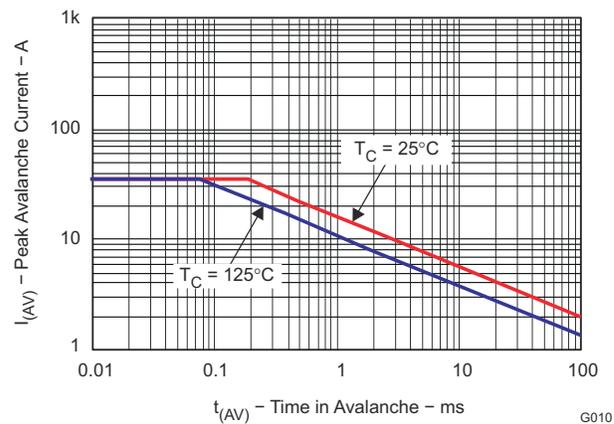


Figure 7-11. Single Pulse Unclamped Inductive Switching

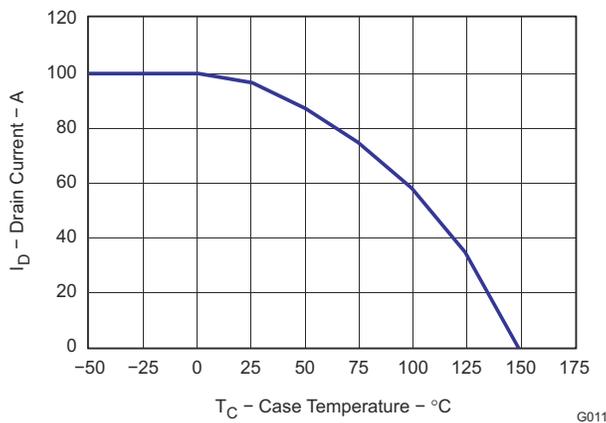


Figure 7-12. Maximum Drain Current vs. Temperature

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16322Q5	ACTIVE	VSON-CLIP	DQH	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD16322	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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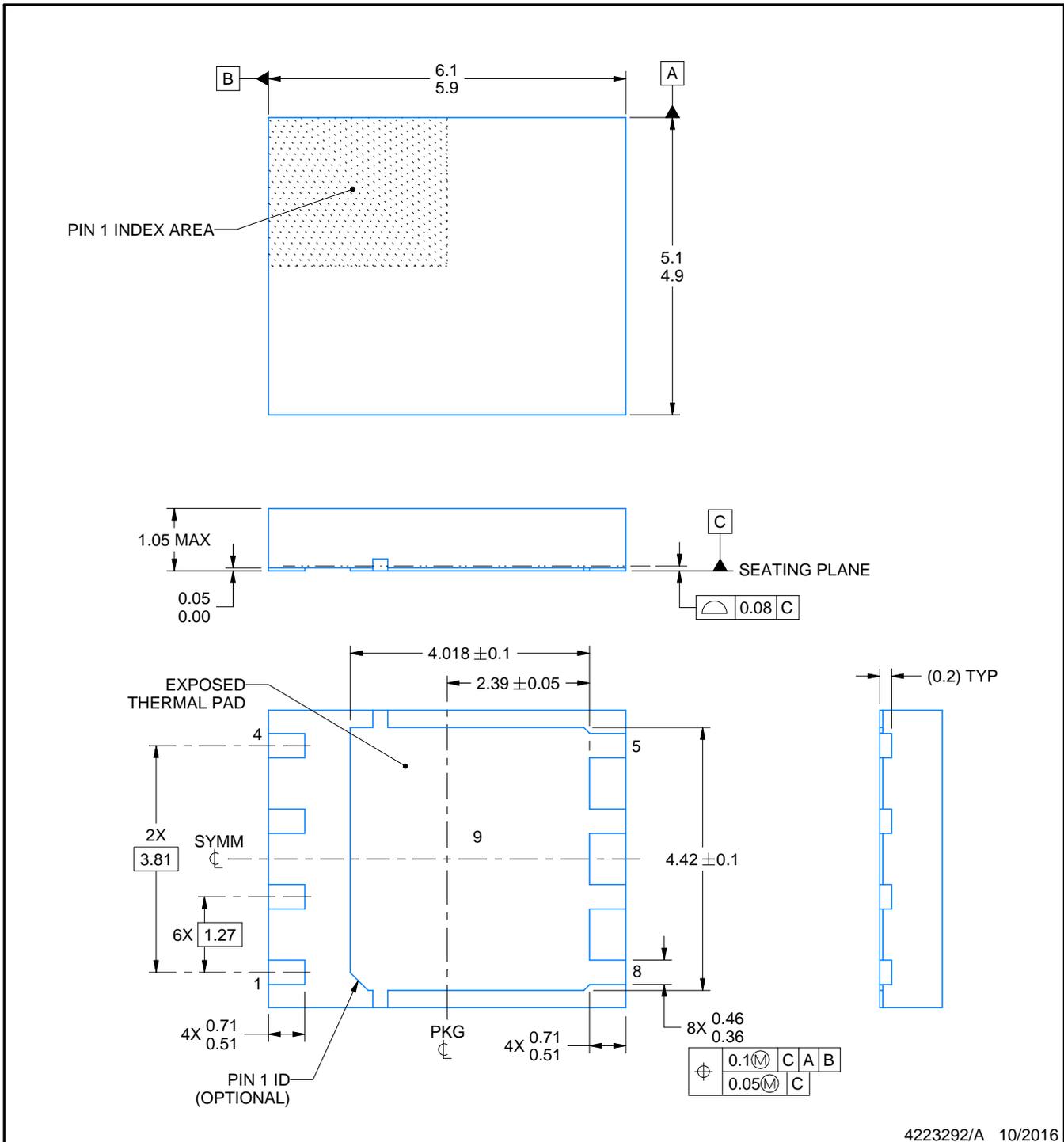
DQH0008A



PACKAGE OUTLINE

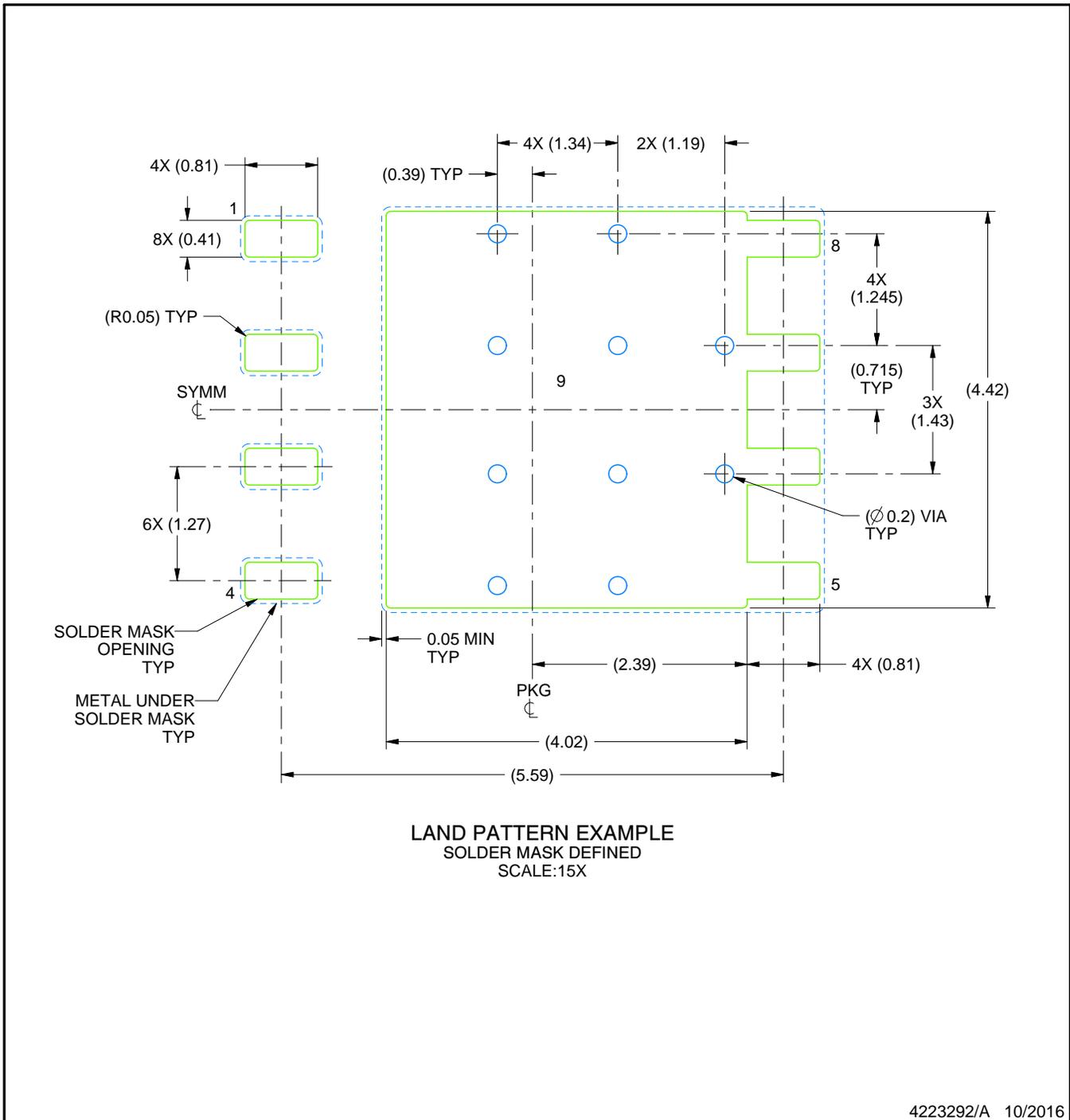
VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



NOTES: (continued)

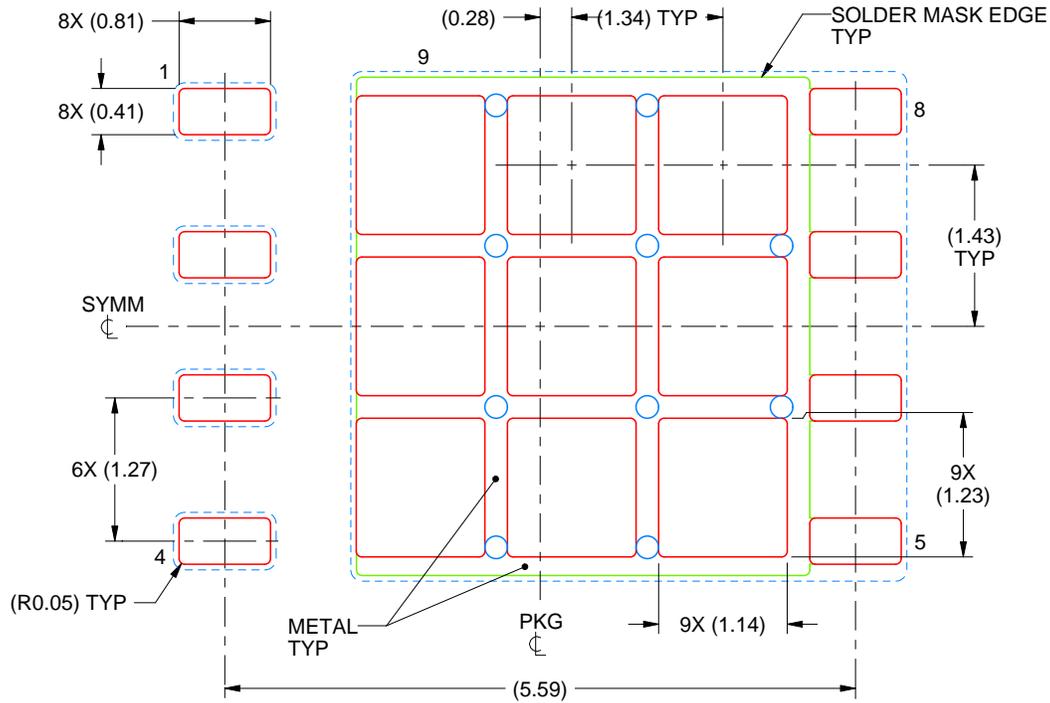
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sl原因271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DQH0008A

VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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