LME49720 Dual High Performance, High Fidelity Audio Operational Amplifier

1 Features

- Easily Drives 600Ω Loads
- Optimized for Superior Audio Signal Fidelity
- Output Short Circuit Protection
- PSRR and CMRR Exceed 120dB (typ)
- SOIC, PDIP, TO-99 Metal Can Packages
- Key Specifications
  - Power Supply Voltage Range: ±2.5 to ±17V
  - THD+N (A_V = 1, V_{OUT} = $3V_{RMS}$, f_{IN} = 1kHz):
    - R_L = 2kΩ: 0.00003% (typ)
    - R_L = 600Ω: 0.00003% (typ)
  - Input Noise Density: 2.7nV/√Hz (typ)
  - Slew Rate: ±20V/μs (typ)
  - Gain Bandwidth Product: 55MHz (typ)
  - Open Loop Gain (R_L = 600Ω): 140dB (typ)
  - Input Bias Current: 10nA (typ)
  - Input Offset Voltage: 0.1mV (typ)
  - DC Gain Linearity Error: 0.000009%

2 Applications

- Ultra High Quality Audio Amplification
- High Fidelity Preamplifiers
- High Fidelity Multimedia
- State of the Art Phono Pre Amps
- High Performance Professional Audio
- High Fidelity Equalization and Crossover Networks
- High Performance Line Drivers
- High Performance Line Receivers
- High Fidelity Active Filters

3 Description

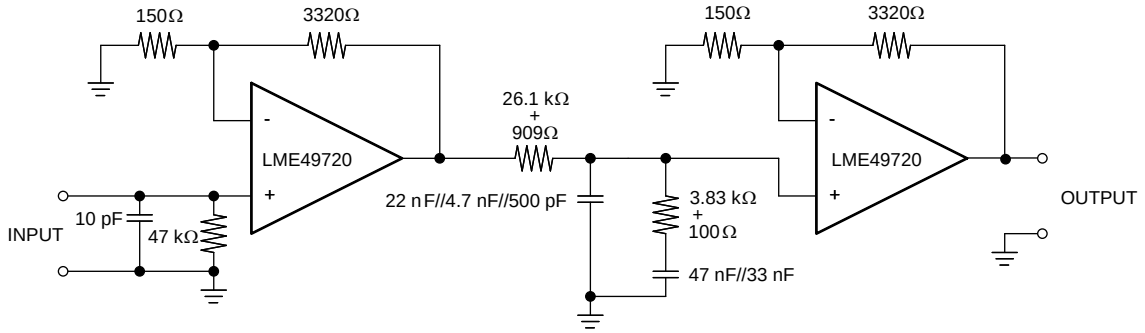
The LME49720 device is part of the ultra-low distortion, low noise, high slew rate operational amplifier series optimized and fully specified for high performance, high fidelity applications. Combining advanced leading-edge process technology with state-of-the-art circuit design, the LME49720 audio operational amplifiers deliver superior audio signal amplification for outstanding audio performance. The LME49720 combines extremely low voltage noise density (2.7nV/√Hz) with vanishingly low THD+N (0.00003%) to easily satisfy the most demanding audio applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LME49720	TO-99 (8)	9.08mm × 9.08mm
	SOIC (8)	4.90mm × 3.91mm
	PDIP (8)	9.81mm × 6.35mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Passively Equalized RIAA Phono Preamplifier



Note: 1% metal film resistors, 5% polypropylene capacitors

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (April 2013) to Revision D	Page
• Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Changed $R_{\theta JA}$ values for D and P packages from 145 °C/W to 107.9 °C/W (D) and from 102 °C/W to 72.9 °C/W (P) in the *Thermal Information* table.	4

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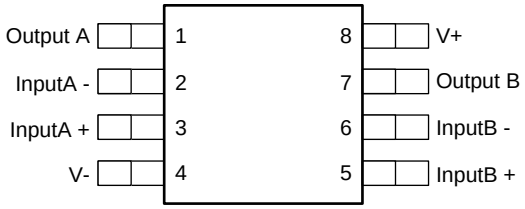
5 Device Comparison Table

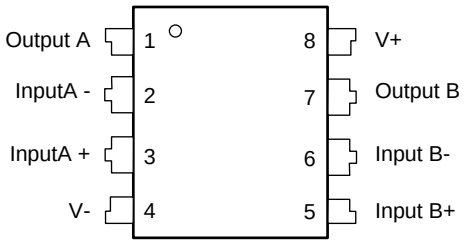
Device Number	Amplifier Type	Number of Channel	Output Current (mA)	Input Noise Density (nV/rtHz)	THD+N (%)
LME49710	Audio Operational	1	37	2.5	0.00003
LME49720	Audio Operational	2	26	2.7	0.00003
LME49721	Audio Operational	2	100	4	0.0002
LME49723	Audio Operational	2	25	3.2	0.0002

6 Pin Configuration and Functions

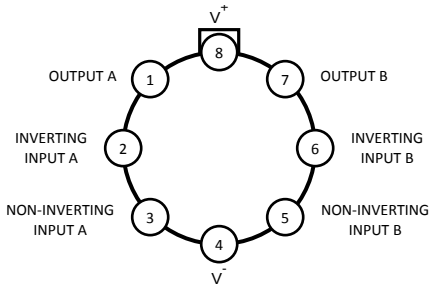
D Package
8 Pin SOIC
Top View



P Packages
8 Pin PDIP
Top View



LMC Package
8 Lead TO-99



Pin Functions

PIN				I/O	DESCRIPTION
NAME	SOIC	PDIP	TO-99		
V+	8	8	8	-	Positive supply voltage
V-	4	4	4	-	Negative supply voltage
InputA-	2	2	2	I	Negative audio input
InputA+	3	3	3	I	Positive audio input
Output A	1	1	1	O	Audio output A
InputB–	6	6	6	I	Negative audio input
InputB+	5	5	5	I	Positive audio input
Output B	7	7	7	O	Audio output B

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7 Specifications

7.1 Absolute Maximum Ratings

see [1][2][3]

		MIN	MAX	UNIT
Power Supply Voltage	($V_S = V^+ – V^–$)		36	V
Input Voltage		(V–) – 0.7V	(V+) + 0.7	V
Output Short Circuit [4]		Continuous		
Power Dissipation		Internally Limited		
Junction Temperature			150	°C
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	–40	85	°C
Supply Voltage Range		±2.5V ≤ V_S ≤ ± 17V		V
Storage Temperature		−65	150	°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
(2) Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For enusred specifications and test conditions, see Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) Amplifier output connected to GND, any number of amplifiers within a package.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) [1]	All pins	2000	V
		Machine Model (MM), per EIAJ IC-121-1981*Application and Implementation*	Pins 1, 4, 7 and 8	200	
			Pins 2, 3, 5 and 6	100	

(1) Human body model, 100pF discharged through a 1.5kΩ resistor.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+,V–	Supply voltage	±2.5		±17	V
T_A	Operating free-air temperature	–40		85	°C
T_J	Operating junction temperature	–40		150	°C

7.4 Thermal Information

THERMAL METRIC[1]		LME49720			UNIT
		D (SOIC)	P (PDIP)	LMC (TO-99)[2]	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.9	72.9	150	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52	77.2	35	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	48.3	44.9	–	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.2	35.7	–	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.8	49.9	–	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Thermal performance of a TO-99 package will depend strongly on mounting condition and there is no standard mounting configuration on a JEDEC PCB for that package type.

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7.5 Electrical Characteristics

The following specifications apply for V_S = ±15V, R_L = 2kΩ, f_{IN} = 1kHz, and T_A = 25°C, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
THD+N	Total harmonic distortion + noise	A_V = 1, V_{OUT} = 3V_{rms} R_L = 2kΩ R_L = 600Ω		0.00003 0.00003	0.00009	%
IMD	Intermodulation distortion	A_V = 1, V_{OUT} = 3V_{RMS} Two-tone, 60Hz & 7kHz 4:1		0.00005		%
GBWP	Gain bandwidth product		45	55		MHz
SR	Slew rate		±15	±20		V/µs
FPBW	Full power bandwidth	V_{OUT} = 1V_{P-P}, –3dB referenced to output magnitude at f = 1kHz		10		MHz
t_s	Settling time	A_V = –1, 10V step, C_L = 100pF 0.1% error range		1.2		µs
e_n	Equivalent input noise voltage	f_{BW} = 20Hz to 20kHz		0.34	0.65	µV_{RMS}
	Equivalent input noise density	f = 1kHz f = 10Hz		2.7 6.4	4.7	nV/√Hz
i_n	Current noise density	f = 1kHz f = 10Hz		1.6 3.1		pA/√Hz
V_{OS}	Offset voltage			±0.1	±0.7	mV
$\Delta V_{OS}/\Delta Temp$	Average input offset voltage drift vs temperature	–40°C ≤ T_A ≤ 85°C		0.2		µV/°C
PSRR	Average input offset voltage shift vs power supply voltage	ΔV_S = 20V (3)	110	120		dB
ISO_{CH-CH}	Channel-to-Channel isolation	f_{IN} = 1kHz f_{IN} = 20kHz		118 112		dB
I_B	Input bias current	V_{CM} = 0V		10	72	nA
$\Delta I_{OS}/\Delta Temp$	Input bias current drift vs temperature	–40°C ≤ T_A ≤ 85°C		0.1		nA/°C
I_{OS}	Input offset current	V_{CM} = 0V		11	65	nA
V_{IN-CM}	Common-Mode input voltage range		(V+) – 2.0 (V-) + 2.0	+14.1 –13.9		V
CMRR	Common-Mode rejection	–10V<Vcm<10V	110	120		dB
Z_{IN}	Differential input impedance			30		kΩ
	Common mode input impedance	–10V<Vcm<10V		1000		MΩ
A_{VOL}	Open loop voltage gain	–10V<Vout<10V, R_L = 600Ω	125	140		dB
		–10V<Vout<10V, R_L = 2kΩ		140		
		–10V<Vout<10V, R_L = 10kΩ		140		
V_{OUTMAX}	Maximum output voltage swing	R_L = 600Ω	±12.5	±13.6		V
		R_L = 2kΩ		±14.0		
		R_L = 10kΩ		±14.1		
I_{OUT}	Output current	R_L = 600Ω, V_S = ±17V	±23	±26		mA
I_{OUT-CC}	Instantaneous short circuit current			+53 –42		mA
R_{OUT}	Output impedance	f_{IN} = 10kHz Closed-Loop Open-Loop		0.01 13		Ω
C_{LOAD}	Capacitive load drive overshoot	100pF		16		%
I_S	Total quiescent current	I_{OUT} = 0mA		10	12	mA

(1) Tested limits are ensured to AOQL (Average Outgoing Quality Level).
(2) Typical specifications are specified at +25ºC and represent the most likely parametric norm.
(3) PSRR is measured as follows: V_{OS} is measured at two supply voltages, ±5V and ±15V. PSRR = | 20log($\Delta V_{OS}/\Delta V_S$) |.

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7.6 Typical Characteristics

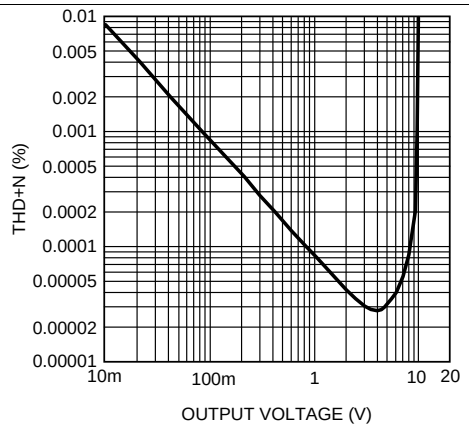

Figure 1. Thd+N vs Output Voltage V_{CC} = 15V, V_{EE} = –15V R_L = 2kΩ

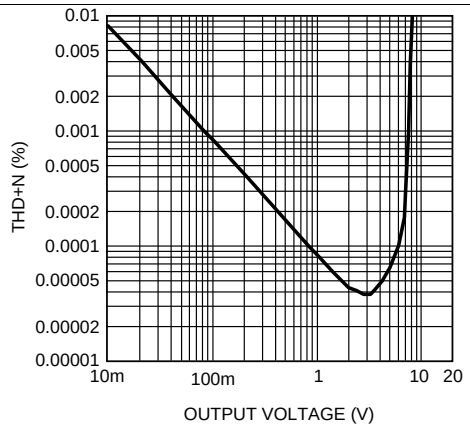

Figure 2. Thd+N vs Output Voltage V_{CC} = 12V, V_{EE} = –12v R_L = 2kΩ

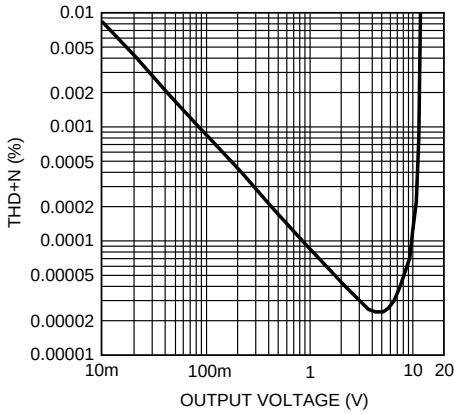

Figure 3. Thd+N vs Output Voltage V_{CC} = 17V, V_{EE} = –17v R_L = 2kΩ

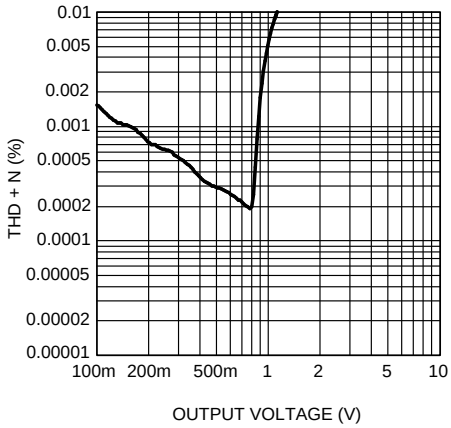

Figure 4. Thd+N vs Output Voltage V_{CC} = 2.5V, V_{EE} = –2.5V R_L = 2kΩ

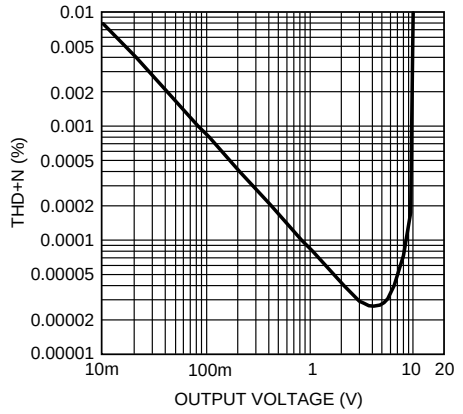

Figure 5. Thd+N vs Output Voltage V_{CC} = 15V, V_{EE} = –15V R_L = 600Ω

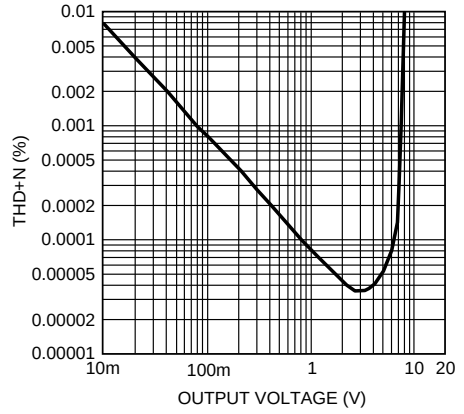

Figure 6. Thd+N vs Output Voltage V_{CC} = 12V, V_{EE} = –12V R_L = 600Ω

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Typical Characteristics (continued)

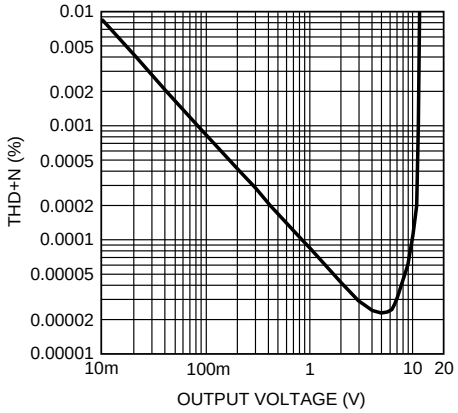

Figure 7. Thd+N vs Output Voltage V_{CC} = 17V, V_{EE} = –17V R_L = 600Ω

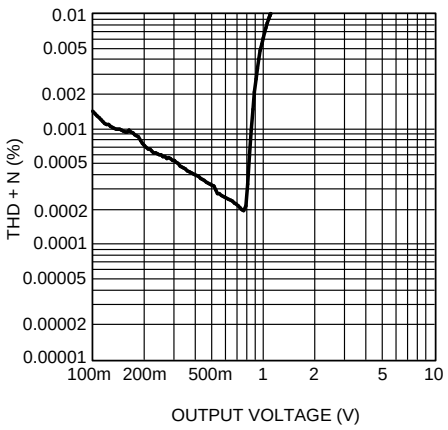

Figure 8. Thd+N vs Output Voltage V_{CC} = 2.5V, V_{EE} = –2.5V R_L = 600Ω

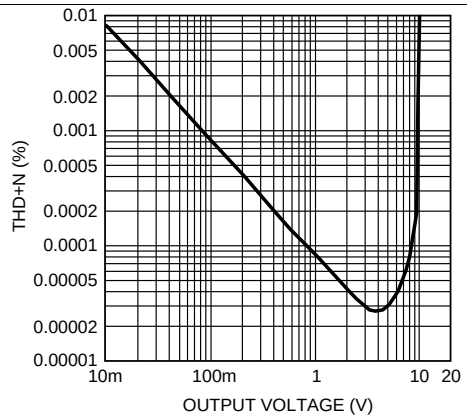

Figure 9. Thd+N vs Output Voltage V_{CC} = 15V, V_{EE} = –15V R_L = 10kΩ

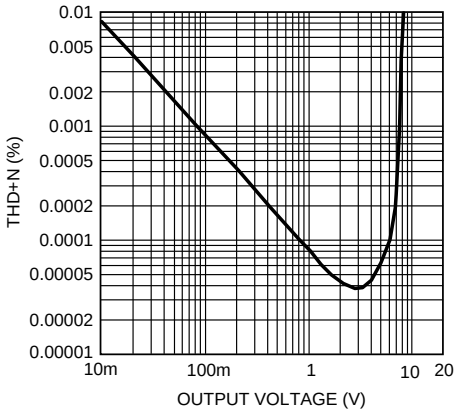

Figure 10. Thd+N vs Output Voltage V_{CC} = 12V, V_{EE} = –12V R_L = 10kΩ

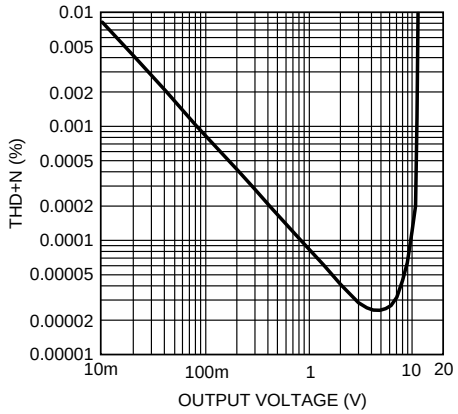

Figure 11. Thd+N vs Output Voltage V_{CC} = 17V, V_{EE} = –17V R_L = 10kΩ

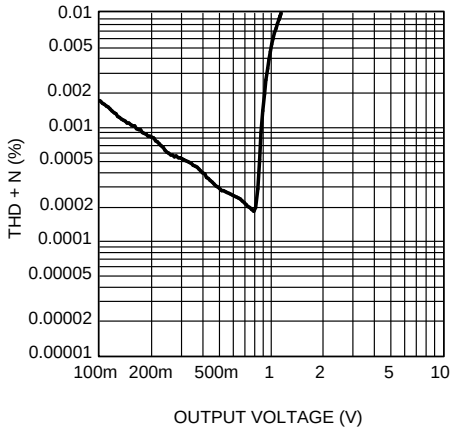

Figure 12. Thd+N vs Output Voltage V_{CC} = 2.5V, V_{EE} = –2.5V R_L = 10kΩ

Typical Characteristics (continued)

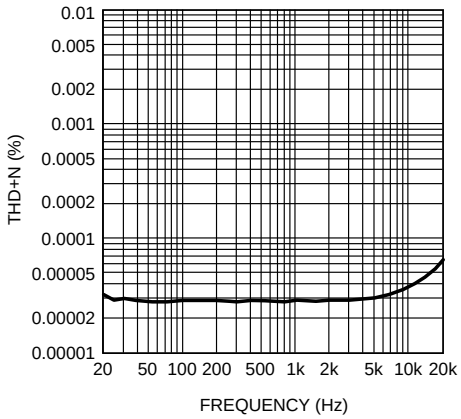

Figure 13. Thd+N vs Frequency V_{CC} = 15V, V_{EE} = –15V, V_{OUT} = 3V_{RMS} R_L = 2kΩ

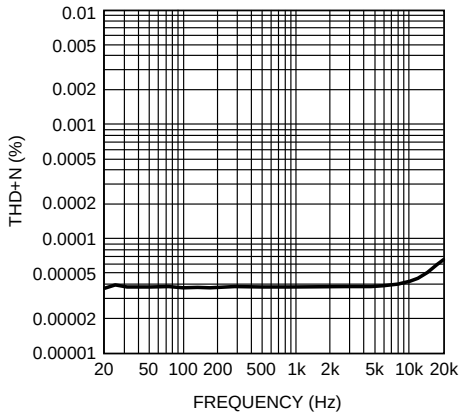

Figure 14. Thd+N vs Frequency V_{CC} = 12V, V_{EE} = –12V, V_{OUT} = 3V_{RMS} R_L = 2kΩ

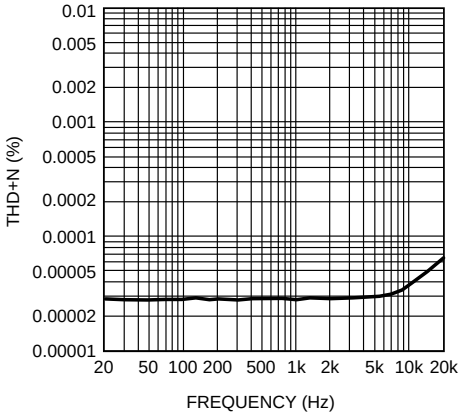

Figure 15. Thd+N vs Frequency V_{CC} = 17V, V_{EE} = –17V, V_{OUT} = 3V_{RMS} R_L = 2kΩ

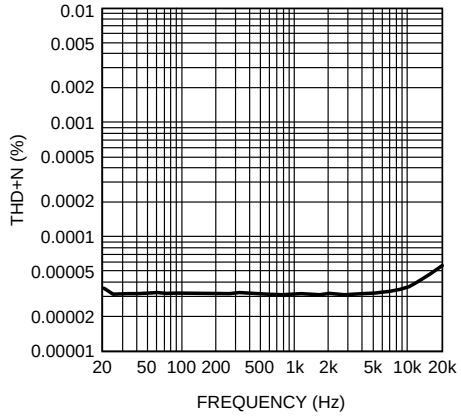

Figure 16. Thd+N vs Frequency V_{CC} = 15V, V_{EE} = –15V, V_{OUT} = 3V_{RMS} R_L = 2kΩ

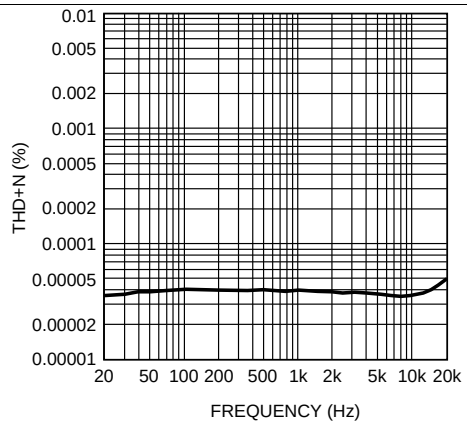

Figure 17. Thd+N vs Frequency V_{CC} = 12V, V_{EE} = –12V, V_{OUT} = 3V_{RMS} R_L = 2kΩ

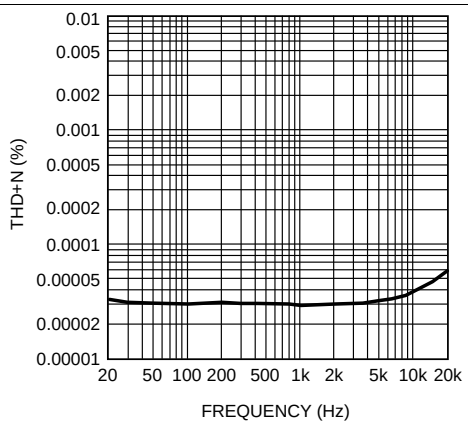

Figure 18. Thd+N vs Frequency V_{CC} = 17V, V_{EE} = –17V, V_{OUT} = 3V_{RMS} R_L = 2kΩ

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Typical Characteristics (continued)

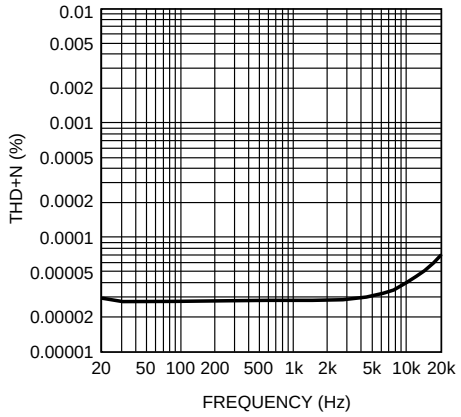

Figure 19. Thd+N vs Frequency V_{CC} = 15V, V_{EE} = –15V, V_{OUT} = $3V_{RMS}$ R_L = 10kΩ

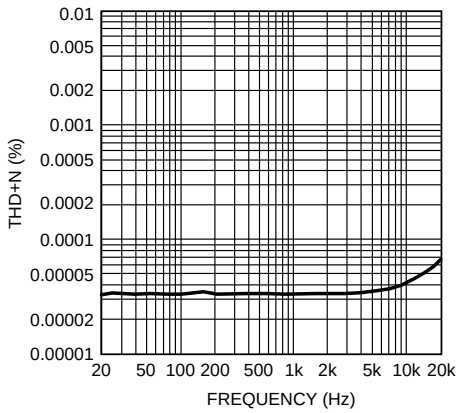

Figure 20. Thd+N vs Frequency V_{CC} = 12V, V_{EE} = –12V, V_{OUT} = $3V_{RMS}$ R_L = 10kΩ

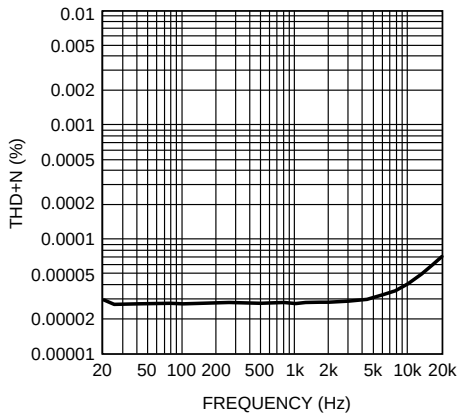

Figure 21. Thd+N vs Frequency V_{CC} = 17V, V_{EE} = –17V, V_{OUT} = $3V_{RMS}$ R_L = 10kΩ

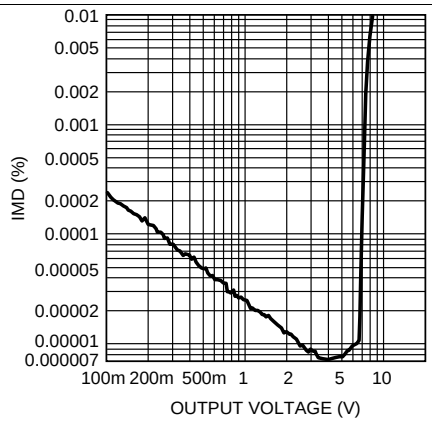

Figure 22. IMD vs Output Voltage V_{CC} = 15V, V_{EE} = –15V R_L = 2kΩ

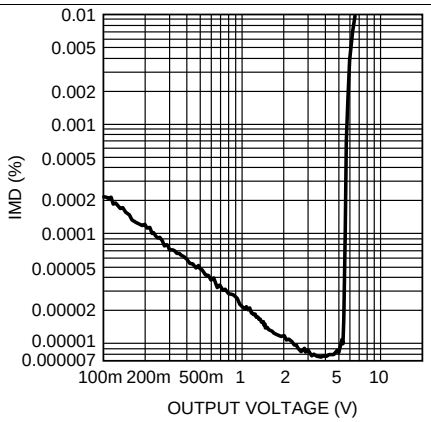

Figure 23. IMD vs Output Voltage V_{CC} = 12V, V_{EE} = –12V R_L = 2kΩ

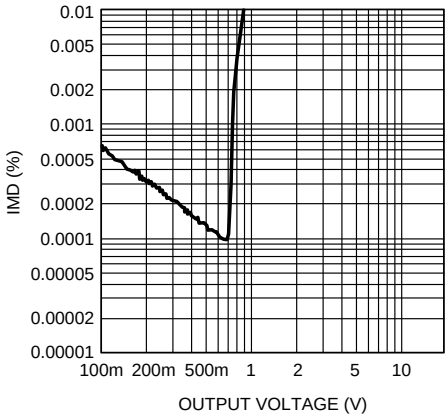

Figure 24. IMD vs Output Voltage V_{CC} = 2.5V, V_{EE} = –2.5V R_L = 2kΩ

Typical Characteristics (continued)

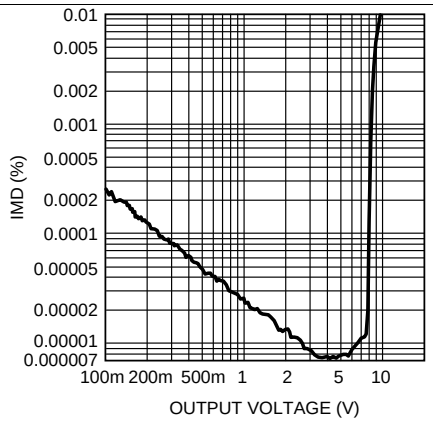

Figure 25. IMD vs Output Voltage V_{CC} = 17V, V_{EE} = –17V R_L = 2kΩ

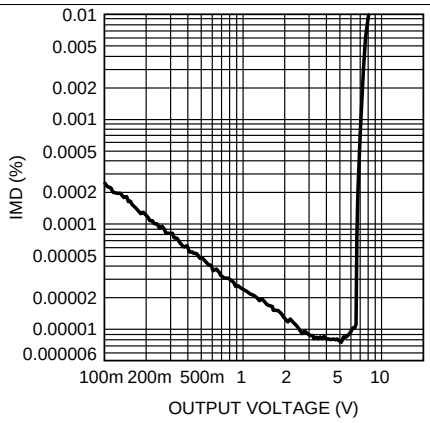

Figure 26. IMD vs Output Voltage V_{CC} = 15V, V_{EE} = –15V R_L = 600Ω

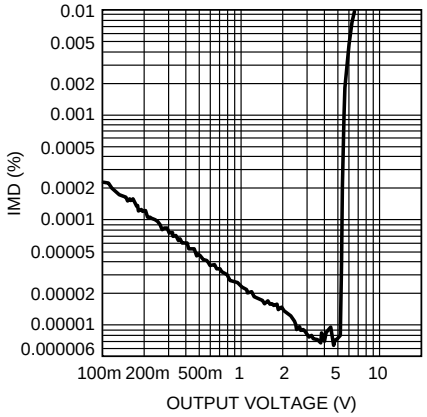

Figure 27. IMD vs Output Voltage V_{CC} = 12V, V_{EE} = –12V R_L = 600Ω

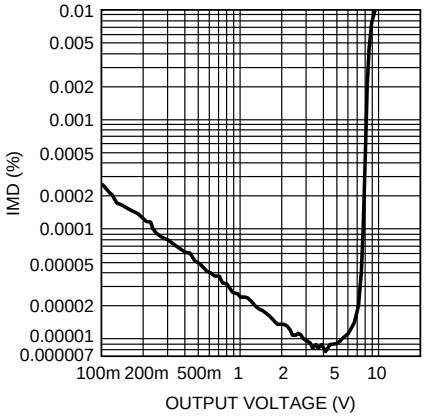

Figure 28. IMD vs Output Voltage V_{CC} = 17V, V_{EE} = –17V R_L = 600Ω

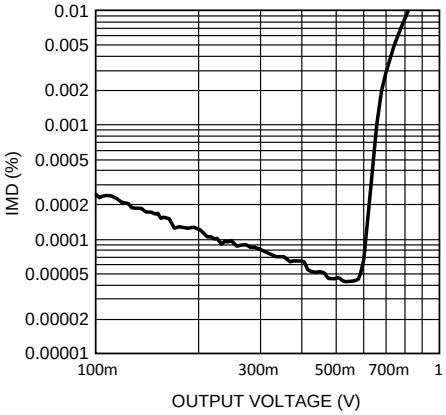

Figure 29. IMD vs Output Voltage V_{CC} = 2.5V, V_{EE} = –2.5V R_L = 600Ω

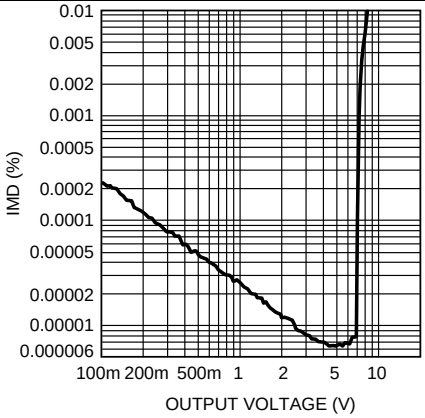

Figure 30. IMD vs Output Voltage V_{CC} = 15V, V_{EE} = –15V R_L = 10kΩ

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Typical Characteristics (continued)

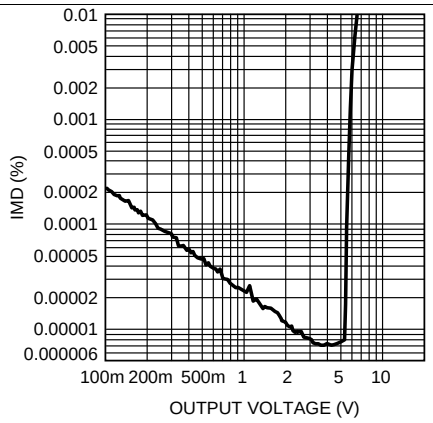

Figure 31. IMD vs Output Voltage V_{CC} = 12V, V_{EE} = –12V R_L = 10kΩ

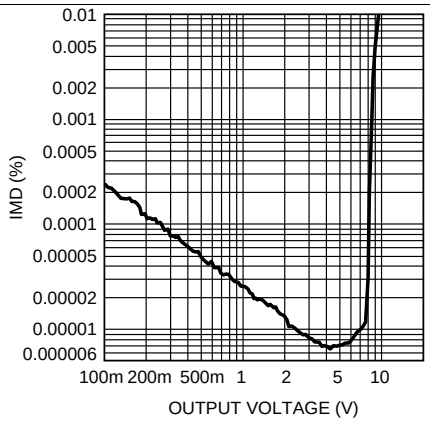

Figure 32. IMD vs Output Voltage V_{CC} = 17V, V_{EE} = –17V R_L = 10kΩ

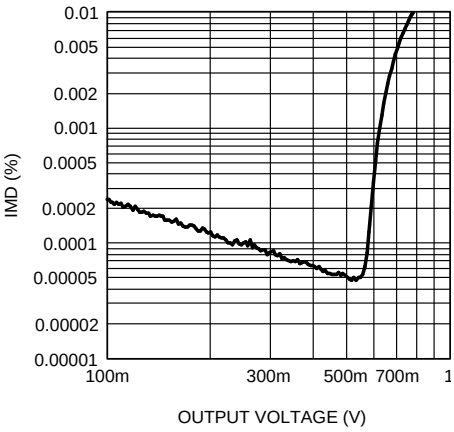

Figure 33. IMD vs Output Voltage V_{CC} = 2.5V, V_{EE} = –2.5V R_L = 10kΩ

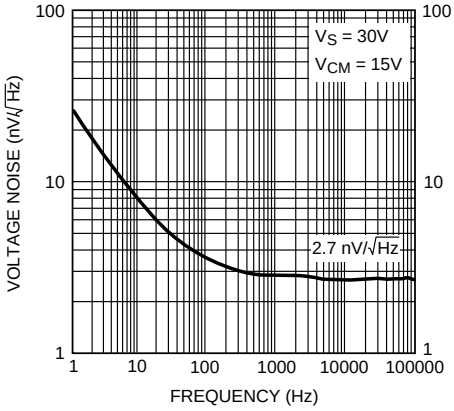

Figure 34. Voltage Noise Density vs Frequency

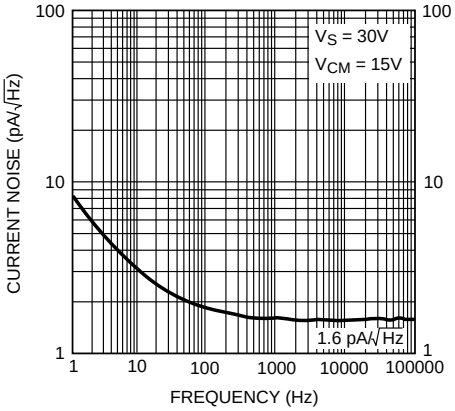

Figure 35. Current Noise Density vs Frequency

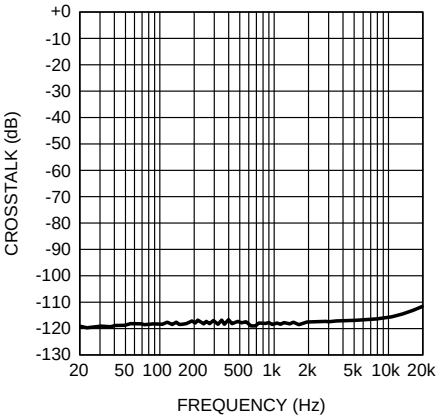

Figure 36. Crosstalk vs Frequency V_{CC} = 15V, V_{EE} = –15V, V_{OUT} = 3V_{RMS} A_V = 0dB, R_L = 2kΩ

Typical Characteristics (continued)

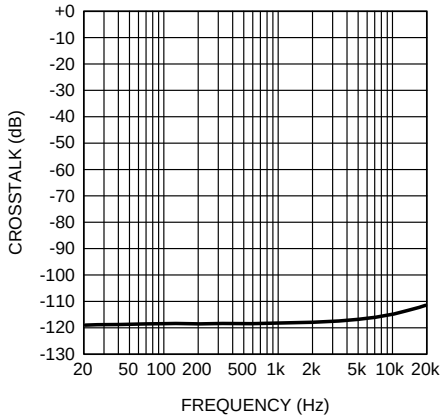

Figure 37. Crosstalk vs Frequency V_{CC} = 15V, V_{EE} = –15V, V_{OUT} = 10V_{RMS} A_V = 0dB, R_L = 2kΩ

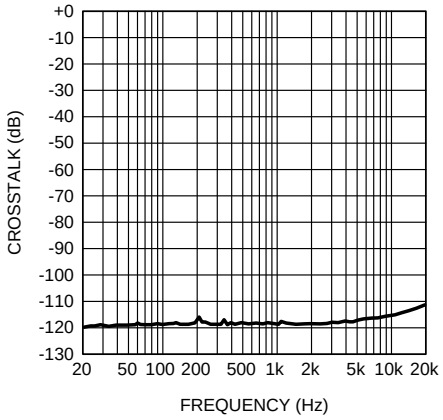

Figure 38. Crosstalk vs Frequency V_{CC} = 12V, V_{EE} = –12V, V_{OUT} = 3V_{RMS} A_V = 0dB, R_L = 2kΩ

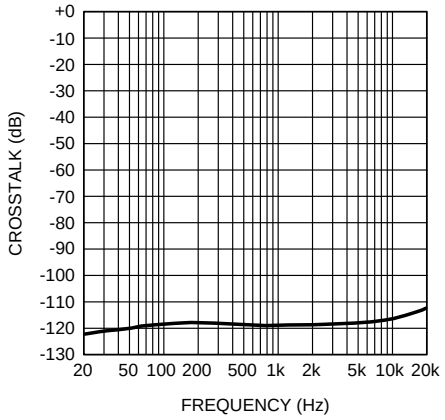

Figure 39. Crosstalk vs Frequency V_{CC} = 12V, V_{EE} = –12V, V_{OUT} = 10V_{RMS} A_V = 0dB, R_L = 2kΩ

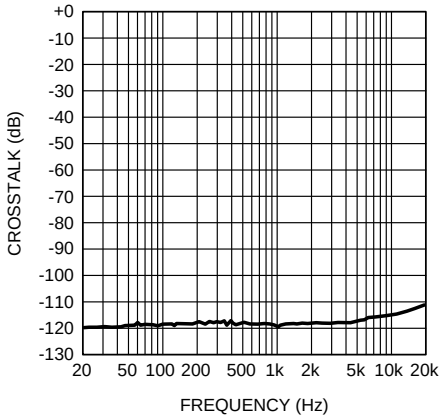

Figure 40. Crosstalk vs Frequency V_{CC} = 17V, V_{EE} = –17V, V_{OUT} = 3V_{RMS} A_V = 0dB, R_L = 2kΩ

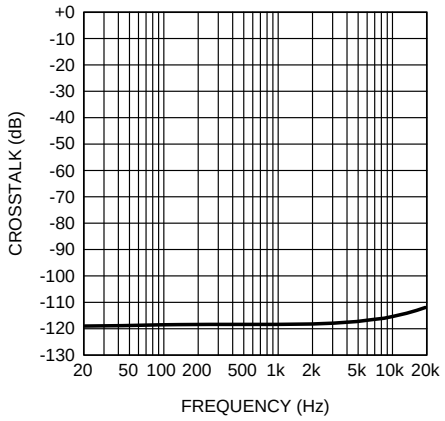

Figure 41. Crosstalk vs Frequency V_{CC} = 17V, V_{EE} = –17V, V_{OUT} = 10V_{RMS} A_V = 0dB, R_L = 2kΩ

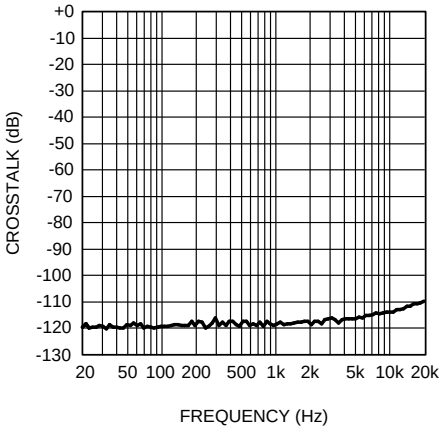

Figure 42. Crosstalk vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V, V_{OUT} = 1V_{RMS} A_V = 0dB, R_L = 2kΩ

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Typical Characteristics (continued)

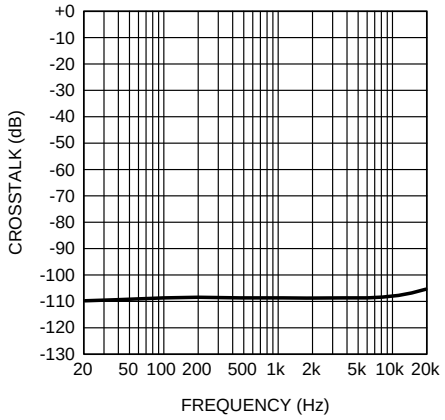

Figure 43. Crosstalk vs Frequency V_{CC} = 15V, V_{EE} = –15V, V_{OUT} = 3V_{RMS} A_V = 0dB, R_L = 600Ω

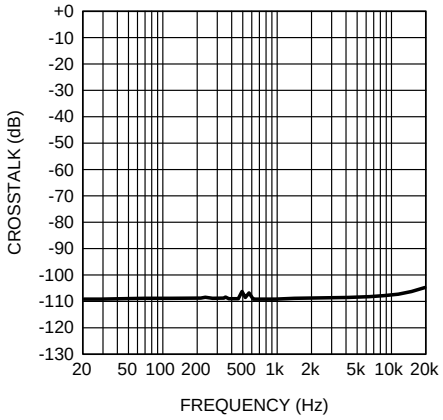

Figure 44. Crosstalk vs Frequency V_{CC} = 15V, V_{EE} = –15V, V_{OUT} = 10V_{RMS} A_V = 0dB, R_L = 600Ω

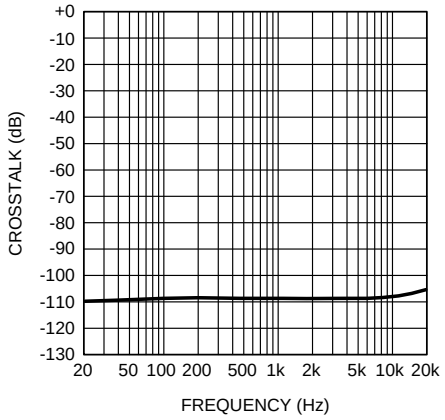

Figure 45. Crosstalk vs Frequency V_{CC} = 12V, V_{EE} = –12V, V_{OUT} = 3V_{RMS} A_V = 0dB, R_L = 600Ω

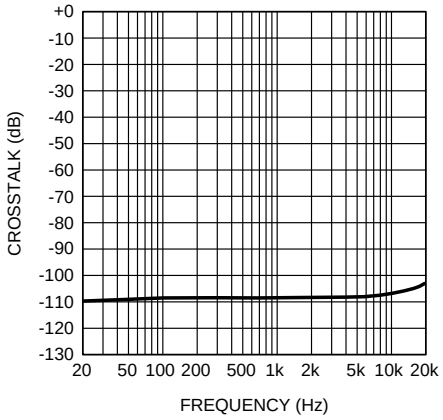

Figure 46. Crosstalk vs Frequency V_{CC} = 12V, V_{EE} = –12V, V_{OUT} = 10V_{RMS} A_V = 0dB, R_L = 600Ω

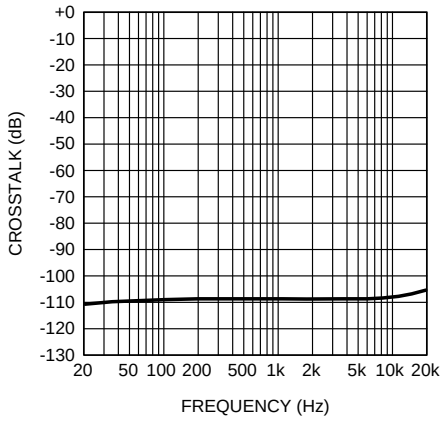

Figure 47. Crosstalk vs Frequency V_{CC} = 17V, V_{EE} = –17V, V_{OUT} = 3V_{RMS} A_V = 0dB, R_L = 600Ω

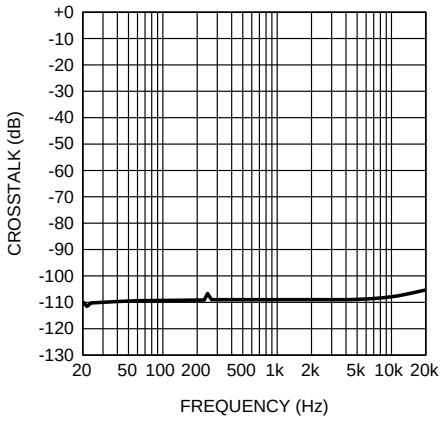

Figure 48. Crosstalk vs Frequency V_{CC} = 17V, V_{EE} = –17V, V_{OUT} = 10V_{RMS} A_V = 0dB, R_L = 600Ω

Typical Characteristics (continued)

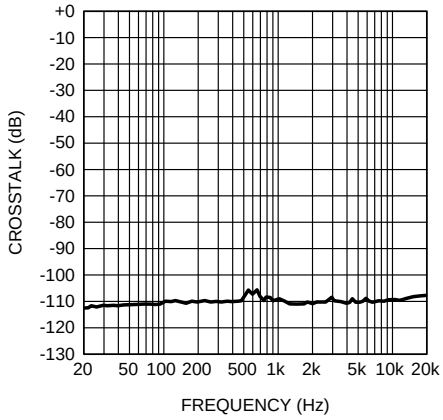

Figure 49. Crosstalk vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V, V_{OUT} = 1V_{RMS} A_V = 0dB, R_L = 600Ω

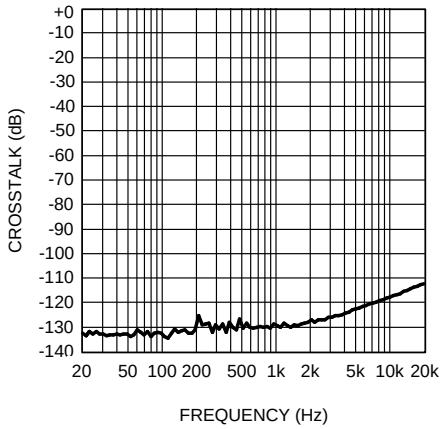

Figure 50. Crosstalk vs Frequency V_{CC} = 15V, V_{EE} = –15V, V_{OUT} = 3V_{RMS} A_V = 0dB, R_L = 10kΩ

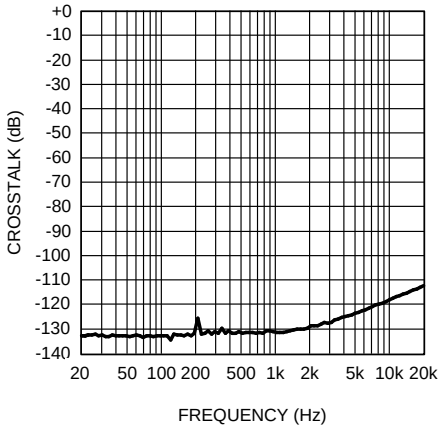

Figure 51. Crosstalk vs Frequency V_{CC} = 15V, V_{EE} = –15V, V_{OUT} = 10V_{RMS} A_V = 0dB, R_L = 10kΩ

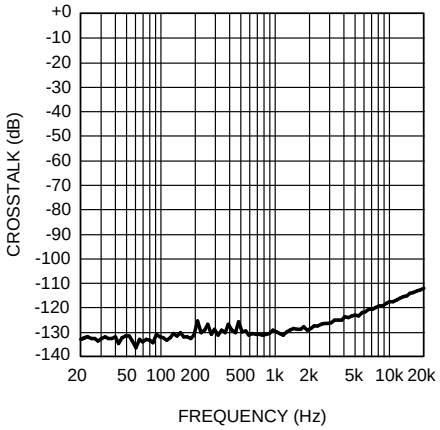

Figure 52. Crosstalk vs Frequency V_{CC} = 12V, V_{EE} = –12V, V_{OUT} = 3V_{RMS} A_V = 0dB, R_L = 10kΩ

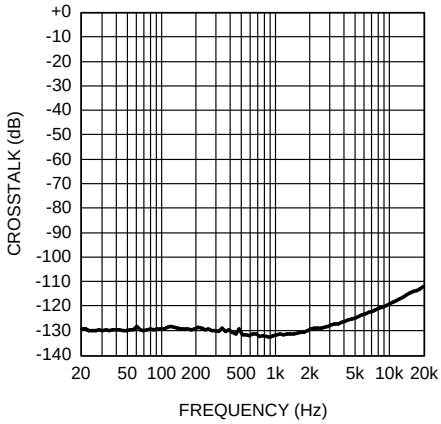

Figure 53. Crosstalk vs Frequency V_{CC} = 12V, V_{EE} = –12V, V_{OUT} = 10V_{RMS} A_V = 0dB, R_L = 10kΩ

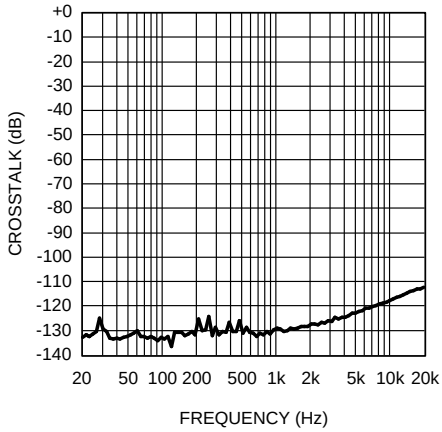

Figure 54. Crosstalk vs Frequency V_{CC} = 17V, V_{EE} = –17V, V_{OUT} = 3V_{RMS} A_V = 0dB, R_L = 10kΩ

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Typical Characteristics (continued)

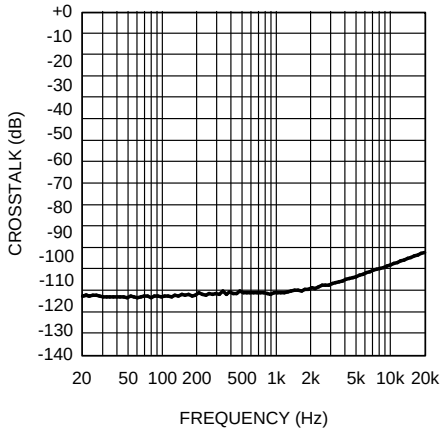

Figure 55. Crosstalk vs Frequency V_{CC} = 17V, V_{EE} = –17V, V_{OUT} = 10V_{RMS} A_V = 0dB, R_L = 10kΩ

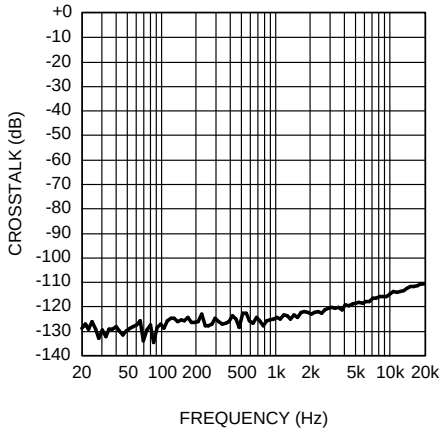

Figure 56. Crosstalk vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V, V_{OUT} = 1V_{RMS} A_V = 0dB, R_L = 10kΩ

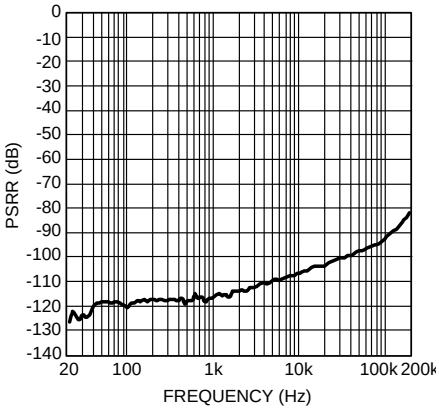

Figure 57. PSRR+ vs Frequency V_{CC} = 15V, V_{EE} = –15V R_L = 10kΩ, F = 200kHz, V_{RIPPLE} = 200mvpp

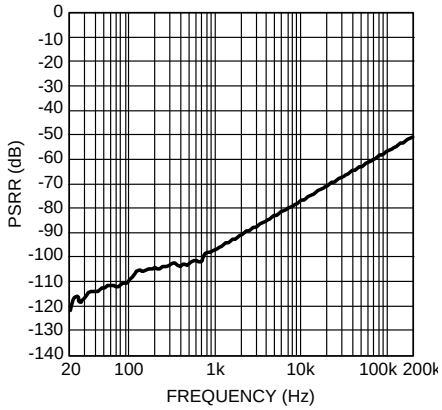

Figure 58. PSRR- vs Frequency V_{CC} = 15V, V_{EE} = –15V R_L = 10kΩ, F = 200kHz, V_{RIPPLE} = 200mvpp

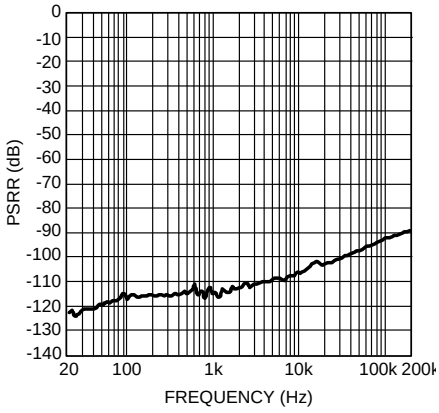

Figure 59. PSRR+ vs Frequency V_{CC} = 15V, V_{EE} = –15V R_L = 2kΩ, F = 200kHz, V_{RIPPLE} = 200mvpp

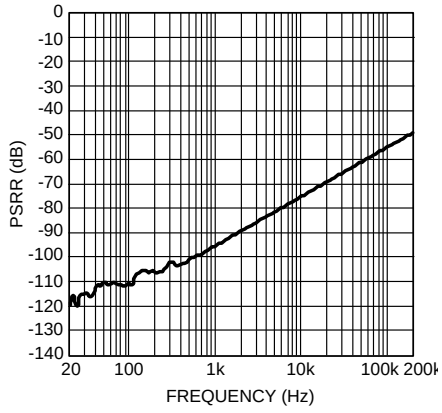

Figure 60. PSRR- vs Frequency V_{CC} = 15V, V_{EE} = –15V R_L = 2kΩ, F = 200kHz, V_{RIPPLE} = 200mvpp

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Typical Characteristics (continued)

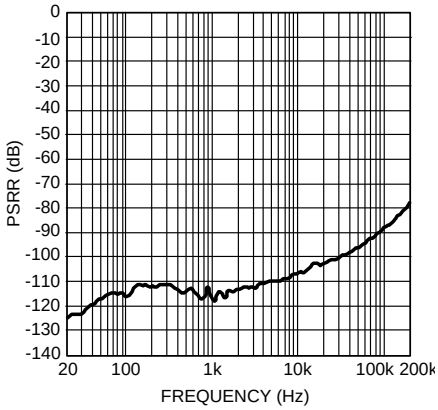

Figure 61. PSRR+ vs Frequency V_{CC} = 15V, V_{EE} = –15V R_L = 600Ω, F = 200kHz, V_{RIPPLE} = 200mvpp

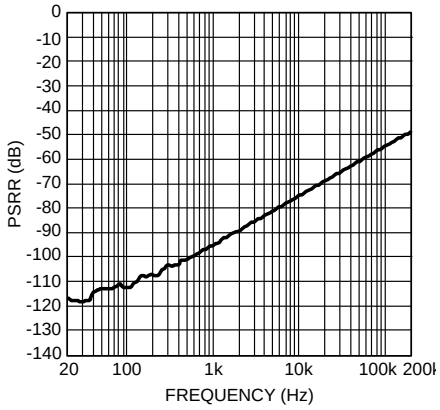

Figure 62. PSRR- vs Frequency V_{CC} = 15V, V_{EE} = –15V R_L = 600Ω, F = 200kHz, V_{RIPPLE} = 200mvpp

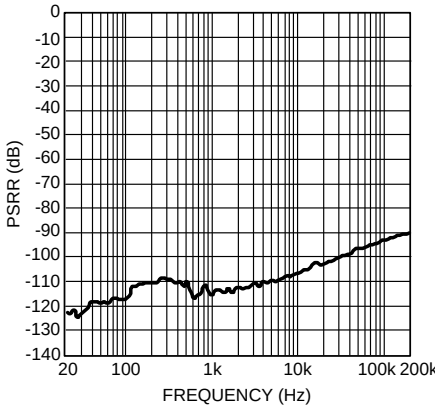

Figure 63. PSRR+ vs Frequency V_{CC} = 12V, V_{EE} = –12V R_L = 10kΩ, F = 200kHz, V_{RIPPLE} = 200mvpp

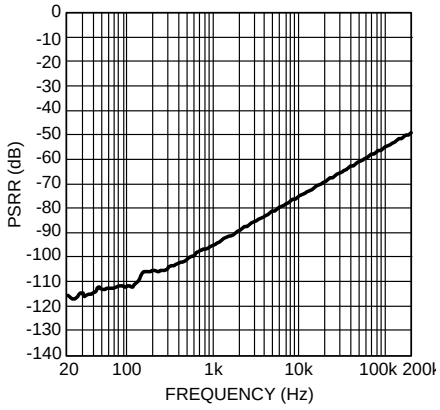

Figure 64. PSRR– vs Frequency V_{CC} = 12V, V_{EE} = –12V R_L = 10kΩ, F = 200kHz, V_{RIPPLE} = 200mvpp

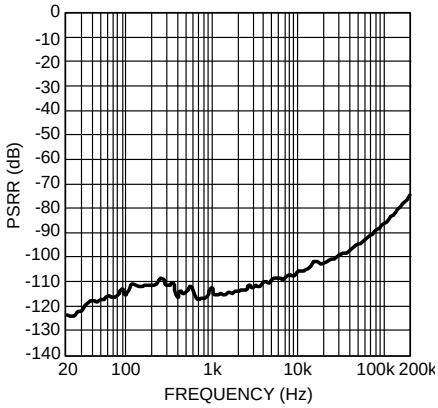

Figure 65. PSRR+ vs Frequency V_{CC} = 12V, V_{EE} = –12V R_L = 2kΩ, F = 200kHz, V_{RIPPLE} = 200mvpp

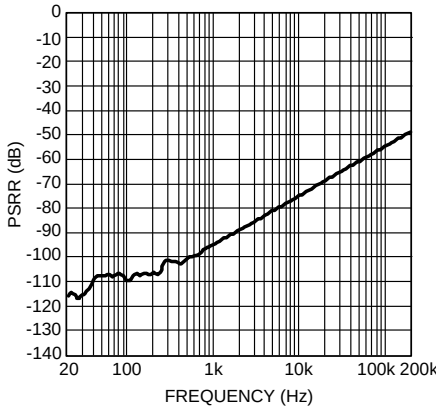

Figure 66. PSRR– vs Frequency V_{CC} = 12V, V_{EE} = –12V R_L = 2kΩ, F = 200kHz, V_{RIPPLE} = 200mvpp

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Typical Characteristics (continued)

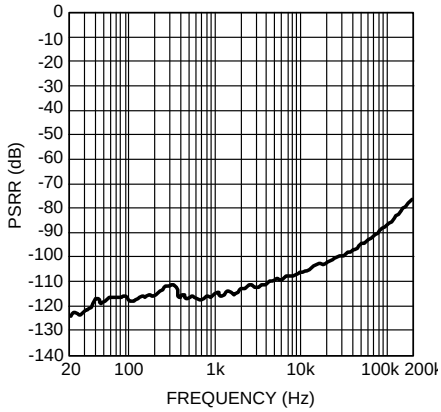

Figure 67. PSRR+ vs Frequency V_{CC} = 12V, V_{EE} = –12V R_L = 600Ω, F = 200kHz, V_{RIPPLE} = 200mvpp

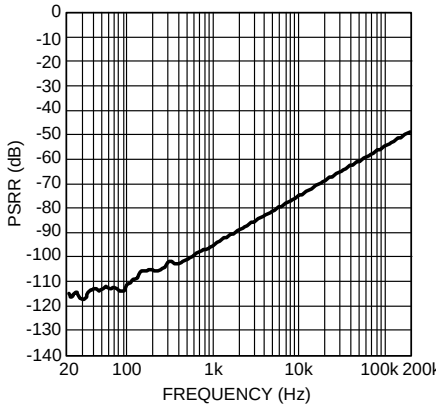

Figure 68. PSRR– vs Frequency V_{CC} = 12V, V_{EE} = –12V R_L = 600Ω, F = 200kHz, V_{RIPPLE} = 200mvpp

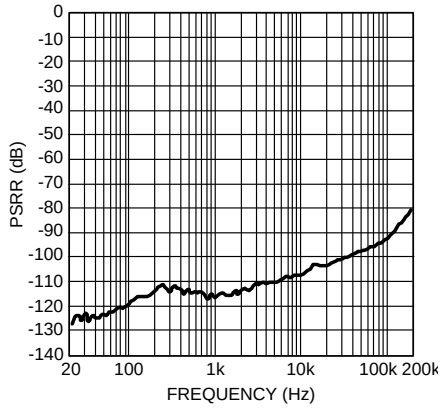

Figure 69. PSRR+ vs Frequency V_{CC} = 17V, V_{EE} = –17V R_L = 10kΩ, F = 200kHz, V_{RIPPLE} = 200mvpp

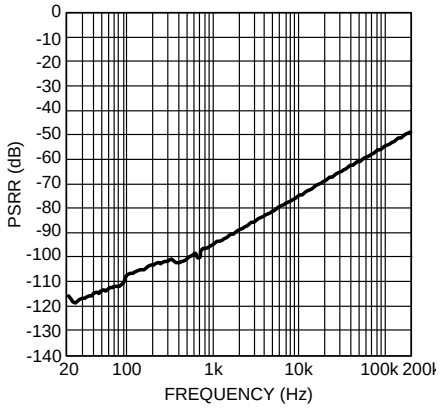

Figure 70. PSRR– vs Frequency V_{CC} = 17V, V_{EE} = –17V R_L = 10kΩ, F = 200kHz, V_{RIPPLE} = 200mvpp

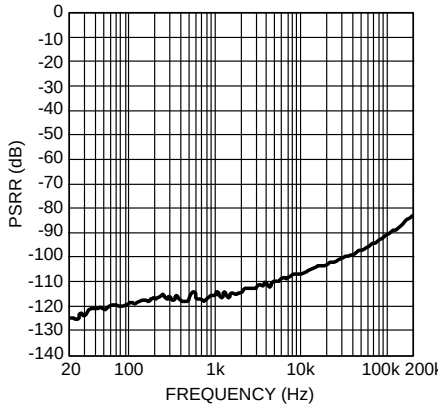

Figure 71. PSRR+ vs Frequency V_{CC} = 17V, V_{EE} = –17V R_L = 2kΩ, F = 200kHz, V_{RIPPLE} = 200mvpp

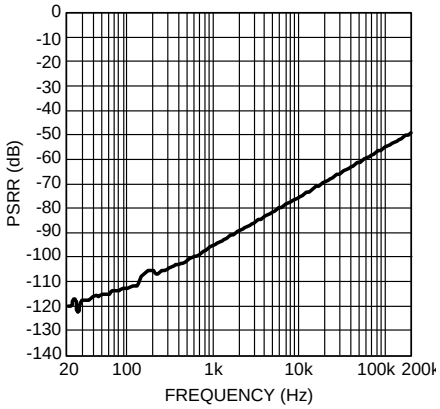

Figure 72. PSRR– vs Frequency V_{CC} = 17V, V_{EE} = –17V R_L = 2kΩ, F = 200kHz, V_{RIPPLE} = 200mvpp

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Typical Characteristics (continued)

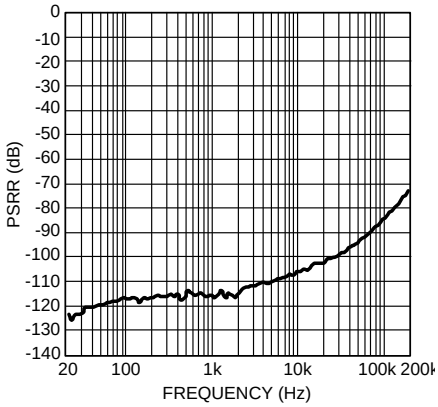

Figure 73. PSRR+ vs Frequency V_{CC} = 17V, V_{EE} = –17V R_L = 600Ω, F = 200kHz, V_{RIPPLE} = 200mvpp

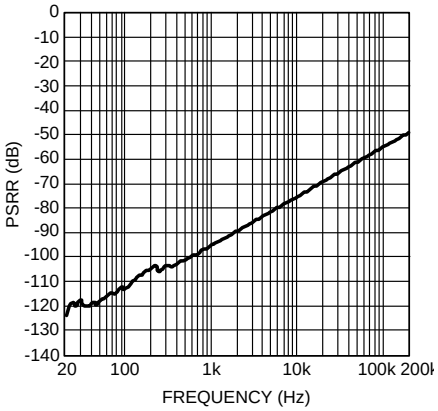

Figure 74. PSRR– vs Frequency V_{CC} = 17V, V_{EE} = –17V R_L = 600Ω, F = 200kHz, V_{RIPPLE} = 200mvpp

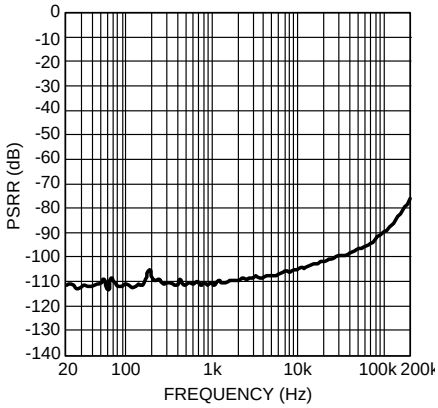

Figure 75. PSRR+ vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V R_L = 10kΩ, F = 200kHz, V_{RIPPLE} = 200mvpp

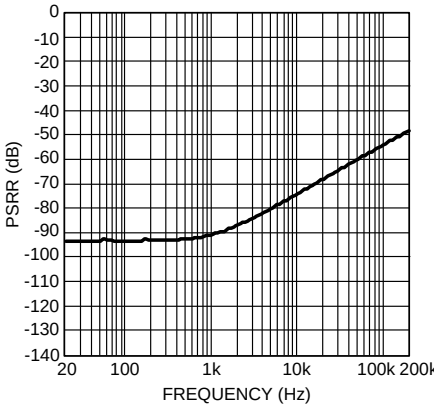

Figure 76. PSRR– vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V R_L = 10kΩ, F = 200kHz, V_{RIPPLE} = 200mvpp

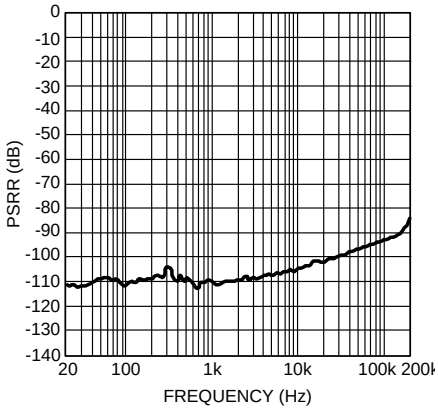

Figure 77. PSRR+ vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V R_L = 2kΩ, F = 200kHz, V_{RIPPLE} = 200mvpp

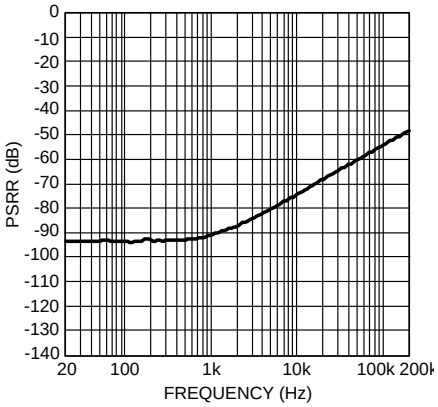

Figure 78. PSRR– vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V R_L = 2kΩ, F = 200kHz, V_{RIPPLE} = 200mvpp

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Typical Characteristics (continued)

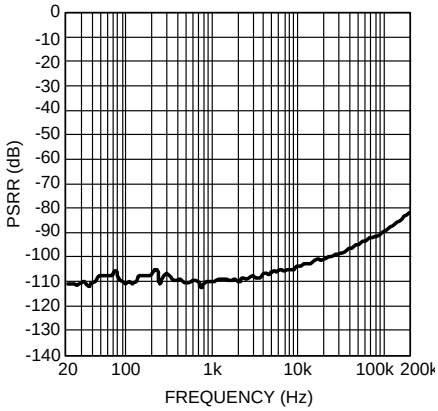

Figure 79. PSRR+ vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V R_L = 600Ω, F = 200kHz, V_{RIPPLE} = 200mvpp

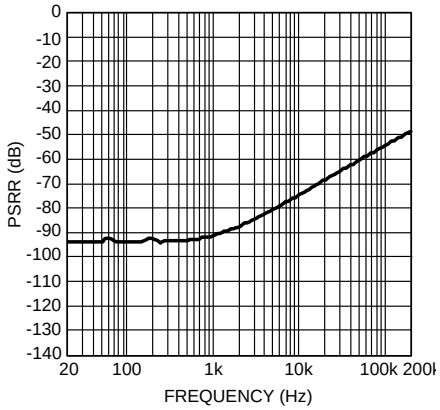

Figure 80. PSRR– vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V R_L = 600Ω, F = 200kHz, V_{RIPPLE} = 200mvpp

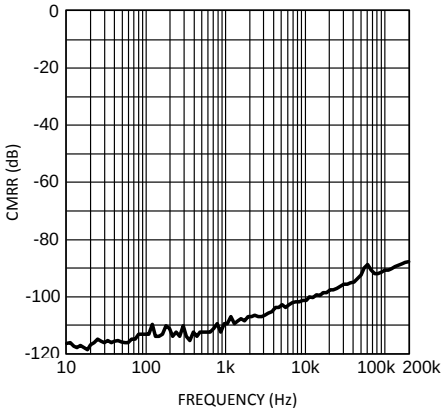

Figure 81. Cmrr vs Frequency V_{CC} = 15V, V_{EE} = –15V R_L = 2kΩ

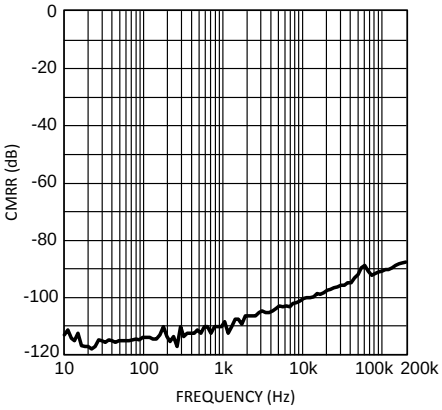

Figure 82. Cmrr vs Frequency V_{CC} = 12V, V_{EE} = –12V R_L = 2kΩ

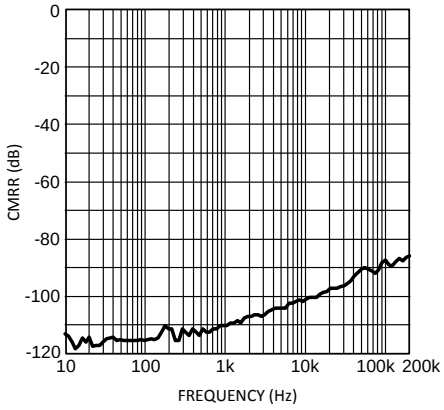

Figure 83. Cmrr vs Frequency V_{CC} = 17V, V_{EE} = –17V R_L = 2kΩ

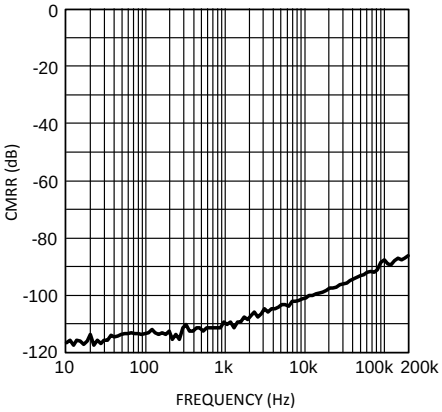

Figure 84. Cmrr vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V R_L = 2kΩ

Typical Characteristics (continued)

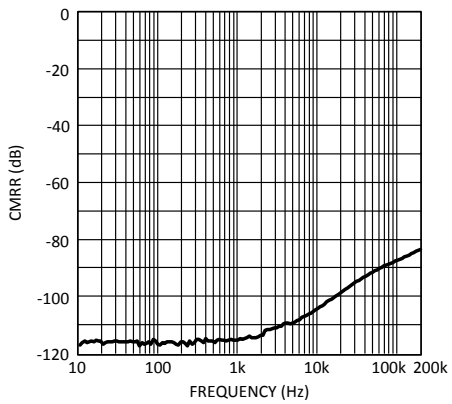

Figure 85. Cmrr vs Frequency V_{CC} = 15V, V_{EE} = –15V R_L = 600Ω

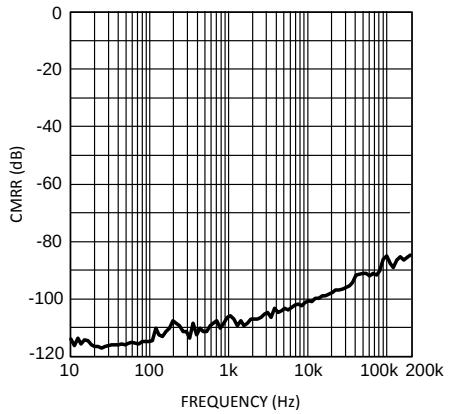

Figure 86. Cmrr vs Frequency V_{CC} = 12V, V_{EE} = –12V R_L = 600Ω

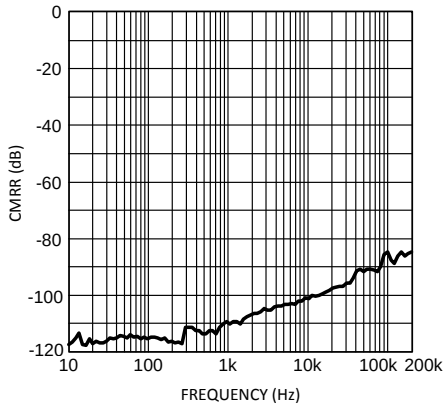

Figure 87. Cmrr vs Frequency V_{CC} = 17V, V_{EE} = –17V R_L = 600Ω

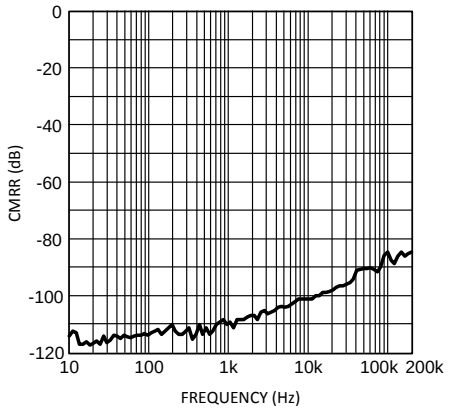

Figure 88. Cmrr vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V R_L = 600Ω

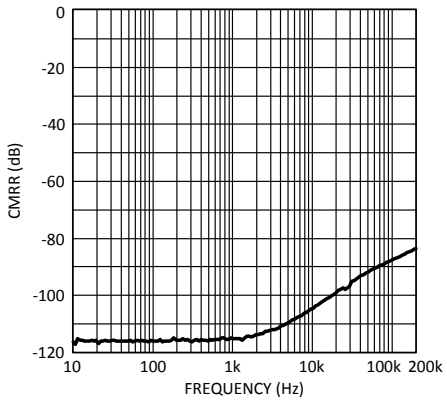

Figure 89. Cmrr vs Frequency V_{CC} = 15V, V_{EE} = –15V R_L = 10kΩ

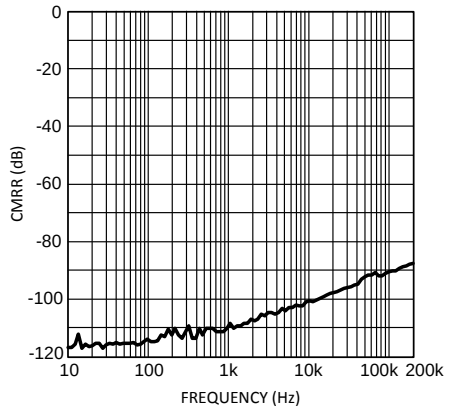

Figure 90. Cmrr vs Frequency V_{CC} = 12V, V_{EE} = –12V R_L = 10kΩ

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Typical Characteristics (continued)

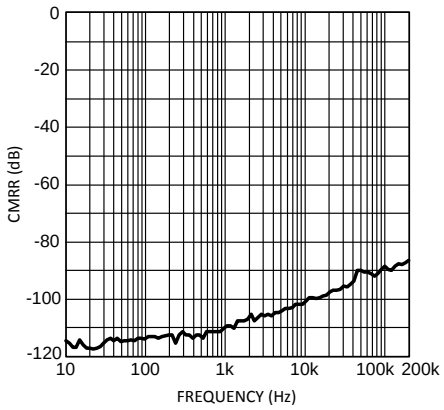

Figure 91. Cmrr vs Frequency V_{CC} = 17V, V_{EE} = –17V R_L = 10kΩ

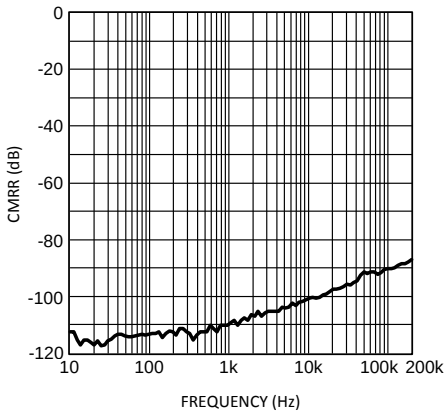

Figure 92. Cmrr vs Frequency V_{CC} = 2.5V, V_{EE} = –2.5V R_L = 10kΩ

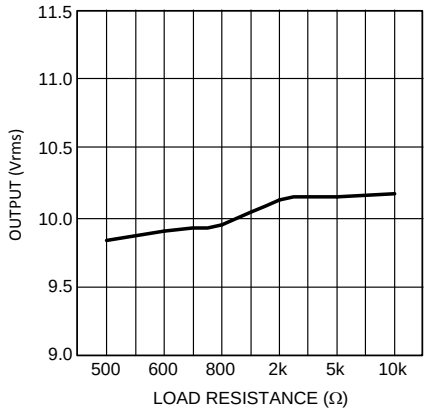

Figure 93. Output Voltage vs Load Resistance V_{DD} = 15V, V_{EE} = –15v Thd+N = 1%

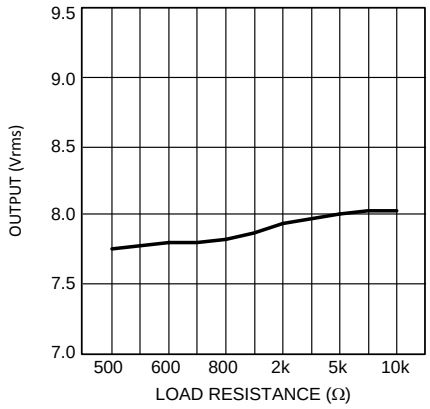

Figure 94. Output Voltage vs Load Resistance V_{DD} = 12V, V_{EE} = –12v Thd+N = 1%

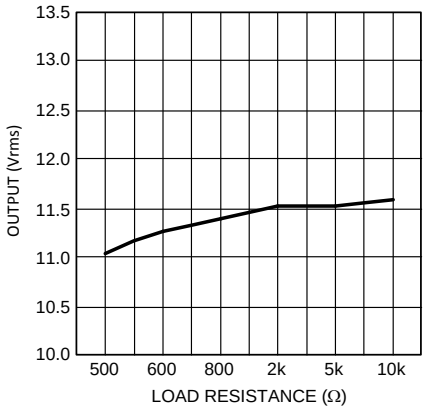

Figure 95. Output Voltage vs Load Resistance V_{DD} = 17V, V_{EE} = –17v Thd+N = 1%

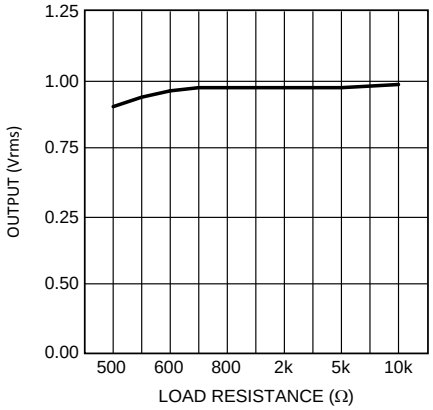

Figure 96. Output Voltage vs Load Resistance V_{DD} = 2.5V, V_{EE} = –2.5v Thd+N = 1%

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Typical Characteristics (continued)

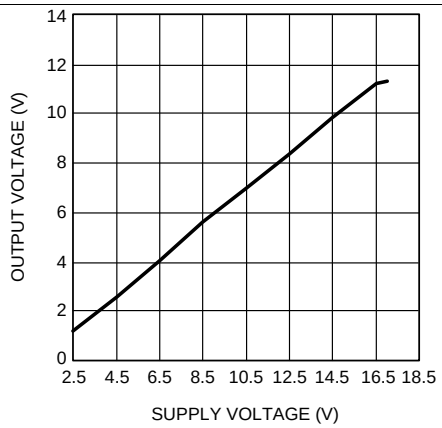

Figure 97. Output Voltage vs Supply Voltage R_L = 2kΩ, Thd+N = 1%

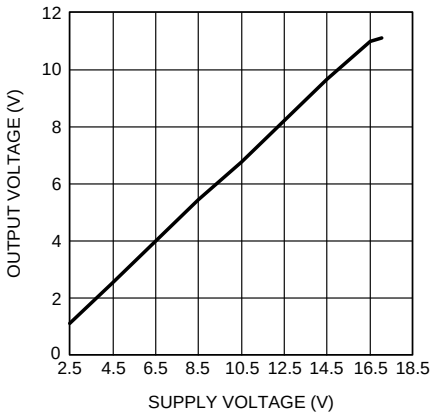

Figure 98. Output Voltage vs Supply Voltage R_L = 600Ω, Thd+N = 1%

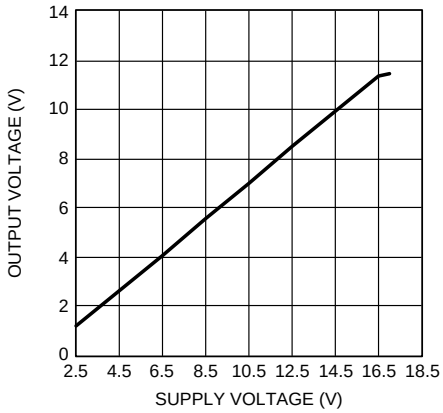

Figure 99. Output Voltage vs Supply Voltage R_L = 10kΩ, Thd+N = 1%

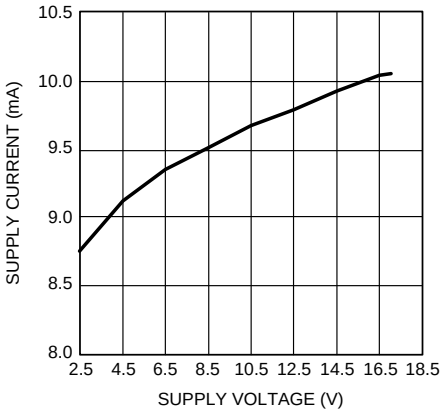

Figure 100. Supply Current vs Supply Voltage R_L = 2kΩ

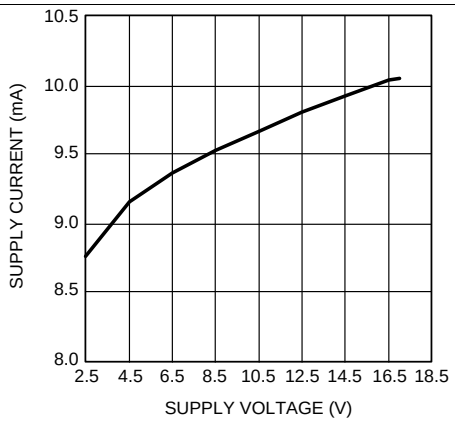

Figure 101. Supply Current vs Supply Voltage R_L = 600Ω

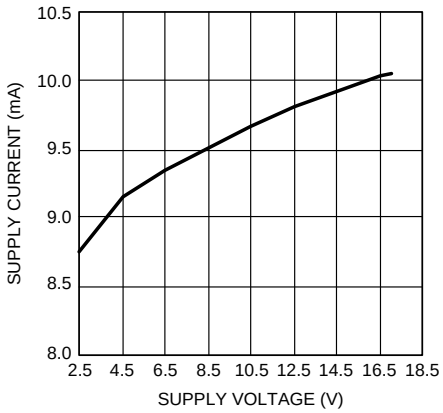

Figure 102. Supply Current vs Supply Voltage R_L = 10kΩ

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Typical Characteristics (continued)

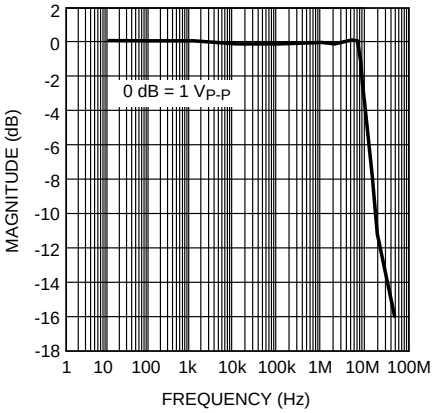

Figure 103. Full Power Bandwidth vs Frequency

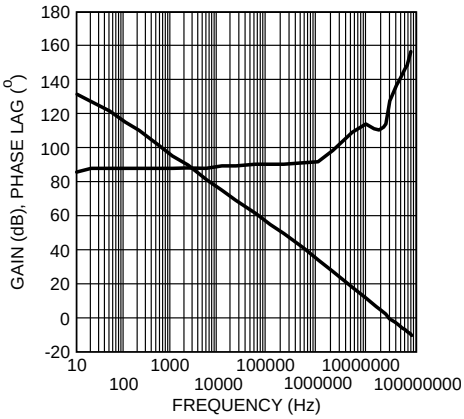

Figure 104. Gain Phase vs Frequency

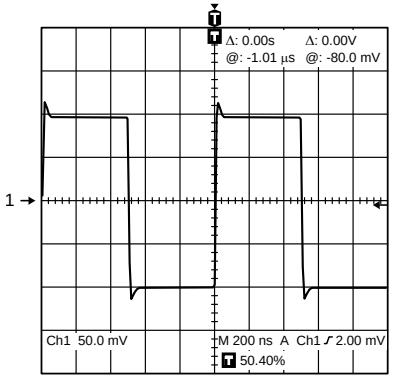

Figure 105. Small-Signal Transient Response A_V = 1, C_L = 10pf

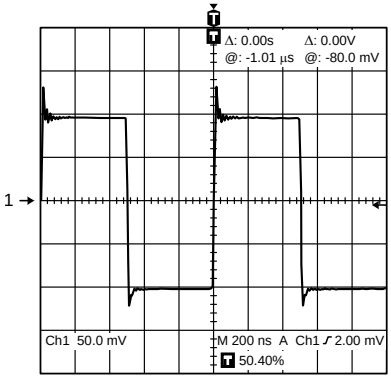

Figure 106. Small-Signal Transient Response A_V = 1, C_L = 100pf

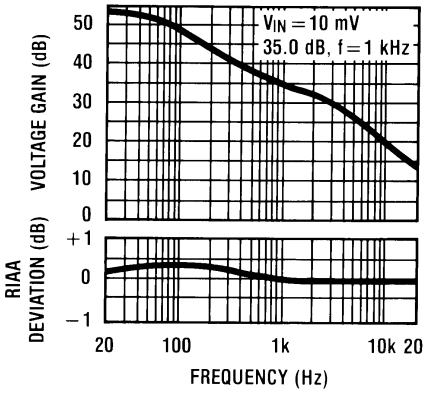

Figure 107. RIAA Preamp Voltage Gain, RIAA Deviation vs Frequency

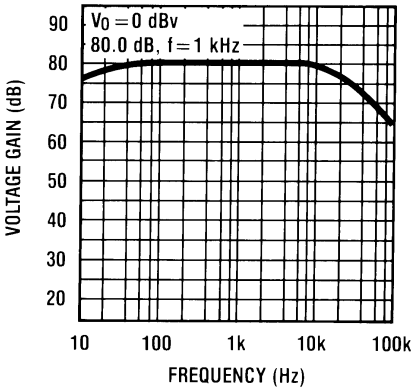

Figure 108. Flat Amp Voltage Gain vs Frequency

8 Parameter Measurement Information

All parameters are measured according to the conditions described in the *Specifications* section.

8.1 Distortion Measurements

The vanishingly low residual distortion produced by LME49720 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution, however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49720's low residual distortion is an input referred internal error. As shown in Figure 109, adding the 10Ω resistor connected between the amplifier's inverting and non-inverting inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is amplified by a factor of 101. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101, which means that measurement resolution increases by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 109.

This technique is verified by duplicating the measurements with high closed loop gain and/or making the measurements at high frequencies. Doing so produces distortion components that are within the measurement equipment's capabilities. This datasheet's THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.

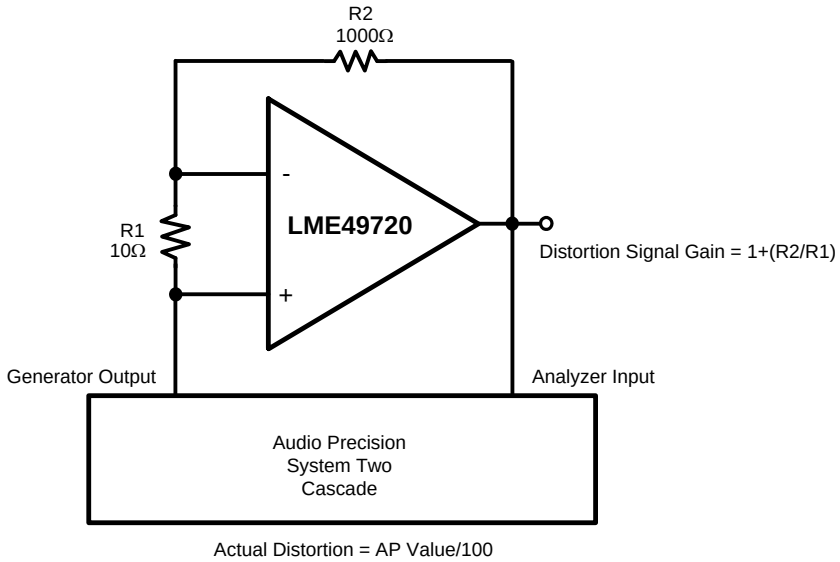

Figure 109. THD+N and IMD Distortion Test Circuit

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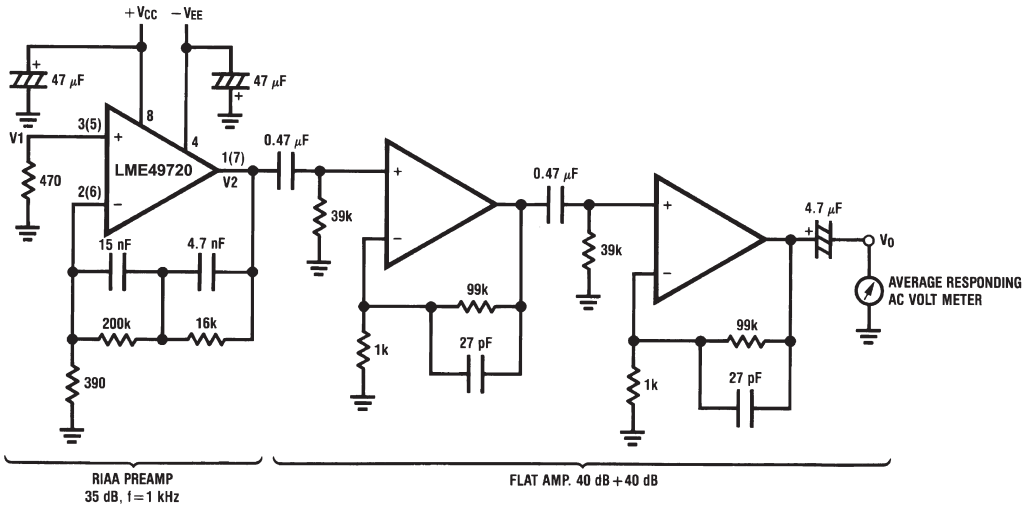
Distortion Measurements (continued)



Complete shielding is required to prevent induced pick up from external sources. Always check with oscilloscope for power line noise.
Total Gain: 115 dB @F = 1 kHz
Input Referred Noise Voltage: E_n = V0/560,000 (V)

Figure 110. Noise Measurement Circuit

9 Detailed Description

9.1 Overview

The LME49720 audio operational amplifier delivers superior audio signal amplification for outstanding audio performance.

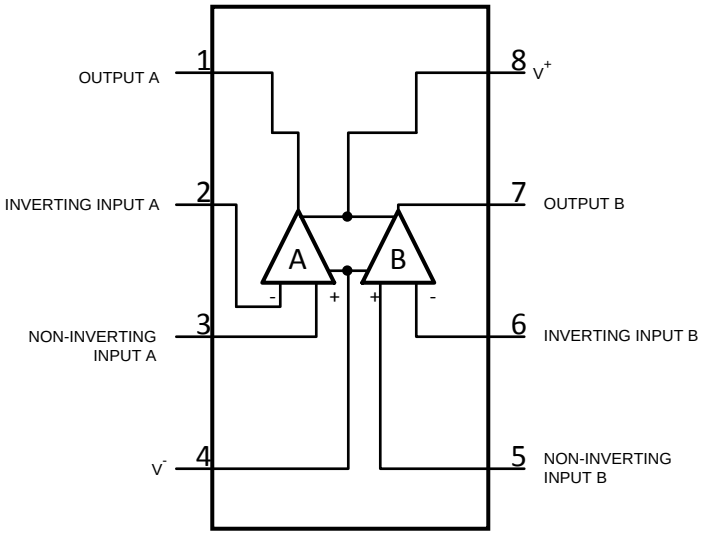
To ensure that the most challenging loads are driven without compromise, the LME49720 has a high slew rate of ±20V/μs and an output current capability of ±26mA. Further, dynamic range is maximized by an output stage that drives 2kΩ loads to within 1V of either power supply voltage and to within 1.4V when driving 600Ω loads.

The LME49720's outstanding CMRR (120dB), PSRR (120dB), and V_{OS} (0.1mV) give the amplifier excellent operational amplifier DC performance.

The LME49720 has a wide supply range of ±2.5V to ±17V. Over this supply range the LME49720's input circuitry maintains excellent common-mode and power supply rejection, as well as maintaining its low input bias current. The LME49720 is unity gain stable. This Audio Operational Amplifier achieves outstanding AC performance while driving complex loads with values as high as 100pF.

The LME49720 is available in 8–lead narrow body SOIC, 8–lead PDIP, and 8–lead TO-99. Demonstration boards are available for each package.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Capacitive Load

The LME49720 is a high speed op amp with excellent phase margin and stability. Capacitive loads up to 100pF will cause little change in the phase characteristics of the amplifiers and are therefore allowable.

Capacitive loads greater than 100pF must be isolated from the output. The most straightforward way to do this is to put a resistor in series with the output. This resistor will also prevent excess power dissipation if the output is accidentally shorted.

9.3.2 Balance Cable Driver

With high peak-to-peak differential output voltage and plenty of low distortion drive current, the LME49720 makes an excellent balanced cable driver. Combining the single-to-differential configuration with a balanced cable driver results in a high performance single-ended input to balanced line driver solution.

Although the LME49720 can drive capacitive loads up to 100pF, cable loads exceeding 100pF can cause instability. For such applications, series resistors are needed on the outputs before the capacitive load.

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9.4 Device Functional Modes

This device does not have operation mode.

10 Application and Implementation

NOTE

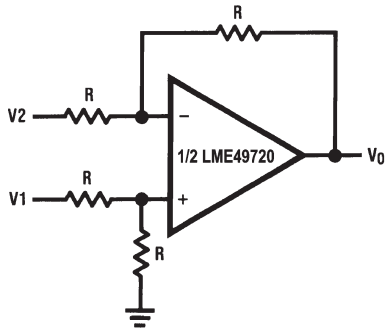
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

These typical connection diagrams highlight the required external components and system level connections for proper operation of the device. Any design variation can be supported by TI through schematic and layout reviews. Visit e2e.ti.com for design assistance and join the audio amplifier discussion forum for additional information

10.2 Typical Applications

10.2.1 Single Ended Converter



$V_O = V1–V2$

Figure 111. Balanced To Single Ended Converter

10.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Power Supply	±15
Speaker	2 KΩ

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Surface Mount Capacitors

Temperature and applied DC voltage influence the actual capacitance of high-K materials. Table 2 shows the relationship between the different types of high-K materials and their associated tolerances, temperature coefficients, and temperature ranges. Notice that a capacitor made with X5R material can lose up to 15% of its capacitance within its working temperature range.

Select high-K ceramic capacitors according to the following rules:

1. Use capacitors made of materials with temperature coefficients of X5R, X7R, or better.
2. Use capacitors with DC voltage ratings of at least twice the application voltage.
3. Choose a capacitance value at least twice the nominal value calculated for the application.

Multiply the nominal value by a factor of 2 for safety. If a 10-µF capacitor is required, use 20µF.

The preceding rules and recommendations apply to capacitors used in connection with this device. The LME49720 cannot meet its performance specifications if the rules and recommendations are not followed.

Table 2. Typical Tolerance and Temperature Coefficient of Capacitance by Material

Material	COG/NPO	X7R	X5R
Typical Tolerance	±5%	±10%	80/–20%
Temperature	±30ppm	±15%	22/–82%
Temperature Range, ºC	–55/125ºC	–55/125ºC	–30/85 ºC

10.2.1.3 Application Curves

For application curves, see the figures listed in Table 3.

Table 3. Table of Graphs

DESCRIPTION	FIGURE NUMBER
THD+N vs Output Power	See Figure 1
THD+N vs Frequency	See Figure 13
Crosstalk vs Frequency	See Figure 36
PSRR vs Frequency	See Figure 58

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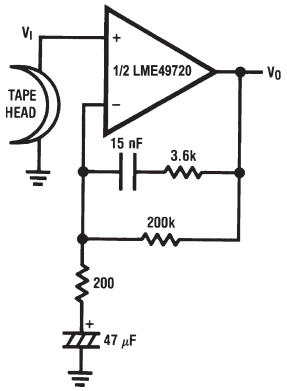
10.2.2 Other Applications



A_V = 34.5
F = 1 kHz
E_n = 0.38 µV
A Weighted

Figure 112. Nab Preamp

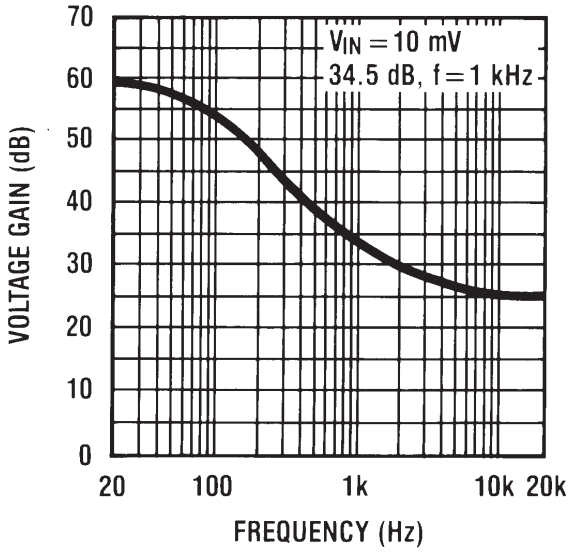
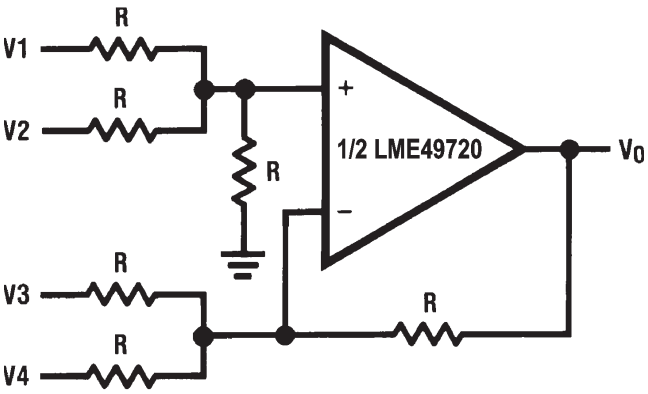
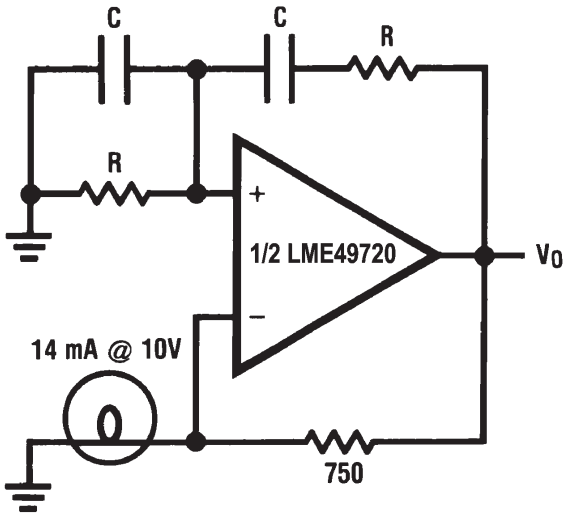


Figure 113. Nab Preamp Voltage Gain vs Frequency



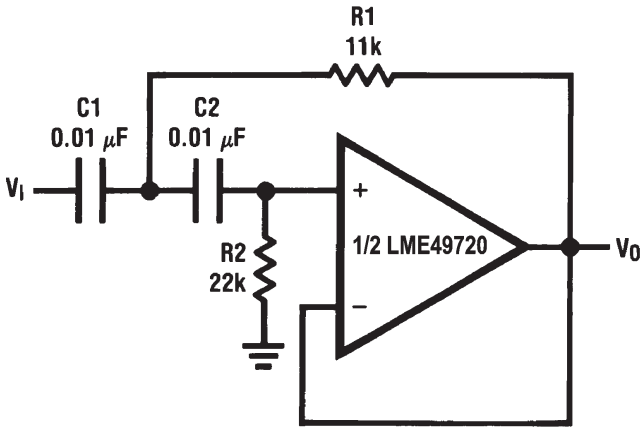
V_O = V1 + V2 − V3 − V4

Figure 114. Adder/Subtracter



$$f_o = \frac{1}{2\pi RC}$$

Figure 115. Sine Wave Oscillator



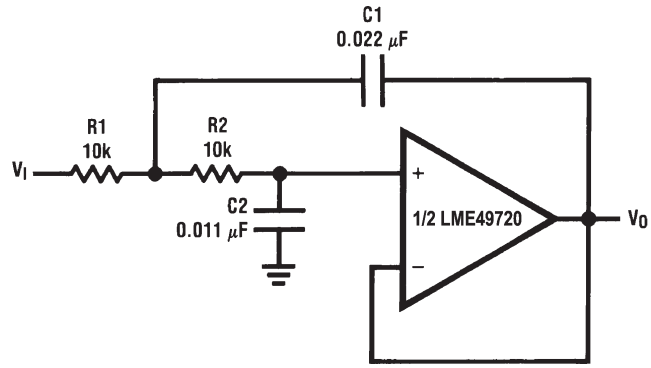
$$\text{if } C1 = C2 = C$$

$$R1 = \frac{\sqrt{2}}{2\omega_o C}$$

$$R2 = 2 \times R1$$

Illustration is f_0 = 1 kHz

Figure 116. Second Order High Pass Filter (Butterworth)



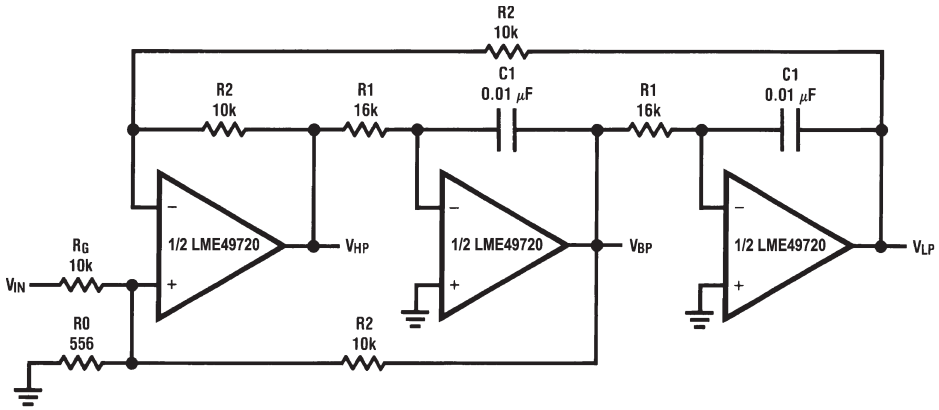
$$\text{if } R1 = R2 = R$$

$$C1 = \frac{\sqrt{2}}{\omega_o R}$$

$$C2 = \frac{C1}{2}$$

Illustration is f_0 = 1 kHz

Figure 117. Second Order Low Pass Filter (Butterworth)



$$f_0 = \frac{1}{2\pi C1R1}, Q = \frac{1}{2}\left(1 + \frac{R2}{R0} + \frac{R2}{RG}\right), A_{BP} = QA_{LP} = QA_{LH} = \frac{R2}{RG}$$

Illustration is f_0 = 1 kHz, Q = 10, A_{BP} = 1

Figure 118. State Variable Filter

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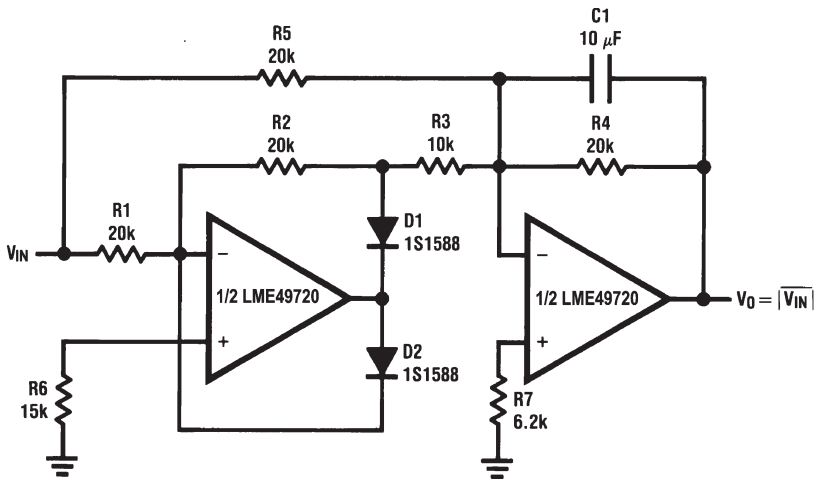


Figure 119. AC/DC Converter

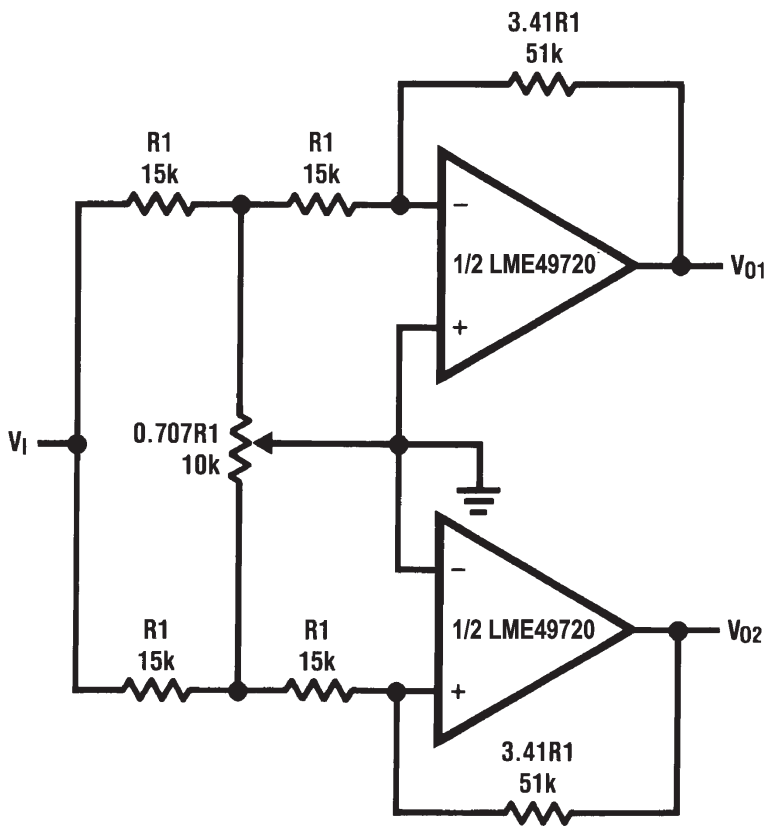


Figure 120. 2 Channel Panning Circuit (Pan Pot)

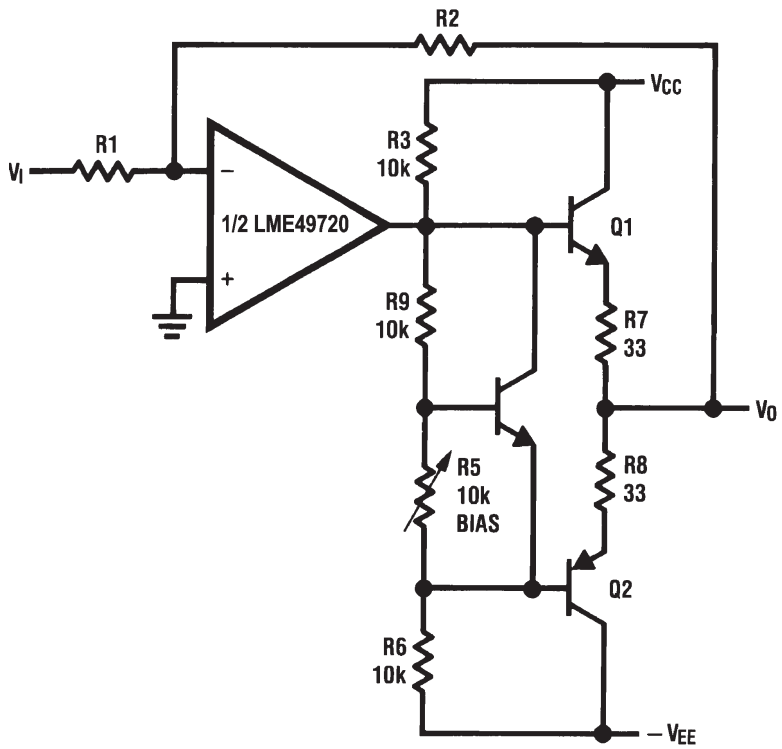
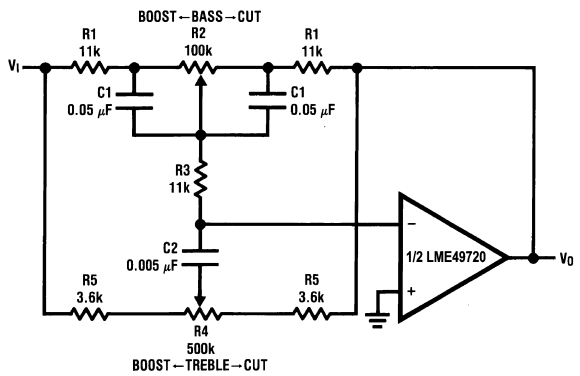


Figure 121. Line Driver



$$f_L = \frac{1}{2\pi R2C1}, f_{LB} = \frac{1}{2\pi R1C1}$$

$$f_H = \frac{1}{2\pi R5C2}, f_{HB} = \frac{1}{2\pi(R1 + R5 + 2R3)C2}$$

Illustration is:

f_L = 32 Hz, f_{LB} = 320 Hz

f_H =11 kHz, f_{HB} = 1.1 kHz

Figure 122. Tone Control

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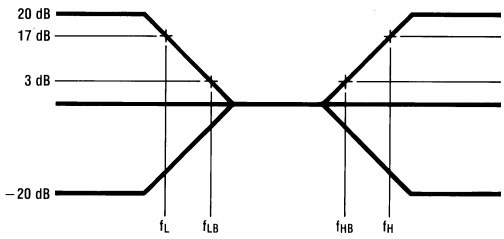
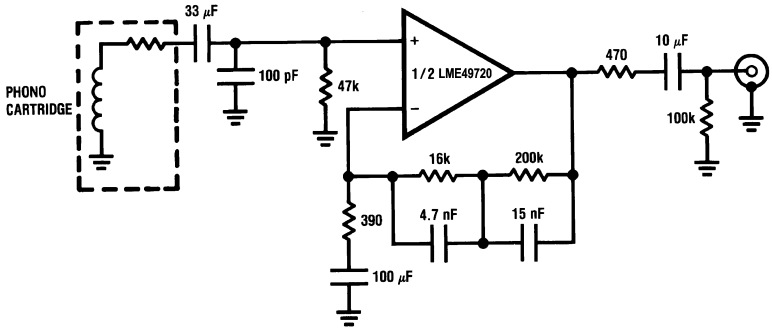
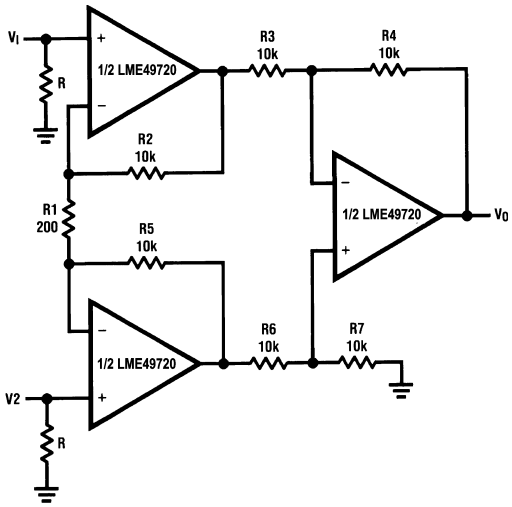


Figure 123. RIAA Preamp Behavior



A_v = 35 dB
E_n = 0.33 µV
S/N = 90 dB
f = 1 kHz
A Weighted
A Weighted, V_{IN} = 10 mV
@f = 1 kHz

Figure 124. RIAA Preamp



If R2 = R5, R3 = R6, R4 = R7

$$V0 = \left(1 + \frac{2R2}{R1}\right)\frac{R4}{R3}(V2 - V1)$$

Illustration is:

V0 = 101(V2 − V1)

Figure 125. Balanced Input Mic Amp

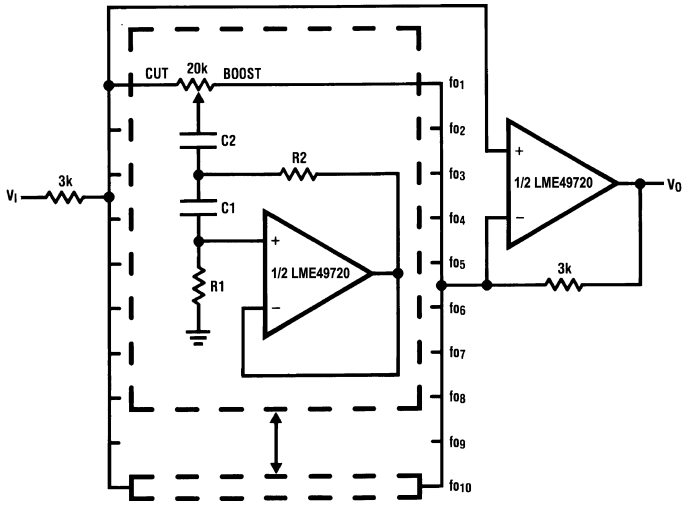


Figure 126. 10 Band Graphic Equalizer

Table 4. Typical Values for Band Graphic Equalizer

fo (Hz)	C_1	C_2	R_1	R_2
32	0.12µF	4.7µF	75kΩ	500Ω
64	0.056µF	3.3µF	68kΩ	510Ω
125	0.033µF	1.5µF	62kΩ	510Ω
250	0.015µF	0.82µF	68kΩ	470Ω
500	8200pF	0.39µF	62kΩ	470Ω
1k	3900pF	0.22µF	68kΩ	470Ω
2k	2000pF	0.1µF	68kΩ	470Ω
4k	1100pF	0.056µF	62kΩ	470Ω
8k	510pF	0.022µF	68kΩ	510Ω
16k	330pF	0.012µF	51kΩ	510Ω

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11 Power Supply Recommendations

The LME49720 is designed to operate a power supply from ±2.5V to ±17V. Therefore, the output voltage range of the power supply must be within this range. The current capability of upper power must not exceed the maximum current limit of the power switch.

11.1 Power Supply Decoupling Capacitors

The LME49720 requires adequate power supply decoupling to ensure a low total harmonic distortion (THD). Place a low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, within 2 mm of the V+ and V- pins. This choice of capacitor and placement helps with higher frequency transients, spikes, or digital hash on the line. In addition to the 0.1 µF ceramic capacitor, it is recommended to place a 2.2 µF to 10 µF capacitor on the V+ and V- pins. This larger capacitor acts as a charge reservoir, providing energy faster than the board supply, thus helping to prevent any droop in the supply voltage.

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12 Layout

12.1 Layout Guidelines

12.1.1 Component Placement

Place all the external components close to the device. Placing the decoupling capacitors as close as possible to the device is important for low total harmonic distortion (THD). Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

12.2 Layout Example

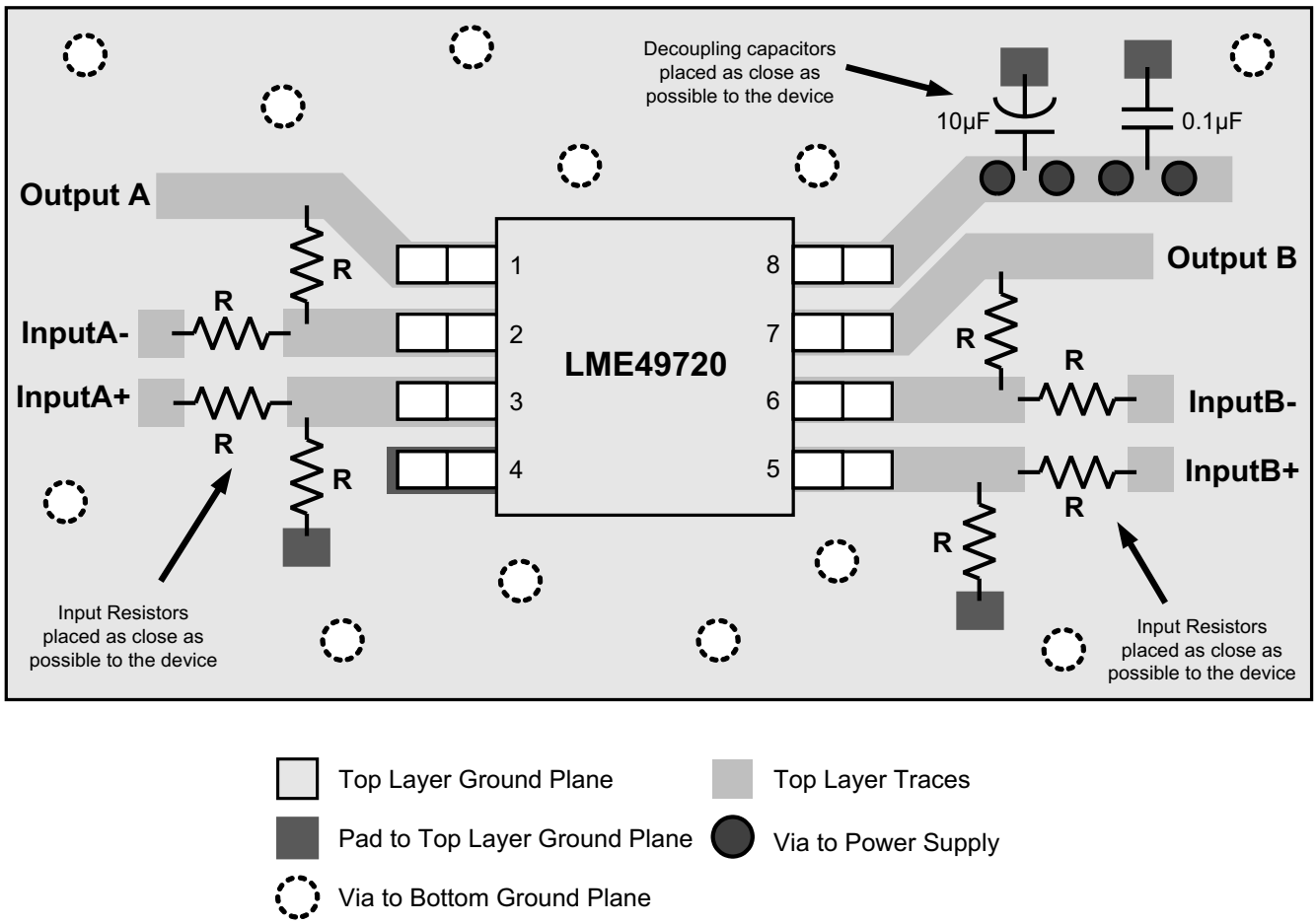

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Figure 127. LME49720SOIC Layout Example

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Layout Example (continued)

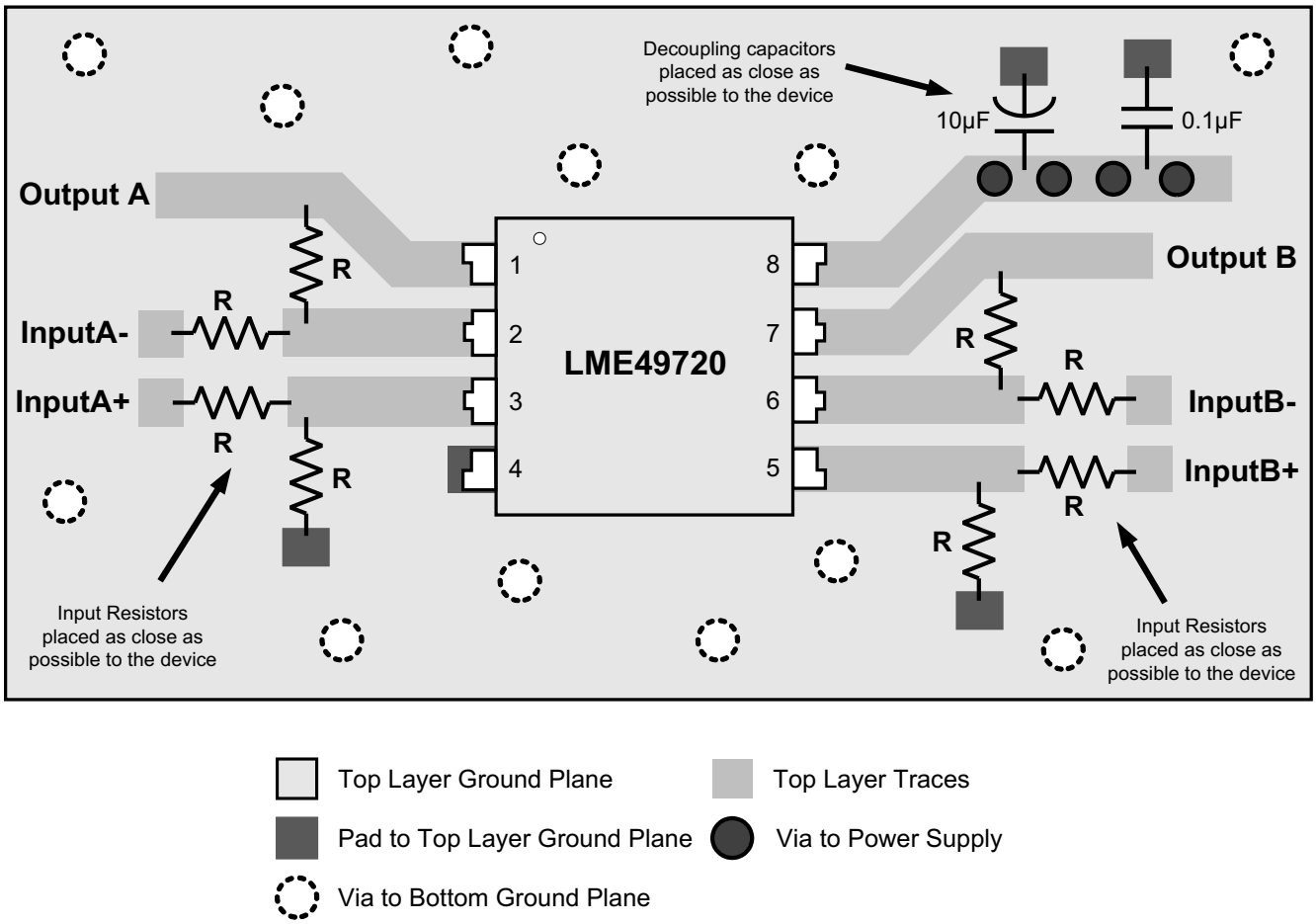

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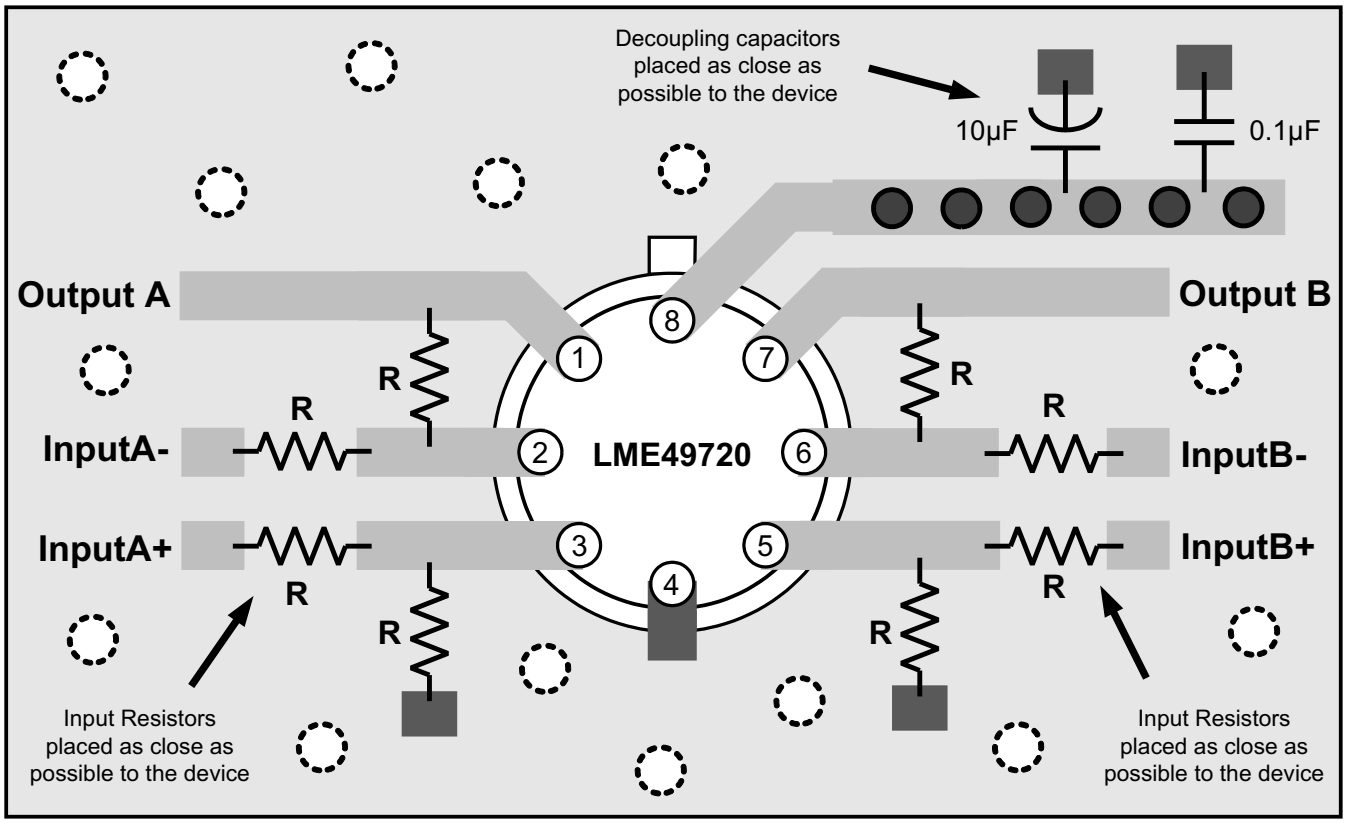
Figure 128. LME49720PDIP Layout Example

Layout Example (continued)



Top Layer Ground Plane
Top Layer Traces
Pad to Top Layer Ground Plane
Via to Power Supply
Via to Bottom Ground Plane

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Figure 129. LME49720TO-99 Layout Example

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13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LME49720MAX/NOPB	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	L49720 MA
LME49720MAX/NOPB.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	L49720 MA
LME49720MAX/NOPB.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	L49720 MA
LME49720NA/NOPB	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LME 49720NA
LME49720NA/NOPB.A	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LME 49720NA
LME49720NA/NOPB.B	Active	Production	PDIP (P) | 8	40 | TUBE	Yes	NIPDAU	Level-1-NA-UNLIM	-40 to 85	LME 49720NA

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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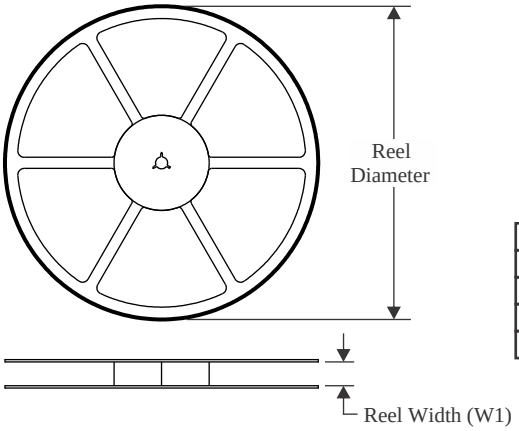
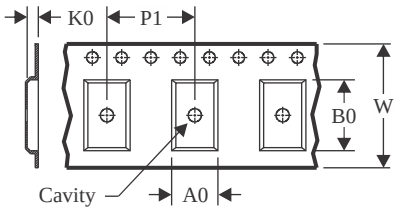
TAPE AND REEL INFORMATION

REEL DIMENSIONS

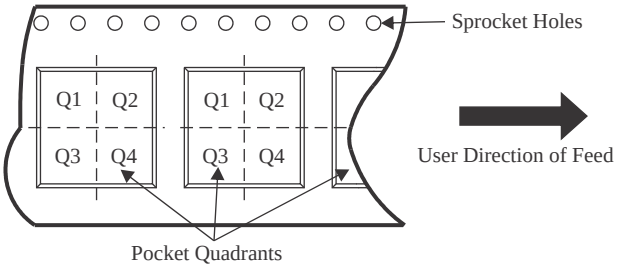


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

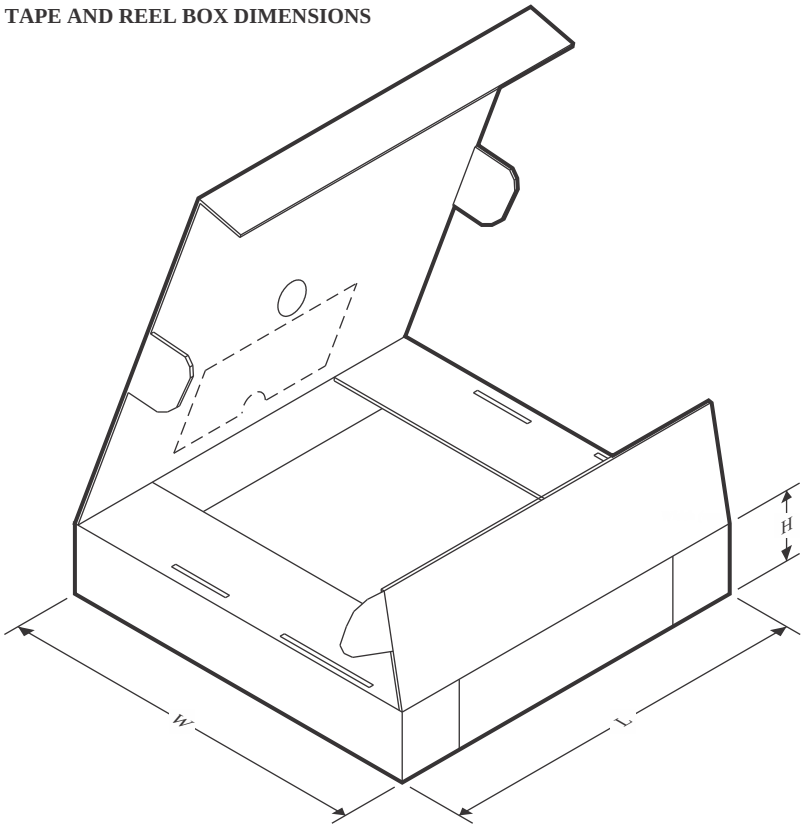
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LME49720MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

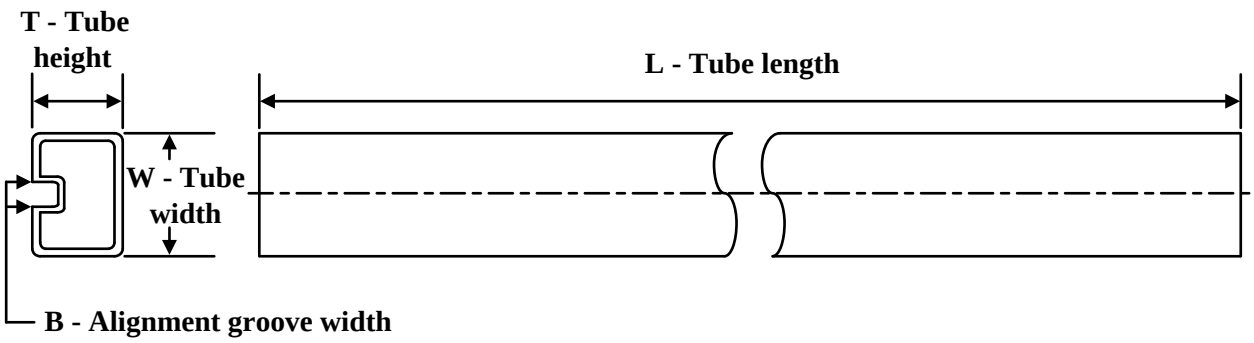
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

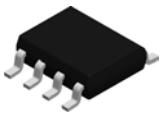
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LME49720MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LME49720NA/NOPB	P	PDIP	8	40	502	14	11938	4.32
LME49720NA/NOPB.A	P	PDIP	8	40	502	14	11938	4.32
LME49720NA/NOPB.B	P	PDIP	8	40	502	14	11938	4.32

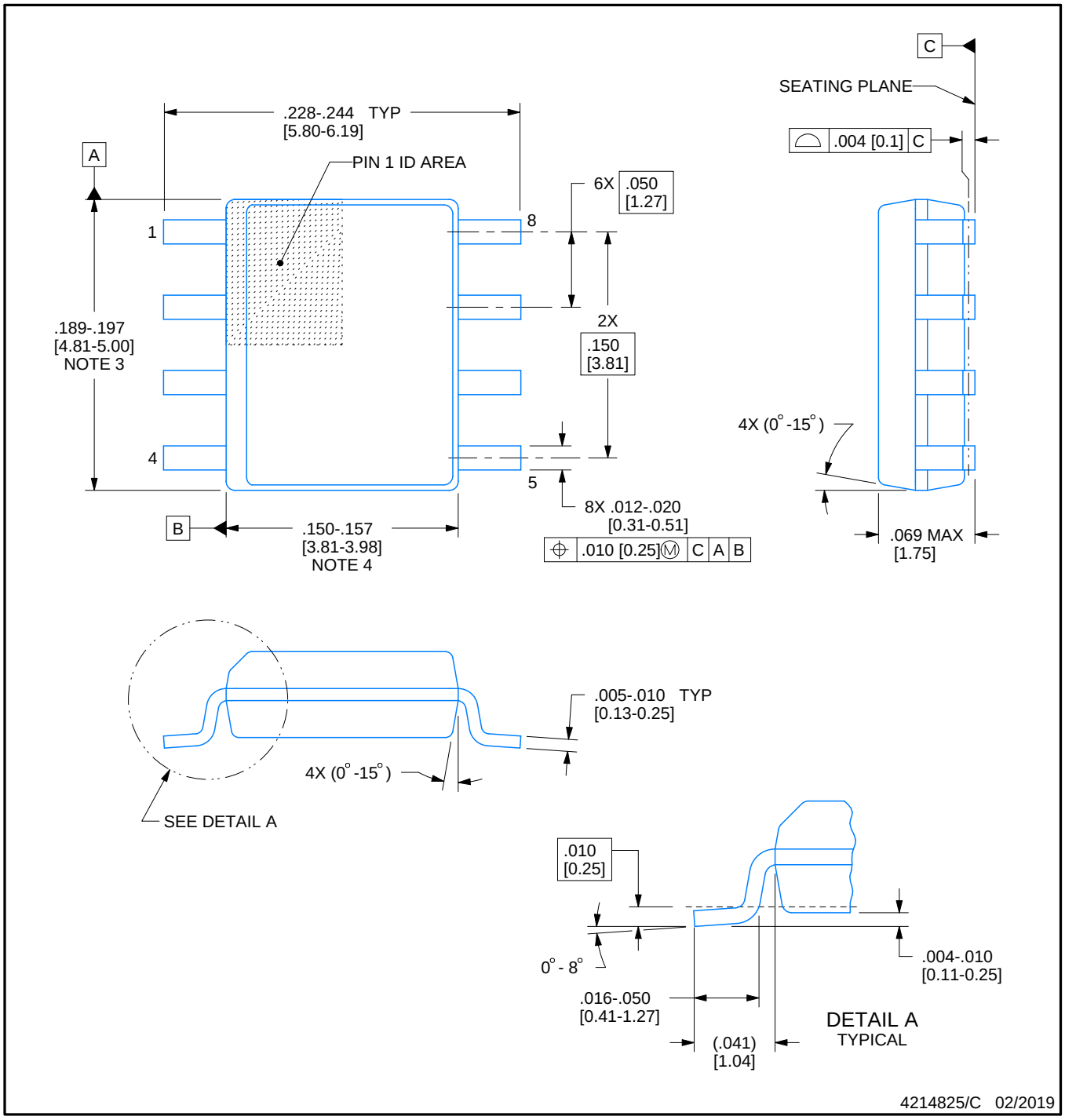


PACKAGE OUTLINE

D0008A

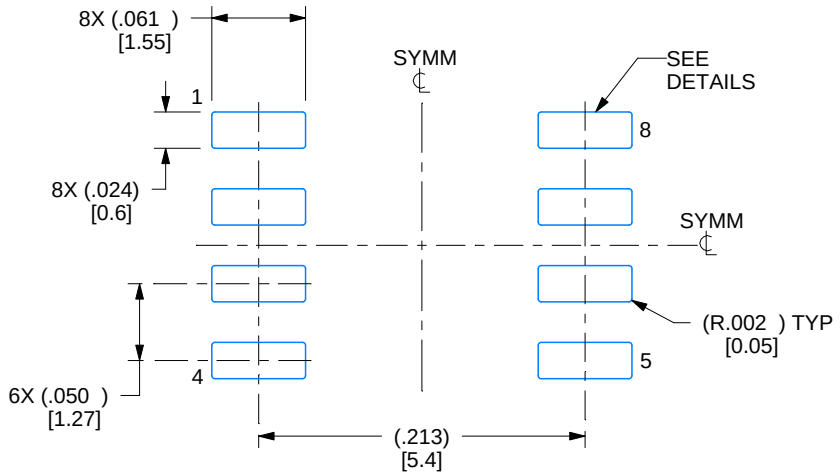
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

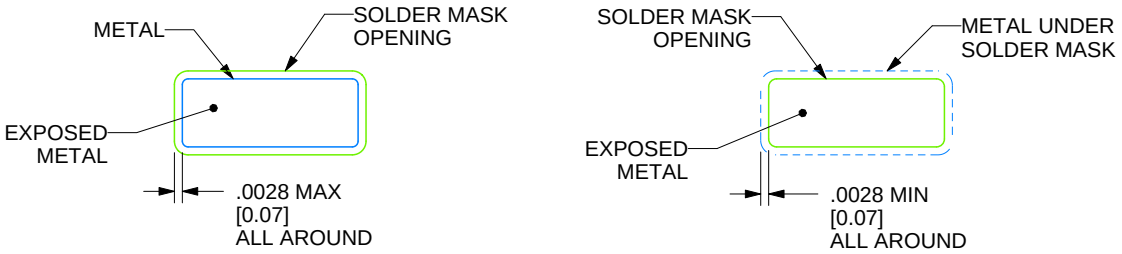


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

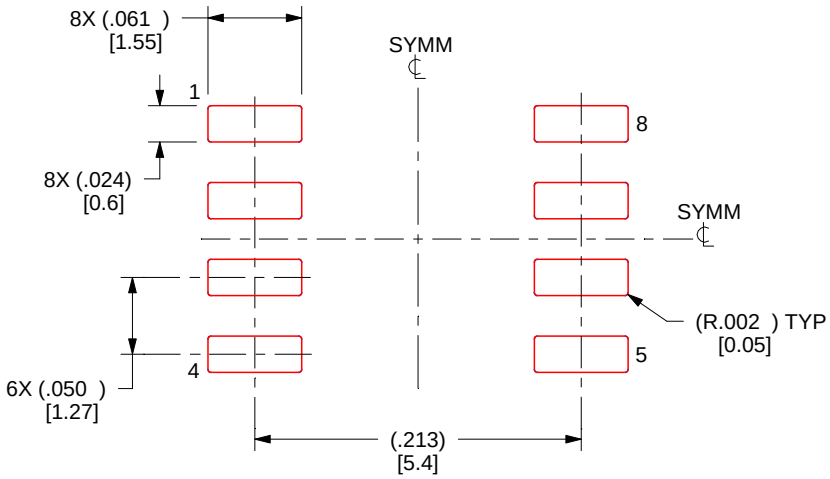


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



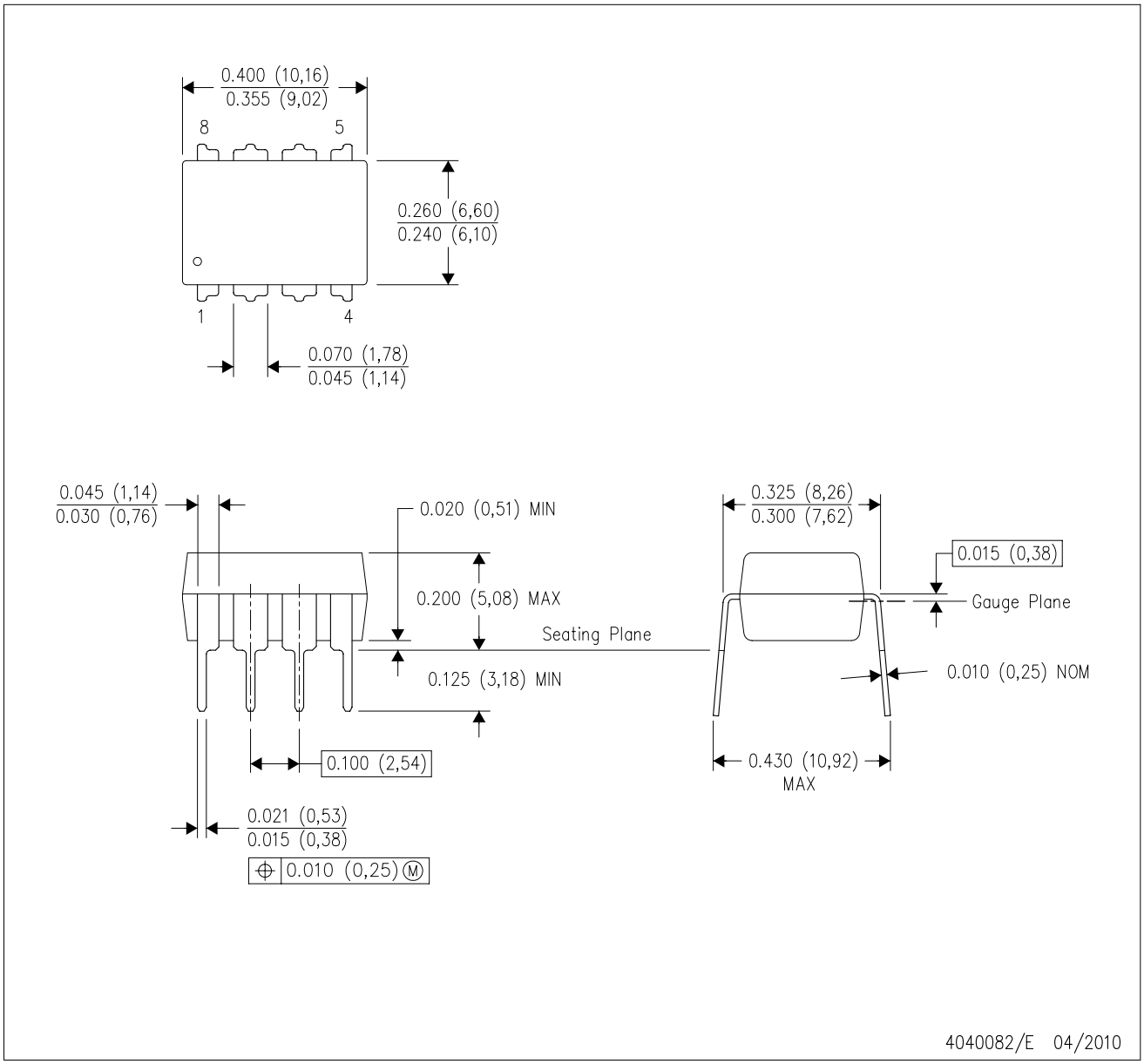
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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Last updated 10/2025