AM26C31 Quadruple Differential Line Driver

1 Features

- Meets or exceeds the requirements of TIA/EIA-422-B and ITU recommendation V.11
- Low power, I_{CC} = 100μA typical
- Operates from a single 5V supply
- High speed, $t_{PLH} = t_{PHL}$ = 7ns typical
- Low pulse distortion, $t_{sk(p)}$ = 0.5ns typical
- High output impedance in power-off conditions
- Improved replacement for AM26LS31 device
- Available in Q-temp automotive
  - High-reliability automotive applications
  - Configuration control and print support
  - Qualification to automotive standards
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

2 Applications

- Chemical and gas sensors
- Field transmitters: temperature sensors and pressure sensors
- Military: radars and sonars
- Motor control: brushless DC and brushed DC
- Military and avionics imaging
- Temperature sensors and controllers using modbus

3 Description

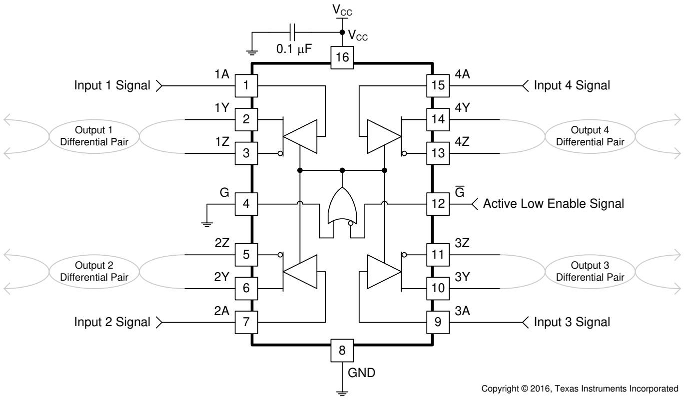
The AM26C31 device is a differential line driver with complementary outputs, designed to meet the requirements of TIA/EIA-422-B and ITU (formerly CCITT). The 3-state outputs have high-current capability for driving balanced lines, such as twisted-pair or parallel-wire transmission lines, and they provide the high-impedance state in the power-off condition. The enable functions are common to all four drivers and offer the choice of an active-high (G) or active-low ($\overline{G}$) enable input. BiCMOS circuitry reduces power consumption without sacrificing speed.

The AM26C31C device is characterized for operation from 0°C to 70°C, the AM26C31I device is characterized for operation from –40°C to +85°C, the AM26C31Q device is characterized for operation over the automotive temperature range of –40°C to +125°C, and the AM26C31M device is characterized for operation over the full military temperature range of –55°C to +125°C.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
AM26C31	CDIP (J, 16)	19.56mm × 6.92mm
	PDIP (N, 16)	19.3mm × 6.35mm
	SO (NS, 16)	10.3mm × 5.3mm
	CFP (W, 16)	10.3mm × 6.73mm
	SOIC (D, 16)	9.9mm × 3.91mm
	SSOP (DB, 16)	6.2mm × 5.3mm
	TSSOP (PW, 16)	5.mm × 4.4mm
	LCCC (FK, 20)	8.89mm × 8.89mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Common Application Diagram

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4 Pin Configuration and Functions

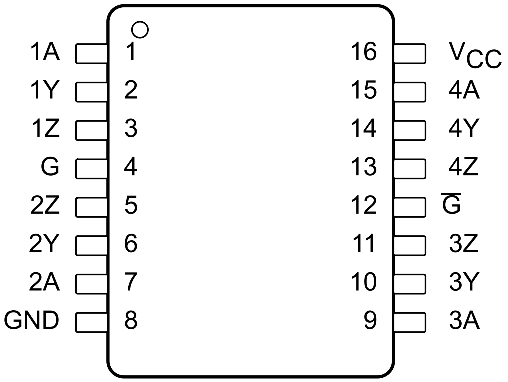

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Figure 4-1. J (CDIP), W (CFP), D (SOIC), DB (SSOP), NS (SO), N (PDIP), or PW (TSSOP) Package 16-Pin (Top View)

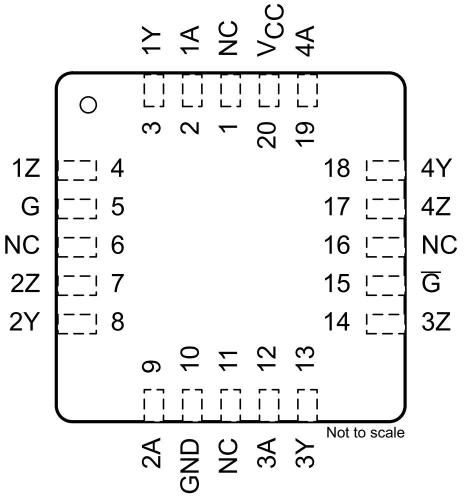

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Figure 4-2. FK (LCCC) Package, 20-Pin (Top View)

Table 4-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	CDIP, CFP, SOIC, SSOP, SO, PDIP, TSSOP	LCCC		
1A	1	2	I	Driver 1 input
1Y	2	3	O	Driver 1 output
1Z	3	4	O	Driver 1 inverted output
2A	7	9	I	Driver 2 input
2Y	6	8	O	Driver 2 output
2Z	5	7	O	Driver 2 inverted output
3A	9	12	I	Driver 3 input
3Y	10	13	O	Driver 3 output
3Z	11	14	O	Driver 3 inverted output
4A	15	19	I	Driver 3 input
4Y	14	18	O	Driver 3 output
4Z	13	17	O	Driver 3 inverted output
G	4	5	I	Active high enable
$\overline{G}$	12	15	I	Active low enable
GND	8	10	—	Ground pin
NC(1)	—	1, 6, 11, 16	—	No internal connection
V_{CC}	16	20	—	Power pin

(1) NC – No connection

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	–0.5	7	V
V_I	Input voltage	–0.5	V_{CC} + 0.5	V
V_{ID}	Differential input voltage	–14	14	V
V_O	Output voltage	–0.5	7	V
I_{IK} I_{OK}	Input or output clamp current		±20	mA
I_O	Output current		±150	mA
	V_{CC} current		200	mA
	GND current	–200		mA
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{ID}	Differential input voltage			±7		V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–20	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature	AM26C31C	0		70	°C
		AM26C31I	–40		85	
		AM26C31Q	–40		125	
		AM26C31M	–55		125	

5.4 Thermal Information

THERMAL METRIC(1)		AM26C31								UNIT
		D (SOIC)	DB (SSOP)	PW (TSSOP)	NS (SO)	N (PDIP)	J (CDIP)	W (CFP)	FK (LCCC)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2) (3)	84.6	102.6	107.5	88.5	60.6	—	—	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	48.7	38.4	46.2	48.1	39.3(4)	58.9(4)	37.1(4)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	54.3	53.7	50.7	40.6	56.4(4)	109.3(4)	36.2(4)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.4	11.8	3.2	13.5	27.5	—	—	—	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	42.8	53.5	53.1	50.3	40.3	—	—	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	12(4)	5.7(4)	4.3(4)	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} - T_A) / R_{\theta JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.
(4) Modelling assumption: MIL-STD-883 for $R_{\theta JC(top)}$ and $R_{\theta JC(bot)}$ JESD51 for $R_{\theta JB}$.

5.5 Electrical Characteristics: AM26C31C and AM26C31I

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	$I_O = -20mA$		2.4	3.4		V
V_{OL}	Low-level output voltage	$I_O = 20mA$			0.2	0.4	V
V_{OD}	Differential output voltage magnitude	$R_L = 100\Omega$, see Figure 6-1		2	3.1		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage(2)	$R_L = 100\Omega$, see Figure 6-1				±0.4	V
V_{OC}	Common-mode output voltage	$R_L = 100\Omega$, see Figure 6-1				3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage(2)	$R_L = 100\Omega$, see Figure 6-1				±0.4	V
I_I	Input current	$V_I = V_{CC}$ or GND				±1	μA
$I_{O(off)}$	Driver output current with power off	$V_{CC} = 0$	$V_O = 6V$			100	μA
			$V_O = -0.25V$			–100	
I_{OS}	Driver output short-circuit current	$V_O = 0$		–30		–150	mA
I_{OZ}	High-impedance off-state output current	$V_O = 2.5V$				20	μA
		$V_O = 0.5V$				–20	
I_{CC}	Quiescent supply current	$I_O = 0$	$V_I = 0$ or 5V			100	μA
			$V_I = 2.4V$ or 0.5V(3)		1.5	3	mA
C_i	Input capacitance				6		pF

(1) All typical values are at $V_{CC} = 5V$ and $T_A = 25°C$.
(2) $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(3) This parameter is measured per input. All other inputs are at 0V or 5V.

5.6 Electrical Characteristics: AM26C31Q and AM26C31M

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{OH}	High-level output voltage	I_O = –20mA		2.2	3.4		V
V_{OL}	Low-level output voltage	I_O = 20mA			0.2	0.4	V
V_{OD}	Differential output voltage magnitude	R_L = 100Ω, see Figure 6-1		2	3.1		V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage[2]	R_L = 100Ω, see Figure 6-1				±0.4	V
V_{OC}	Common-mode output voltage	R_L = 100Ω, see Figure 6-1				3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage[2]	R_L = 100Ω, see Figure 6-1				±0.4	V
I_I	Input current	V_I = V_{CC} or GND				±1	µA
$I_{O(off)}$	Driver output current with power off	V_{CC} = 0	V_O = 6V			100	µA
			V_O = –0.25V			–100	
I_{OS}	Driver output short-circuit current	V_O = 0				–170	mA
I_{OZ}	High-impedance off-state output current	V_O = 2.5V				20	µA
		V_O = 0.5V				–20	
I_{CC}	Quiescent supply current	I_O = 0	V_I = 0 or 5V			100	µA
			V_I = 2.4V or 0.5V[3]			3.2	mA
C_i	Input capacitance				6		pF

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(3) This parameter is measured per input. All other inputs are at 0V or 5V.

5.7 Switching Characteristics: AM26C31C and AM26C31I

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	S1 is open, see Figure 6-2	3	7	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output		3	7	12	
$t_{sk(p)}$	Pulse skew time ($\|t_{PLH} – t_{PHL}\|$)	S1 is open, see Figure 6-2		0.5	4	ns
$t_{r(OD)}$, $t_{f(OD)}$	Differential output rise and fall times	S1 is open, see Figure 6-3		5	10	ns
t_{PZH}	Output enable time to high level	S1 is closed, see Figure 6-4		10	19	ns
t_{PZL}	Output enable time to low level			10	19	
t_{PHZ}	Output disable time from high level	S1 is closed, see Figure 6-4		7	16	ns
t_{PLZ}	Output disable time from low level			7	16	
C_{pd}	Power dissipation capacitance (each driver)[2]	S1 is open, see Figure 6-2		170		pF

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) C_{pd} is used to estimate the switching losses according to $P_D = C_{pd} \times V_{CC}{}^2 \times f$, where f is the switching frequency.

5.8 Switching Characteristics: AM26C31Q and AM26C31M

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	S1 is open, see Figure 6-2		7	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output			6.5	12	
$t_{sk(p)}$	Pulse skew time ($\lvert t_{PLH} - t_{PHL} \rvert$)	S1 is open, see Figure 6-2		0.5	4	ns
$t_{r(OD)}$, $t_{f(OD)}$	Differential output rise and fall times	S1 is open, see Figure 6-3		5	12	ns
t_{PZH}	Output enable time to high level	S1 is closed, see Figure 6-4		10	19	ns
t_{PZL}	Output enable time to low level			10	19	
t_{PHZ}	Output disable time from high level	S1 is closed, see Figure 6-4		7	16	ns
t_{PLZ}	Output disable time from low level			7	16	
C_{pd}	Power dissipation capacitance (each driver)[2]	S1 is open, see Figure 6-2		100		pF

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) C_{pd} is used to estimate the switching losses according to $P_D = C_{pd} \times V_{CC}{}^2 \times f$, where f is the switching frequency.

5.9 Typical Characteristics

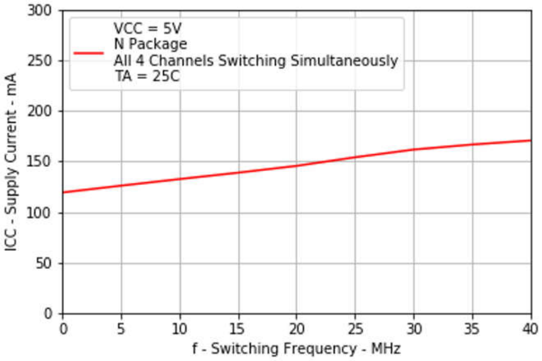


Figure 5-1. Supply Current vs Switching Frequency

6 Parameter Measurement Information

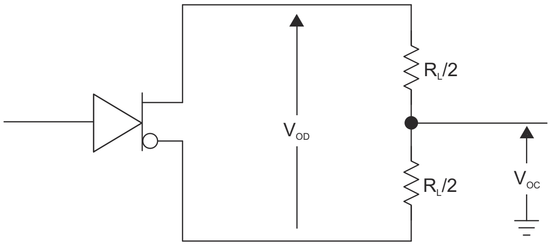
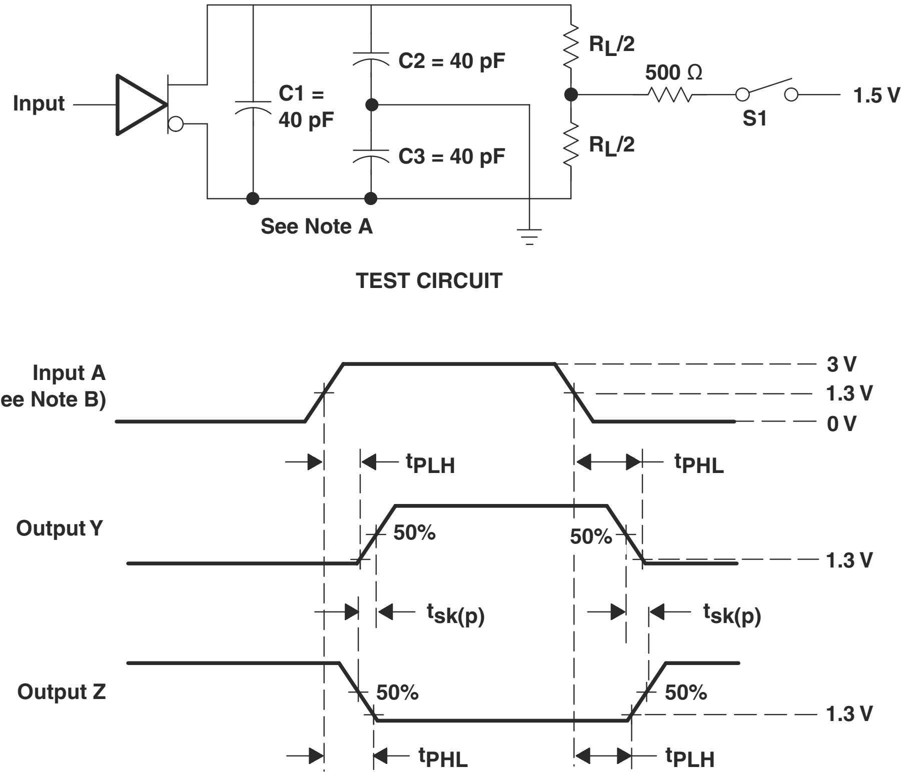


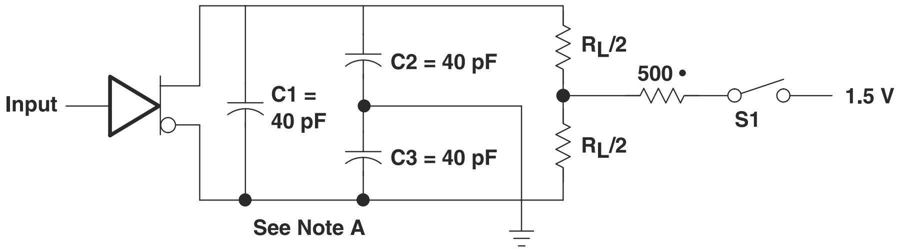
Figure 6-1. Differential and Common-Mode Output Voltages



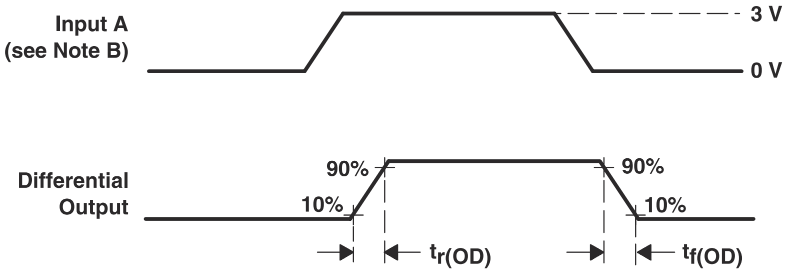
A. C1, C2, and C3 include probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, duty cycle ≤ 50%, and t_r, t_f ≤ 6ns.

Figure 6-2. Propagation Delay Time and Skew Waveforms and Test Circuit



TEST CIRCUIT

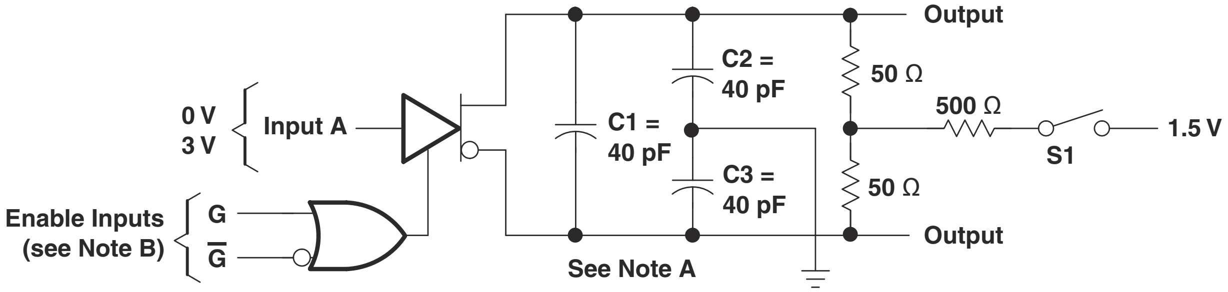


VOLTAGE WAVEFORMS

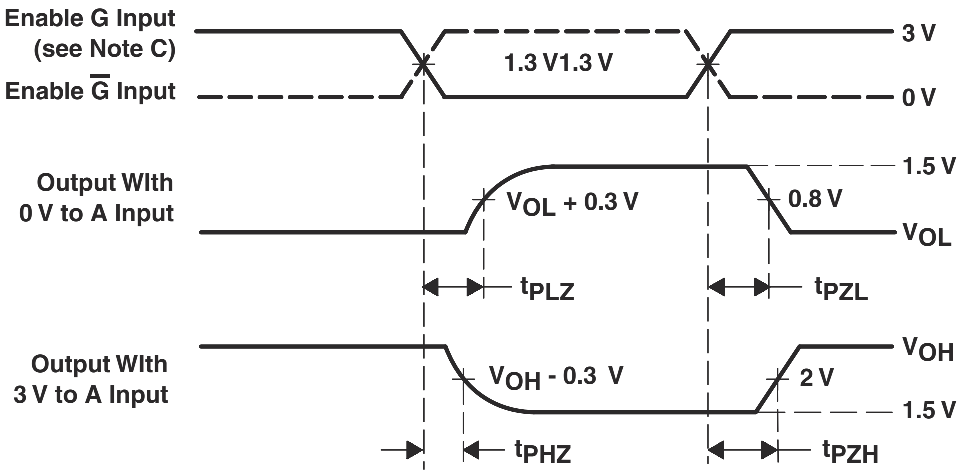
A. C1, C2, and C3 include probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, duty cycle ≤ 50%, and t_r, t_f ≤ 6ns.

Figure 6-3. Differential-Output Rise and Fall-Time Waveforms and Test Circuit



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C1, C2, and C3 include probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, duty cycle ≤ 50%, and t_r, t_f ≤ 6ns.

C. Each enable is tested separately.

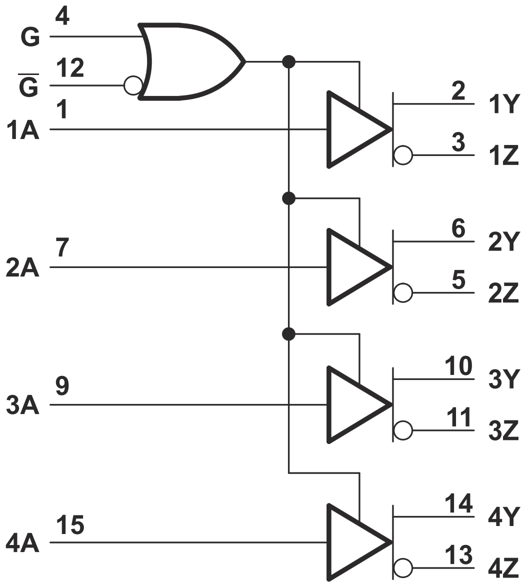
Figure 6-4. Output Enable and Disable Time Waveforms and Test Circuit

7 Detailed Description

7.1 Overview

The AM26C31 is a quadruple differential line driver with complementary outputs. The device is designed to meet the requirements of TIA/EIA-422-B and ITU (formerly CCITT), and it is generally used to communicate over relatively long wires in noisy environments.

7.2 Functional Block Diagrams



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

Figure 7-1. Logic Diagram (Positive Logic)

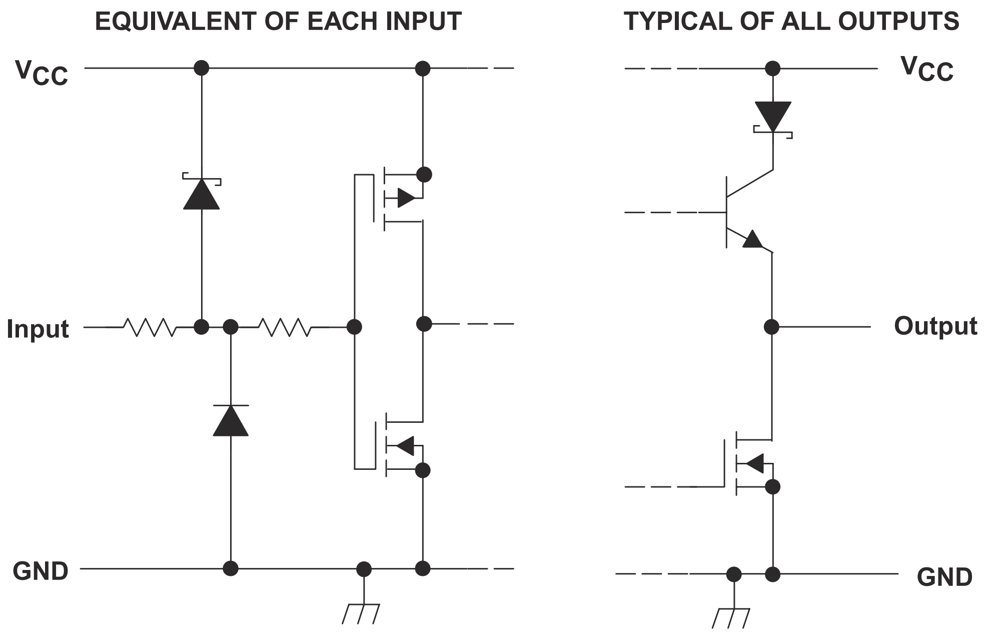


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Figure 7-2. Schematics of Inputs and Outputs

7.3 Feature Description

7.3.1 Active-High and Active-Low

The device can be configured using the G and $\overline{G}$ logic inputs to select transmitter output. A logic high on the G pin or a logic low on the $\overline{G}$ pin enables the device to operate. These pins are simply a way to configure the logic to match that of the receiving or transmitting controller or microprocessor.

7.3.2 Operates From a Single 5V Supply

Both the logic and transmitters operate from a single 5V rail, making designs much more simple. The line drivers and receivers can operate off the same rail as the host controller or a similar low voltage supply, thus simplifying power structure.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the AM26C31.

Table 7-1. Function Table (Each Driver)(1)

INPUT A	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = High level,
L = Low level,
X = Irrelevant,
Z = High impedance (off)

8 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

When designing a system that uses drivers, receivers, and transceivers that comply with RS-422, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. Because RS-422 allows only one driver on the bus, if termination is used, it is placed only at the end of the cable near the last receiver. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, AC termination, and multipoint termination. For laboratory experiments, 100 feet of 100Ω, 24-AWG, twisted-pair cable (Bertek) was used. A single driver and receiver, TI AM26C31C and AM26C32C, respectively, were tested at room temperature with a 5V supply voltage. To show voltage waveforms related to transmission-line reflections, the first plot shows output waveforms from the driver at the start of the cable (A/B); the second plot shows input waveforms to the receiver at the far end of the cable (Y).

8.2 Typical Application

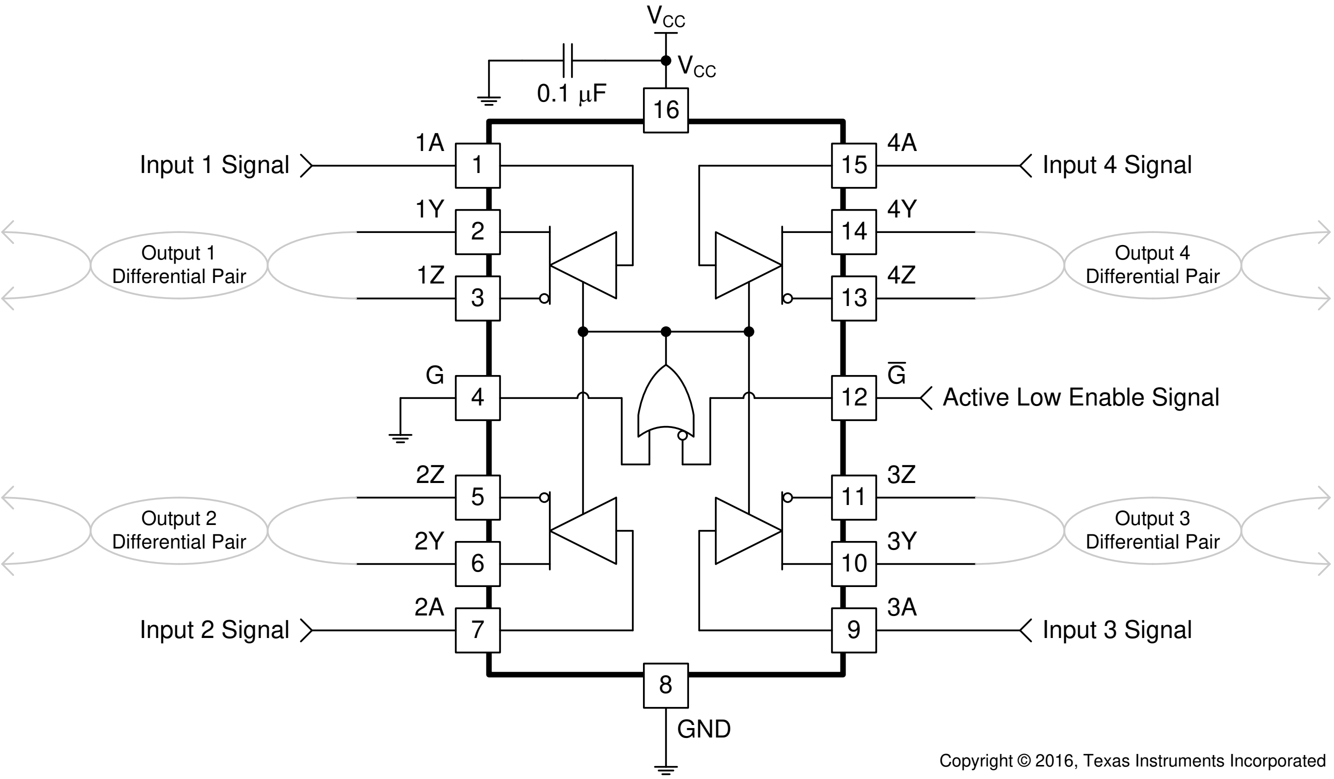

Figure 8-1. Differential Terminated Configuration With All Channels and Active Low Enable Used

8.2.1 Design Requirements

Resistor and capacitor (if used) termination values are shown for each laboratory experiment, but vary from system to system. For example, the termination resistor, R_T, must be within 20% of the characteristic impedance, Zo, of the cable and can vary from about 80Ω to 120Ω.

8.2.2 Detailed Design Procedure

Ensure values in *Absolute Maximum Ratings* are not exceeded.

Supply voltage, V_{IH}, and V_{IL} must comply with *Recommended Operating Conditions*.

8.2.3 Application Curve

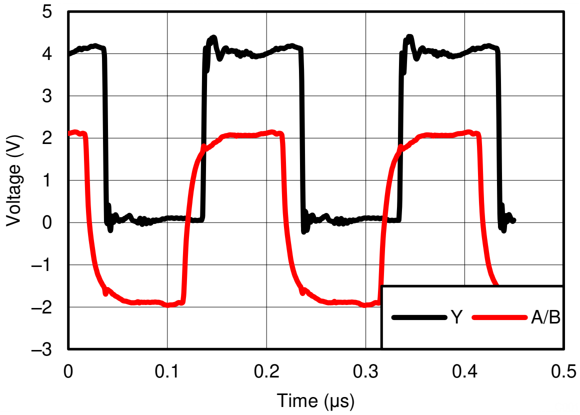

Figure 8-2. Differential 120Ω Terminated Output Waveforms (Cat 5E Cable)

8.3 Power Supply Recommendations

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

8.4.2 Layout Example

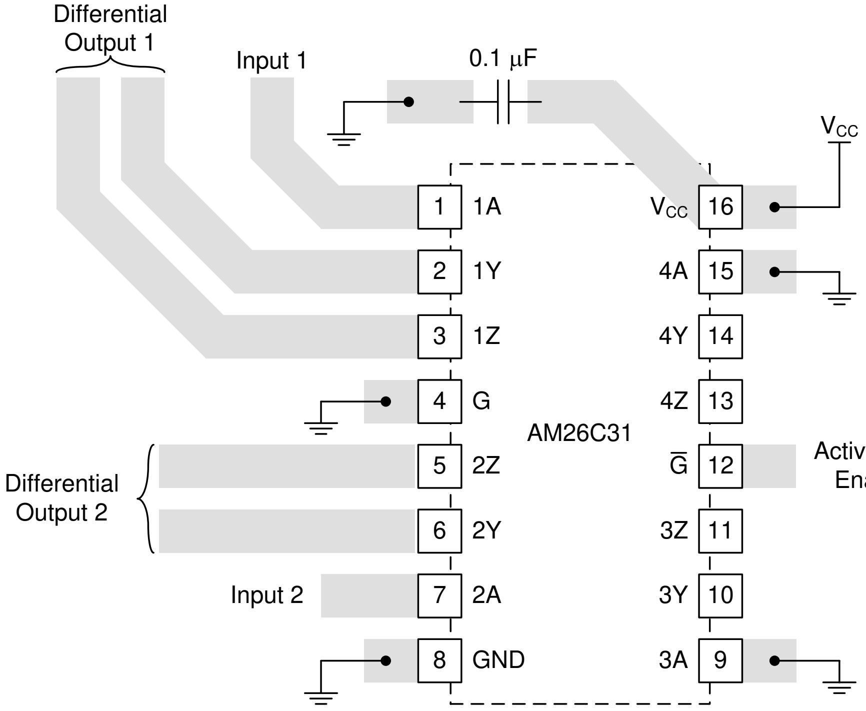

Figure 8-3. Trace Layout on PCB and Recommendations

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision O (June 2016) to Revision P (March 2024) — Page

- Changed the Device Information table to the *Package Information* table.......... 1
- Changed *Thermal Information* table.......... 5
- Changed Figure 5-1.......... 7
- Changed Figure 6-1.......... 8

Changes from Revision N (October 2011) to Revision O (Februrary 2014) — Page

- Updated the *Features* section and added the *Applications* section, the *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.......... 1
- Deleted *Ordering Information* table, see POA at the end of the data sheet.......... 1
- Changed *Thermal Information* table.......... 5

Changes from Revision M (June 2008) to Revision N (October 2011) — Page

- Changed units to mA from μA to fix units typo.......... 4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9163901M2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901M2A AM26C31M	Samples
5962-9163901MEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901MEA AM26C31M	Samples
5962-9163901MFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901MFA AM26C31M	Samples
5962-9163901Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901Q2A AM26C31 MFKB	Samples
5962-9163901QEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901QEA AM26C31MJB	Samples
5962-9163901QFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901QFA AM26C31MWB	Samples
AM26C31CD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	AM26C31C	
AM26C31CDBR	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI	0 to 70	26C31	
AM26C31CDR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	AM26C31C	
AM26C31CN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	AM26C31CN	Samples
AM26C31CNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	26C31	Samples
AM26C31ID	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	AM26C31I	
AM26C31IDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C31I	Samples
AM26C31IDBRE4	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C31I	Samples
AM26C31IDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AM26C31I	Samples
AM26C31IDRG4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	AM26C31I	
AM26C31IN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	AM26C31IN	Samples

PACKAGE OPTION ADDENDUM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AM26C31INE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	AM26C31IN	Samples
AM26C31INSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C31I	Samples
AM26C31IPW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	26C31I	
AM26C31IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	26C31I	Samples
AM26C31IPWRG4	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	26C31I	
AM26C31MFKB	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901Q2A AM26C31 MFKB	Samples
AM26C31MJB	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901QEA AM26C31MJB	Samples
AM26C31MWB	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9163901QFA AM26C31MWB	Samples
AM26C31QD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 125	AM26C31Q	
AM26C31QDG4	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 125	26C31Q	
AM26C31QDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AM26C31Q	Samples
AM26C31QDRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	26C31Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF AM26C31, AM26C31M :

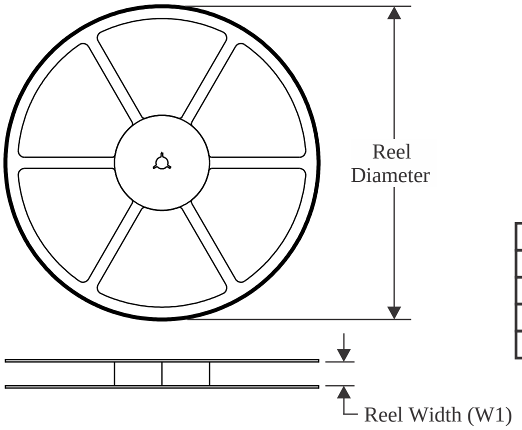
- Catalog : AM26C31
- Enhanced Product : AM26C31-EP, AM26C31-EP
- Military : AM26C31M

NOTE: Qualified Version Definitions:

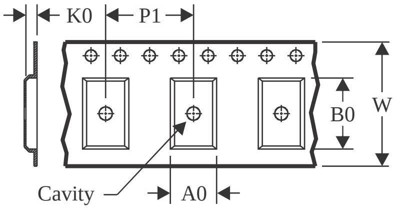
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

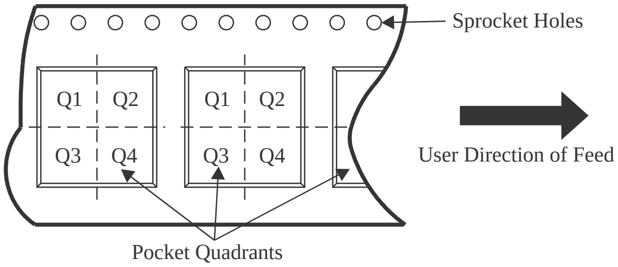


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

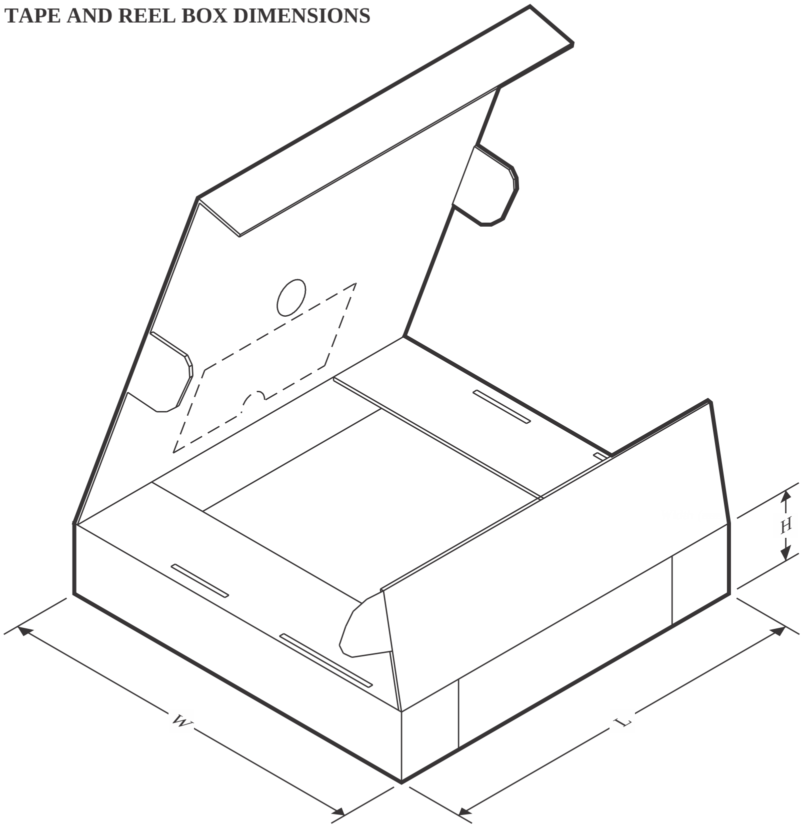
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AM26C31CDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
AM26C31CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26C31CNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26C31IDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
AM26C31IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26C31IDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26C31INSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
AM26C31IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26C31IPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
AM26C31QDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
AM26C31QDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

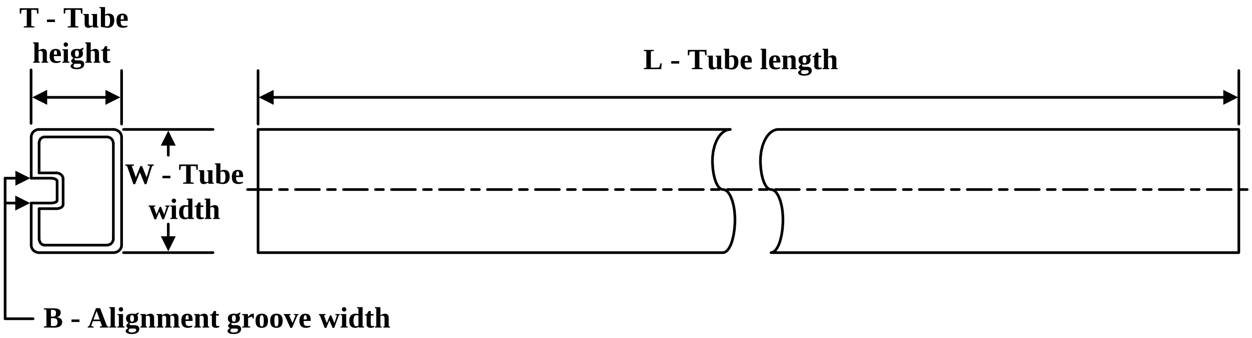
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AM26C31CDBR	SSOP	DB	16	2000	356.0	356.0	35.0
AM26C31CDR	SOIC	D	16	2500	340.5	336.1	32.0
AM26C31CNSR	SO	NS	16	2000	356.0	356.0	35.0
AM26C31IDBR	SSOP	DB	16	2000	356.0	356.0	35.0
AM26C31IDR	SOIC	D	16	2500	340.5	336.1	32.0
AM26C31IDRG4	SOIC	D	16	2500	340.5	336.1	32.0
AM26C31INSR	SO	NS	16	2000	356.0	356.0	35.0
AM26C31IPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
AM26C31IPWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
AM26C31QDR	SOIC	D	16	2500	350.0	350.0	43.0
AM26C31QDRG4	SOIC	D	16	2500	340.5	336.1	32.0

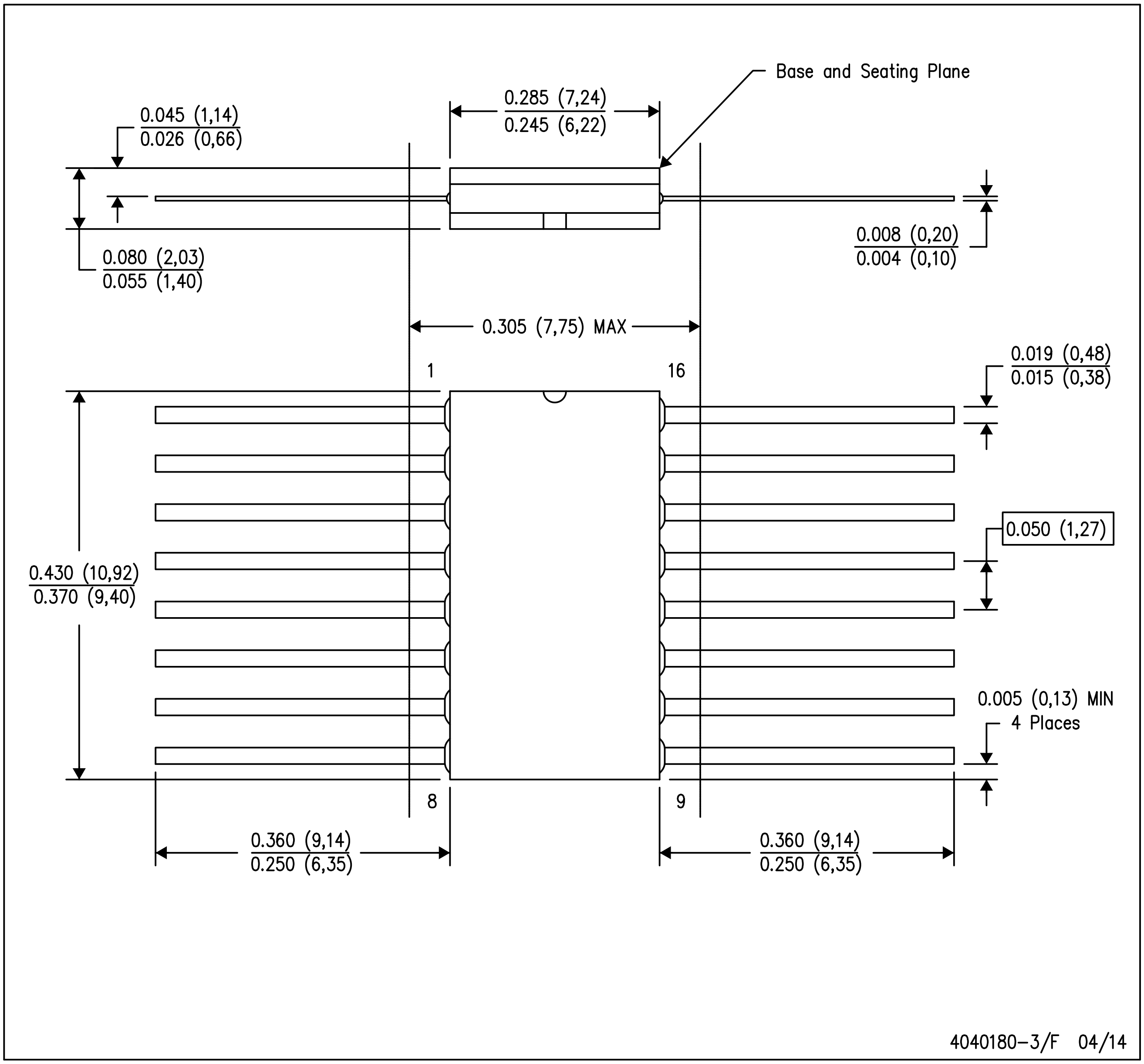
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9163901M2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9163901MFA	W	CFP	16	25	506.98	26.16	6220	NA
5962-9163901Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9163901QFA	W	CFP	16	25	506.98	26.16	6220	NA
AM26C31CD	D	SOIC	16	40	507	8	3940	4.32
AM26C31CDE4	D	SOIC	16	40	507	8	3940	4.32
AM26C31CDG4	D	SOIC	16	40	507	8	3940	4.32
AM26C31CN	N	PDIP	16	25	506	13.97	11230	4.32
AM26C31ID	D	SOIC	16	40	507	8	3940	4.32
AM26C31IDE4	D	SOIC	16	40	507	8	3940	4.32
AM26C31IDG4	D	SOIC	16	40	507	8	3940	4.32
AM26C31IN	N	PDIP	16	25	506	13.97	11230	4.32
AM26C31INE4	N	PDIP	16	25	506	13.97	11230	4.32
AM26C31IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
AM26C31MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
AM26C31MWB	W	CFP	16	25	506.98	26.16	6220	NA
AM26C31QD	D	SOIC	16	40	505.46	6.76	3810	4
AM26C31QDG4	D	SOIC	16	40	505.46	6.76	3810	4

W (R-GDFP-F16) CERAMIC DUAL FLATPACK



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP2-F16

GENERIC PACKAGE VIEW

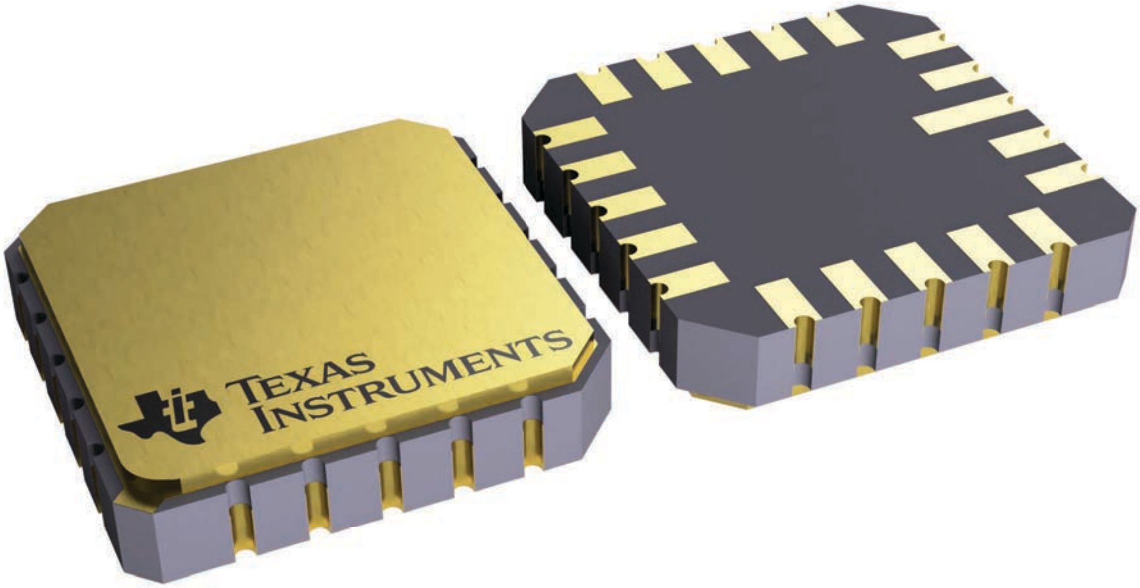
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

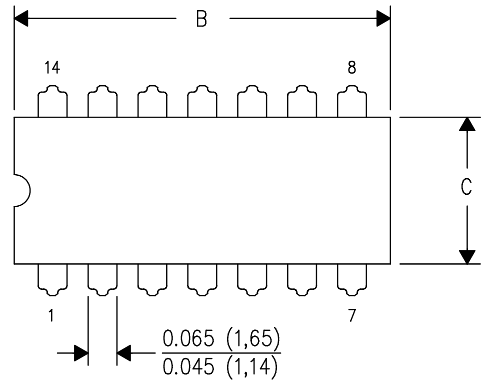
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



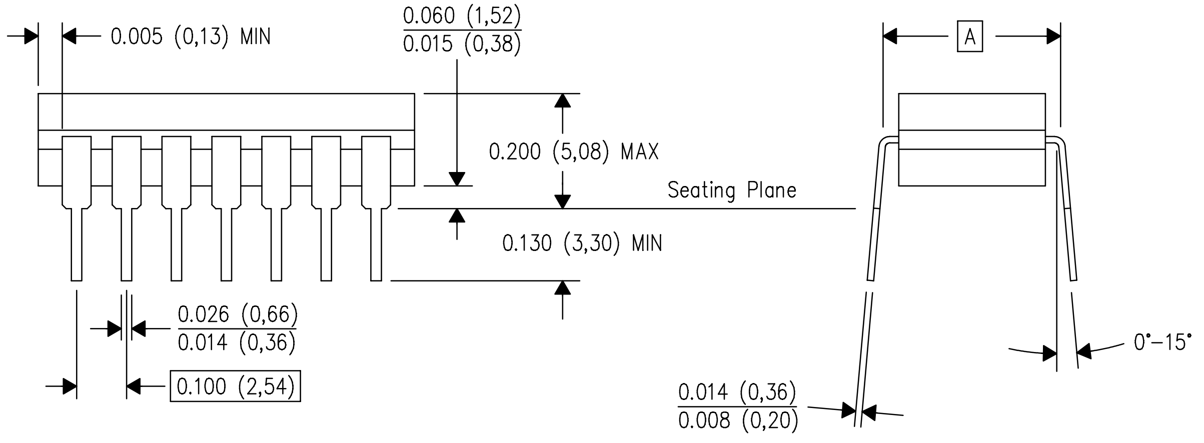
J (R–GDIP–T**)

CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

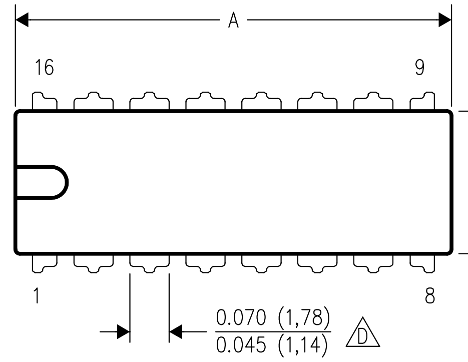


4040083/F 03/03

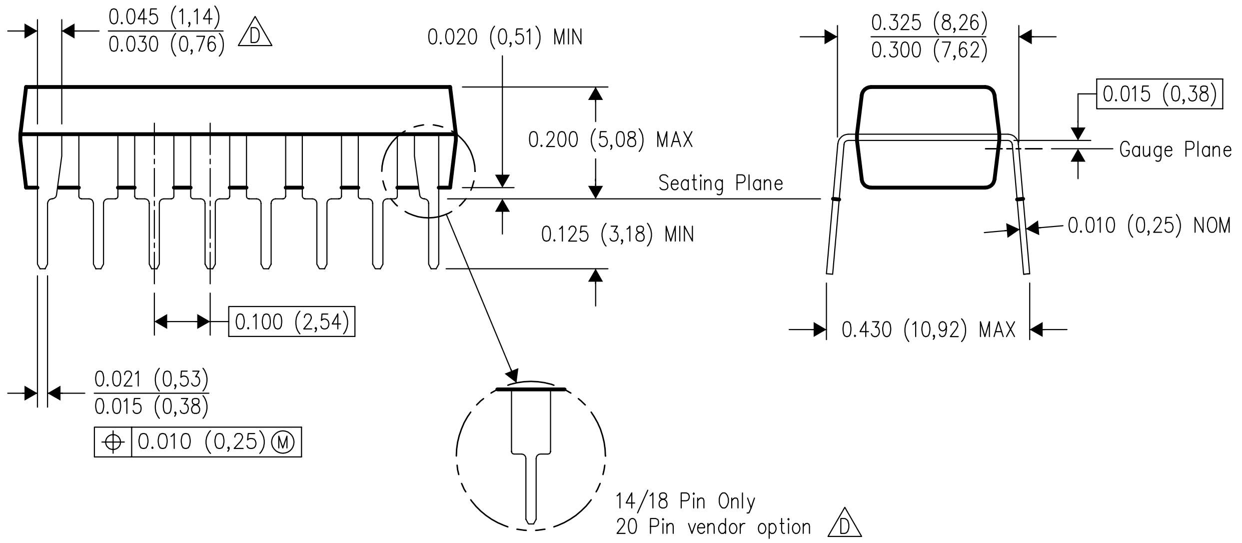
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

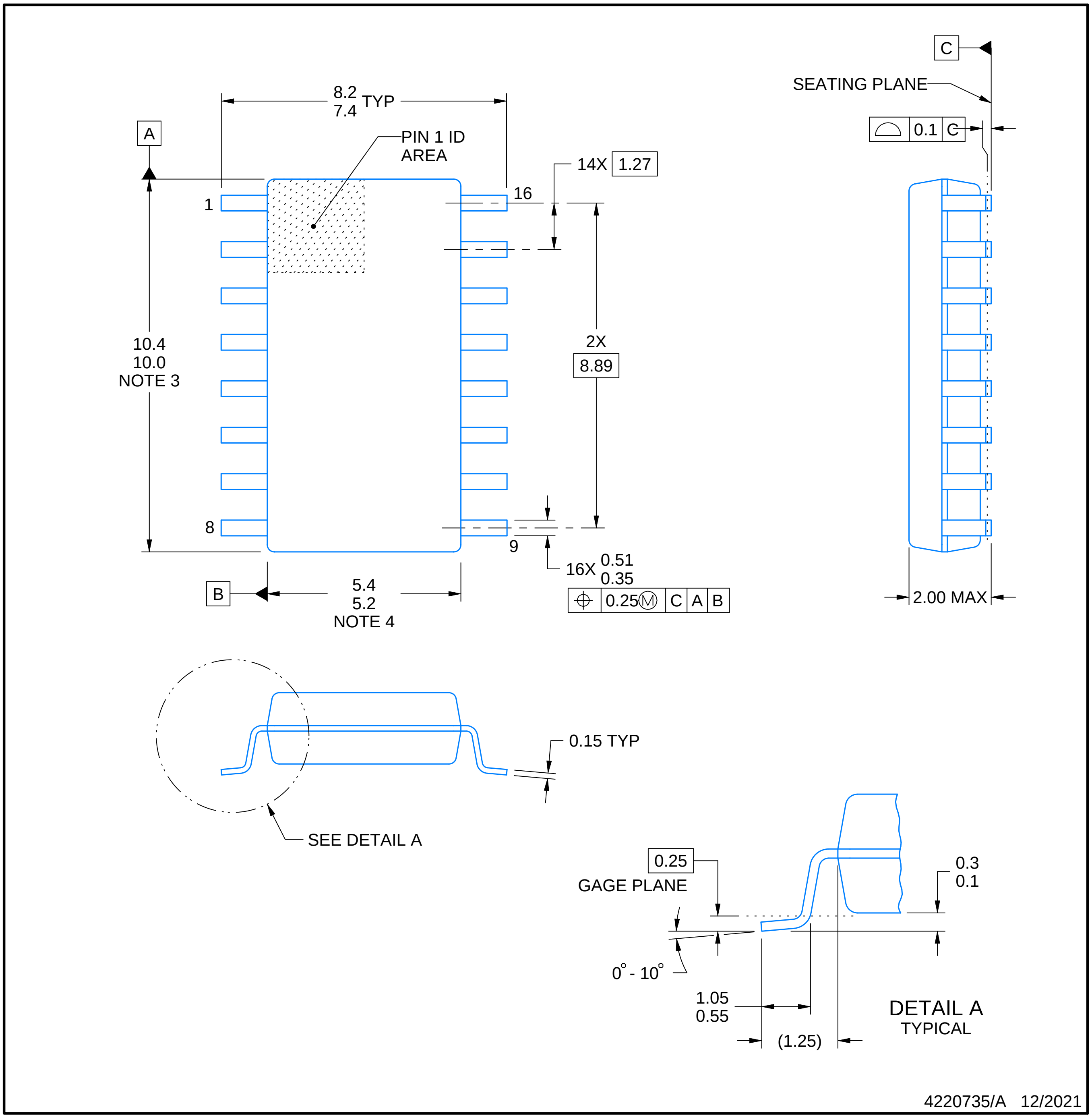


PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD



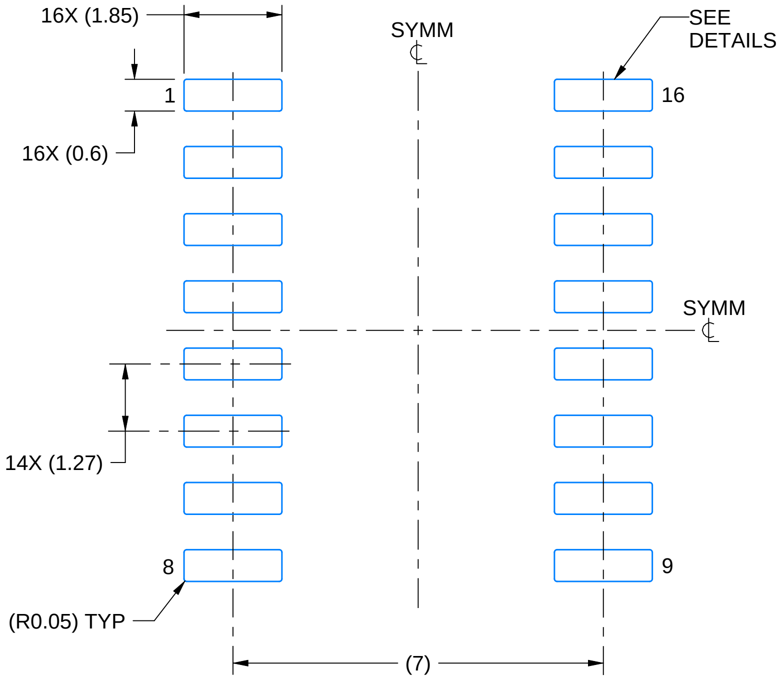
4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

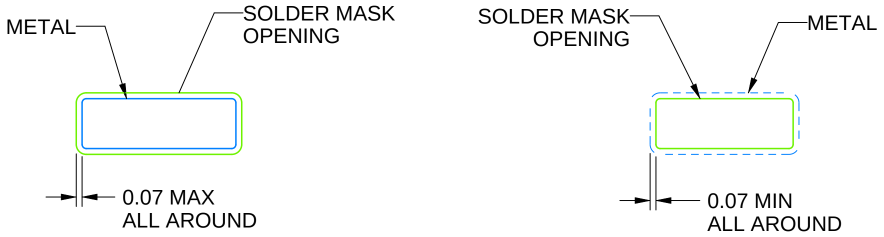


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



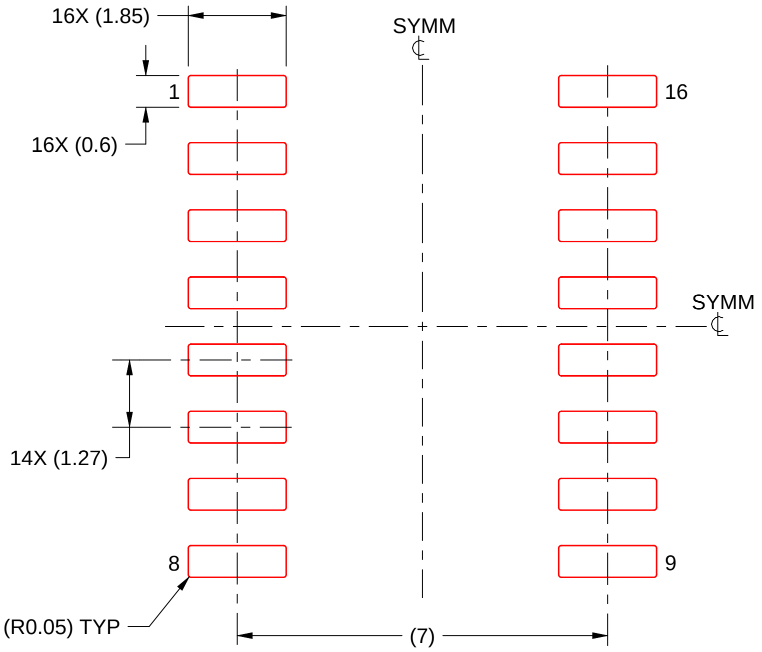
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

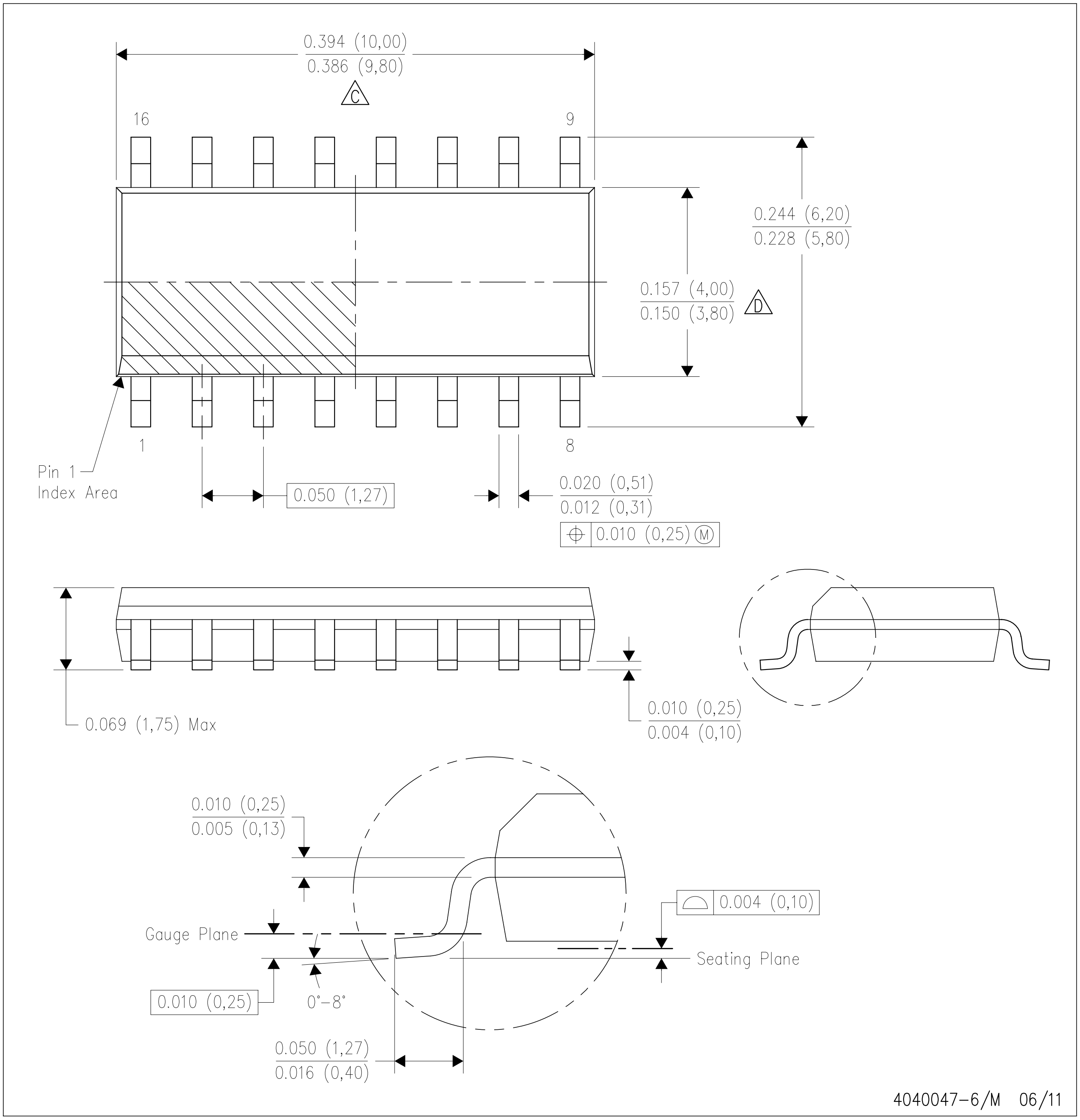


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

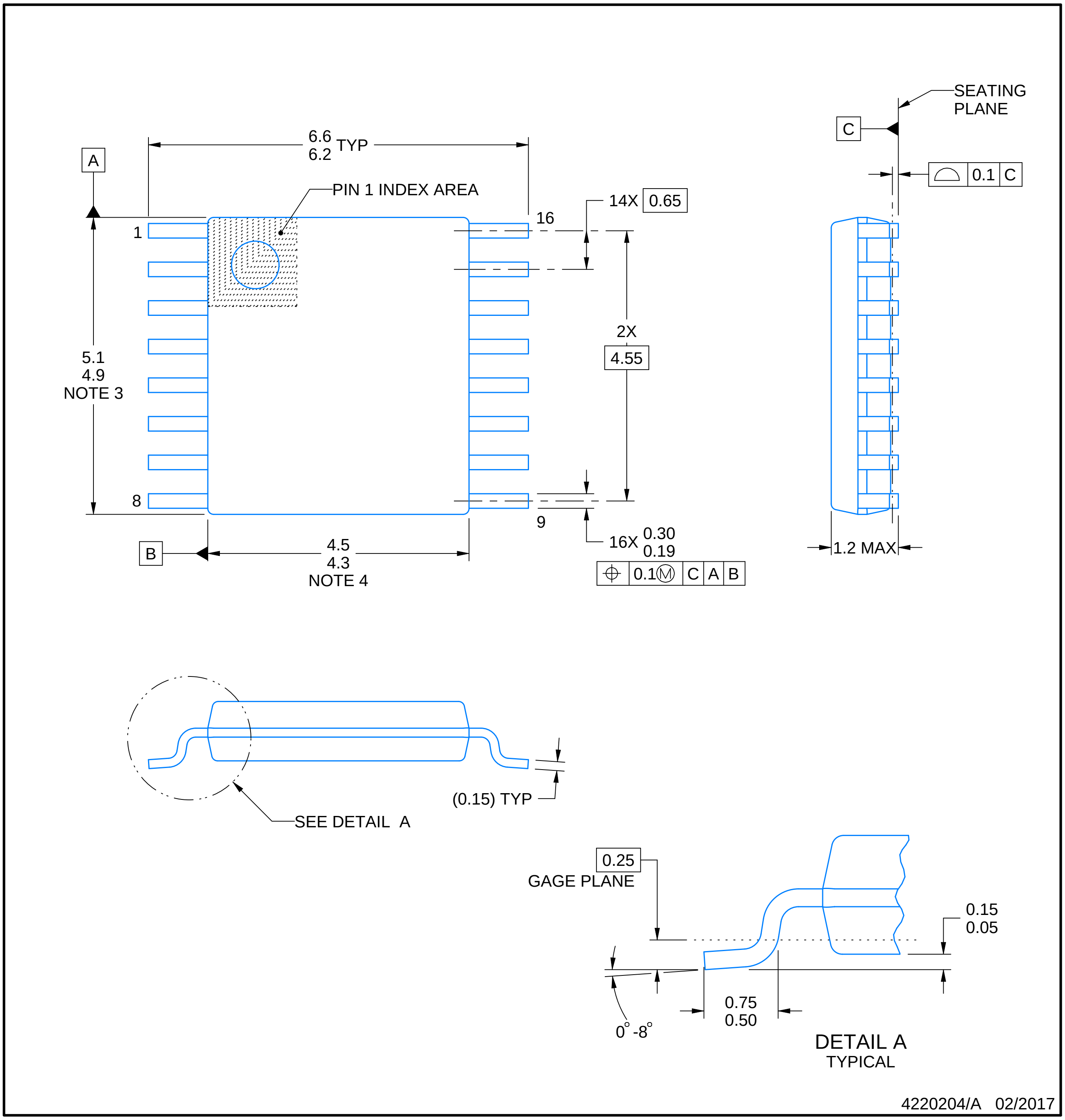
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

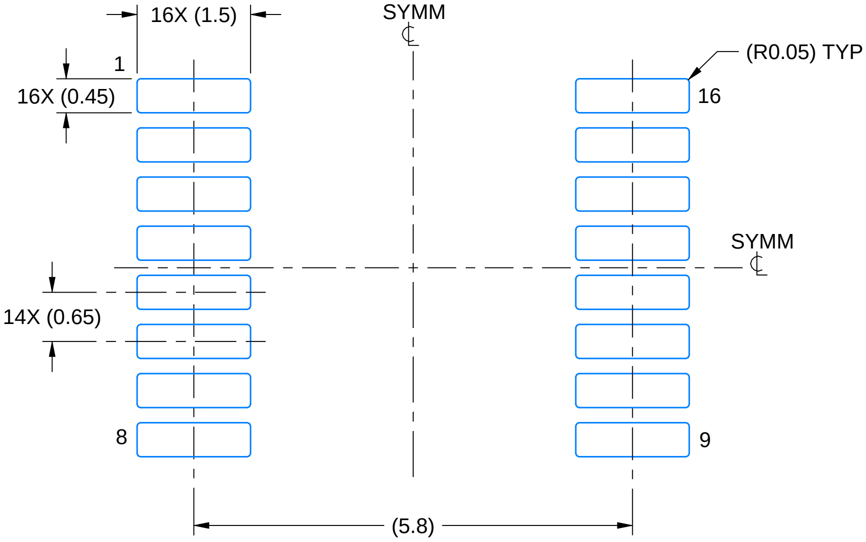


NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AC.

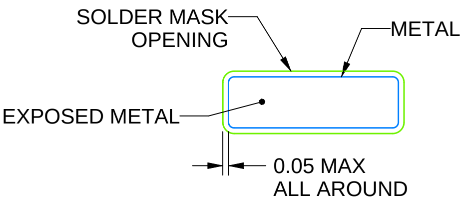


NOTES:

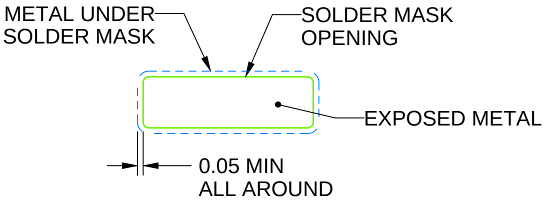
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK
DEFINED
(PREFERRED)



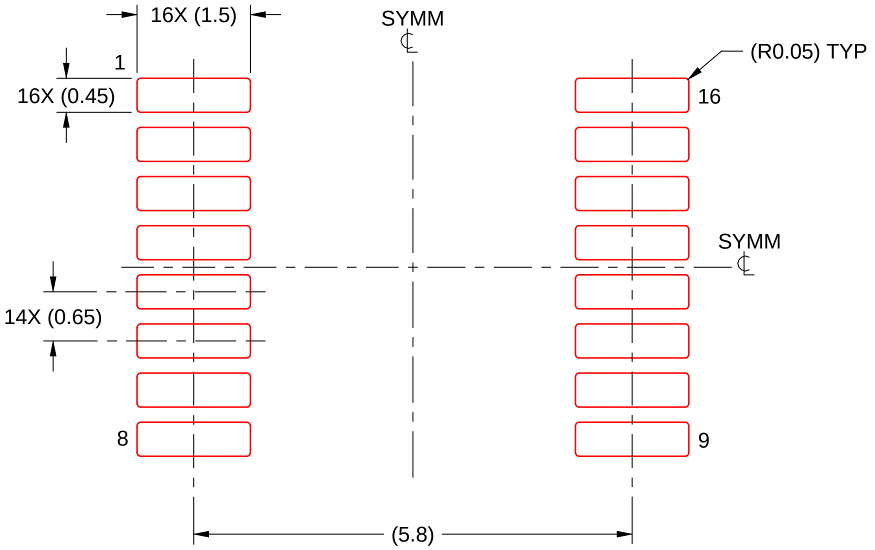
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

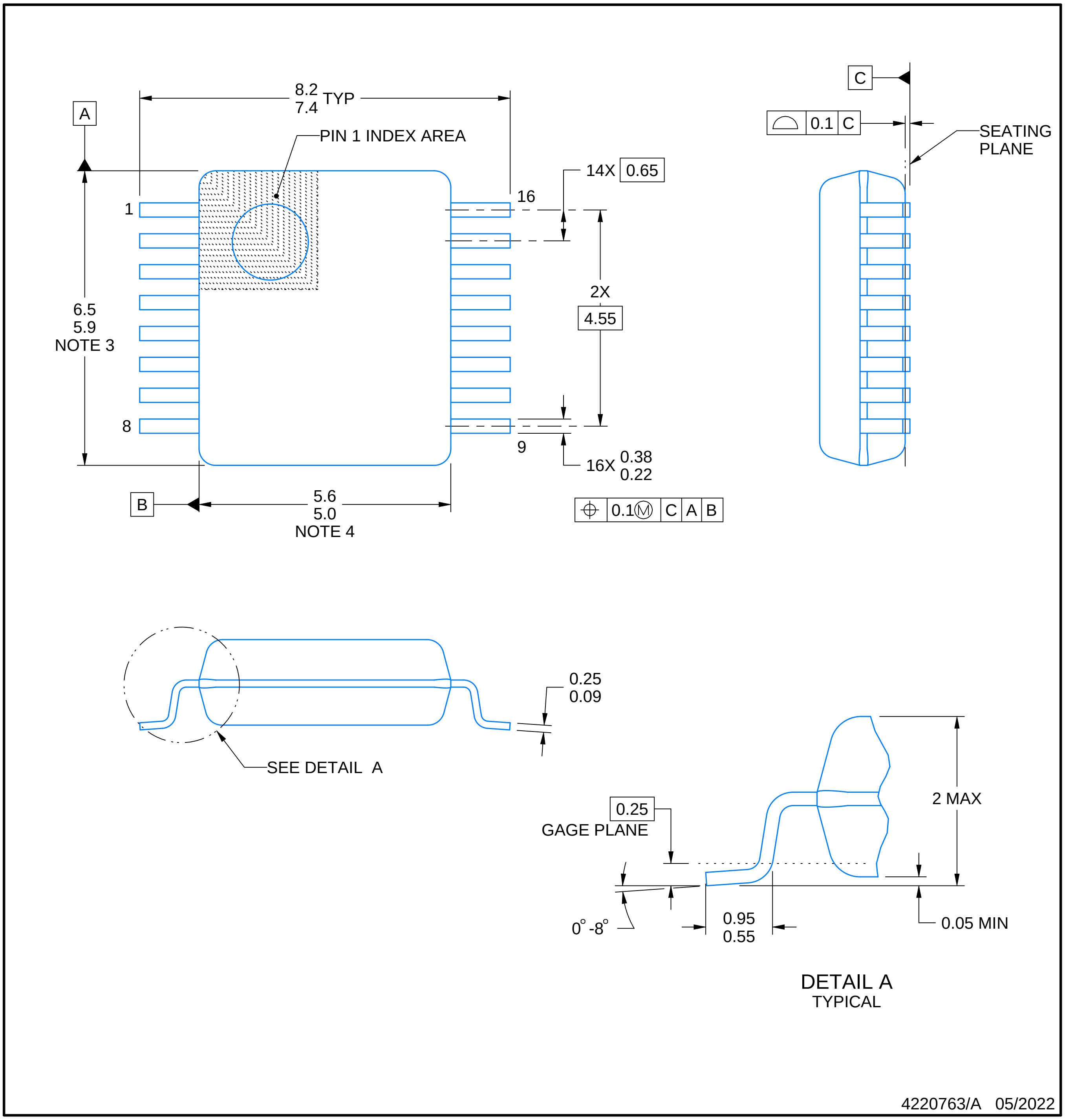


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

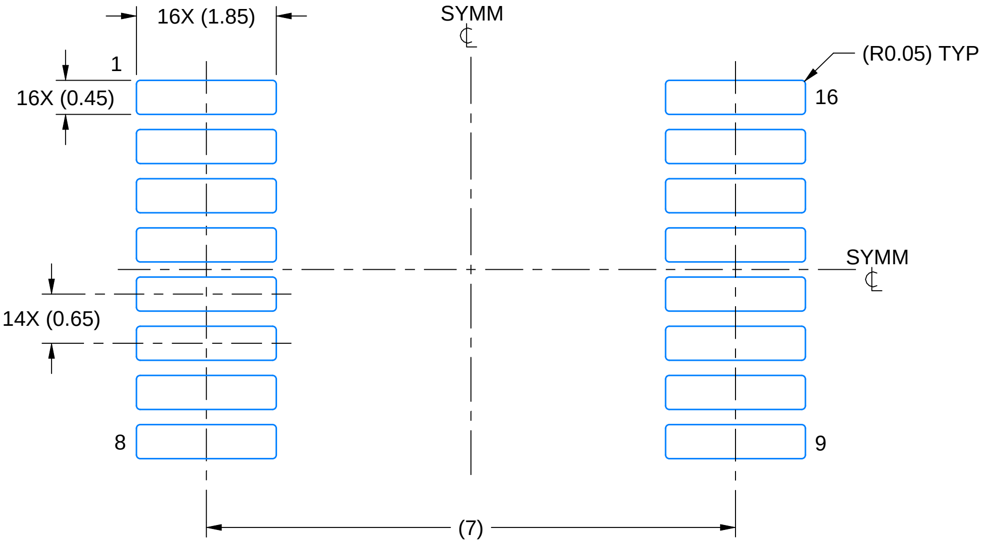
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



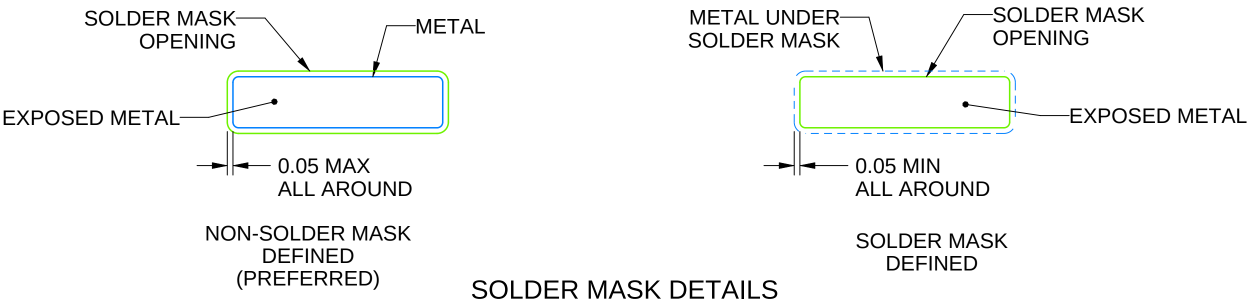
4220763/A 05/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

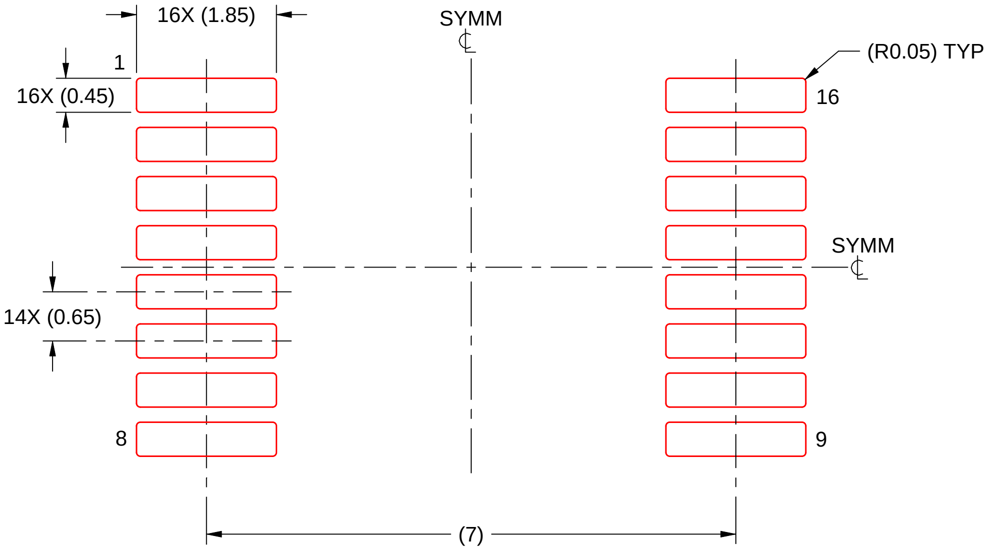


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

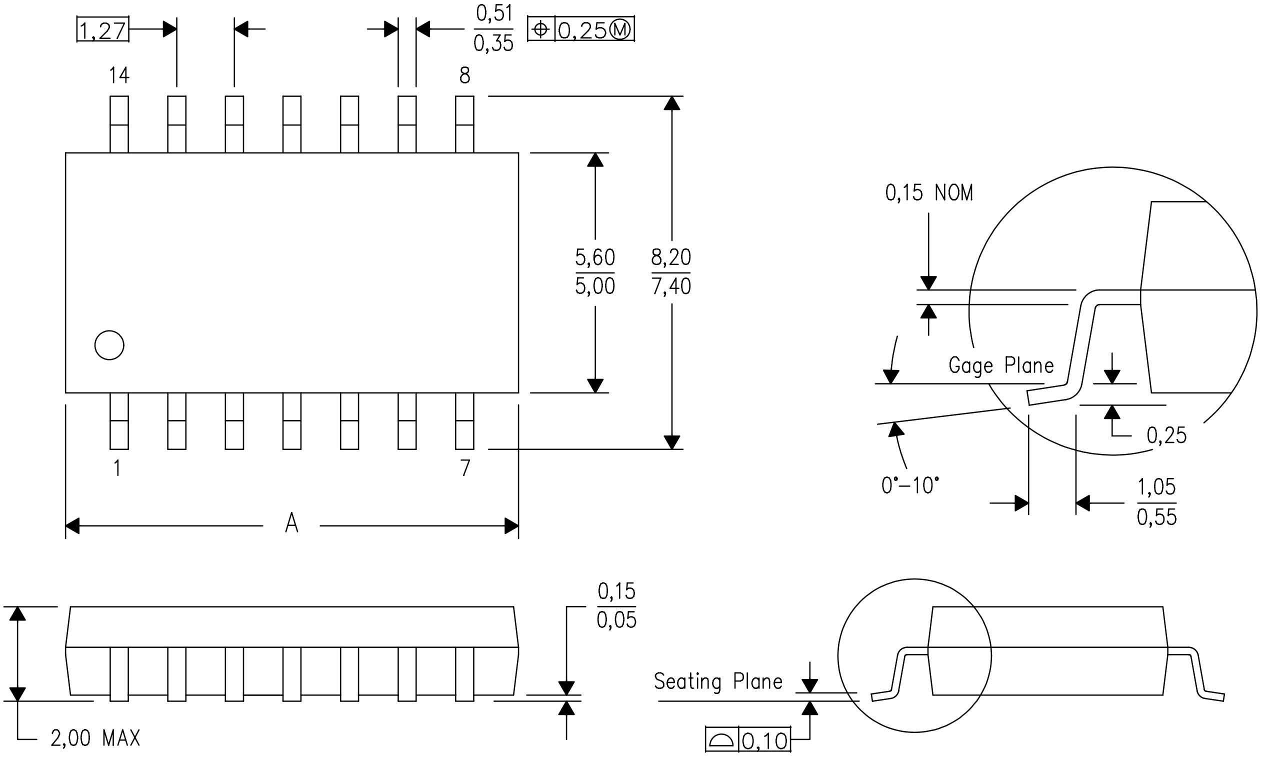
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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